

ABSTRACT

MATRIX CALCULATION APPARATUS, METHOD, SYSTEM, CIRCUIT, AND DEVICE, AND CHIP

5 A matrix calculation apparatus, method, system, circuit, and device, and a chip are provided,
to directly calculate a matrix in a compressed format, thereby improving calculation efficiency of
the matrix in the compressed format. The matrix calculation apparatus includes a vector outer
product processing engine and an accumulator. The matrix calculation apparatus calculates, based
on vector outer products, a first matrix and a second matrix that are in a compressed format. In the
10 calculation process, the vector outer product processing engine performs vector outer product
calculation on a first column vector with reserved row coordinates and a second column vector
with reserved column coordinates, and then the accumulator accumulates, based on indexes of
position coordinates, third element values with same position coordinates to obtain a result matrix
obtained by calculating the two matrices in the compressed format. Compared with a conventional
15 method in which a matrix in a compressed format needs to be first decompressed and then matrix
calculation is performed on a matrix obtained through decompression, the matrix calculation
apparatus provided in embodiments of this application can effectively improve calculation
efficiency of a matrix in a compressed format.

20 FIG. 4A