

5

ELECTRICAL ANTIFUSE WITH EXTERNAL CAPACITANCE

BACKGROUND OF THE INVENTION

10 Technical Field of the Invention

The present invention relates to the field of semiconductors and, more particularly, to programmable antifuse elements in semiconductor memory devices.

Description of the Related Art

15 Integrated circuits often require selectively programmable electrical connections between circuit nodes. Such connections can be implemented by use of an antifuse link which is programmable to interconnect electrodes. For example, antifuses are often used in memory cell arrays such as dynamic random access memories in which failing cell addresses are remapped to functional cell addresses by selective programming of antifuses.

20

Generally, antifuses are fabricated with conductive electrical terminals separated by a dielectric layer. In an "off" state, the anti-fuse has a high resistance between its terminals. The antifuse can be programmed to an "on" state (i.e., a low resistance) by breaking down the

5 interposed dielectric to form a conductive link between the antifuse terminals as described in United States Patent US5,257,222, entitled "Antifuse Programming By Transistor Snap-Back".

Other currently applied antifuse types are structures based on a conventional MOS transistor. Here the MOS transistor is not used in the conventional sense, either as an amplifier or
10 as a switching element, but as a configuration for realizing a dielectric layer ('Gate - oxide') interposed between the gate, source and drain. Such a transistor antifuse is programmed or "blown" by applying a sufficient field or "blow" voltage across the gate oxide of the MOS transistor. The blow process results in a damaged dielectric, which reduces the electrical resistance across the dielectric. Although this blow voltage must reach a threshold value for any
15 breakage to occur in the dielectric, the final resistance resulting from this breakage is lowered if more energy is applied to the antifuse dielectric.

Evaluation circuits attached to the anti-fuse are used to differentiate between the high resistance of the intact oxide (R_{off}) and the lowered resistance of the damaged oxide (R_{on}). The
20 larger the resistance of a programmed antifuse in a memory cell the harder it becomes to determine the status of the antifuse (blown versus unblown).

Typical values for R_{off} are in the range of 10^{12} ohms. The range of R_{on} largely depends on the parameters during the blow process. High blow voltage and high blow current generally lead

5 to lower R_{on} resistances. However, it is desired to minimize those two parameters in order to reduce the size of the associated circuits (e.g. blow voltage generator, blow transistor, wiring, etc.). In current designs, a compromise is made to balance the minimum current needed to reliably blow the antifuse and the area requirements of the blow transistor device to handle that current. From that perspective, values of R_{on} in the range of 10^5 ohms to 10^8 ohms are common.

10 However, with this range of R_{on} , commonly used evaluation circuits are not able to accurately distinguish an unblown anti-fuse and a blown anti-fuse exhibiting the relatively high R_{on} values. Thus, an antifuse may erroneously be detected as un-programmed if the blown antifuse resistance R_{on} is sufficiently large.

15 Thus, there is a need for an improved approach to programming an antifuse which provides a more robust electrical connection which is readily verifiable and distinguishable from an un-programmed antifuse.

5 SUMMARY OF THE INVENTION

The present invention achieves technical advantages as an apparatus, system and method of programming an antifuse comprising of a dielectric interposed between two conductive elements. One of the conductive elements is attached to a capacitor that is precharged to a set
10 voltage. The antifuse is programmed to an “on” state by breaking down the interposed dielectric to form a conductive link between the antifuse terminals from the application of a programming voltage across the conductive elements. Responsive to the applied programming voltage, a field appears on the dielectric which leads to formation of conductive links across it. Electrical energy stored in the capacitor, in response to the formation of these conductive links, is immediately
15 discharged through the links causing a more robust electrical connection between the conductive elements. A particular antifuse can be selected for programming, within an array of such devices, by applying the programming voltage only to the conductive elements of the selected antifuse. Further, the capacitor can be common to a plurality of antifuses in which the capacitor’s stored energy is applied to a select one of the plurality of antifuses, rendered operable by the application
20 of the programming voltage to the conducting elements of the selected antifuse.

5 BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention, reference is made to the following detailed description taken in conjunction with the accompanying drawings wherein:

Figure 1 illustrates a field effect transistor antifuse and electrical connections for applying a programming voltage across the oxide dielectric;

10

Figure 2A illustrates the formation of a filament after a programming voltage is applied across the dielectric;

15

Figure 2B shows a graph of oxide current versus time during the application of a programming voltage;

Figure 3 illustrates a field effect transistor with associated circuitry for applying a programming voltage across the dielectric in accordance with an exemplary embodiment of the present invention; and

20

Figure 4 illustrates an arrangement for applying a programming voltage across the dielectric of a select one of a plurality of field effect transistors in accordance with an exemplary embodiment of the present invention.

5 DETAILED DESCRIPTION OF THE INVENTION

The numerous innovative teachings of the present application will be described with particular reference to the presently preferred exemplary embodiments. However, it should be understood that this class of embodiments provides only a few examples of the many
10 advantageous uses and innovative teachings herein. In general, statements made in the specification of the present application do not necessarily delimit any of the various claimed inventions. Moreover, some statements may apply to some inventive features, but not to others.

Throughout the drawings, it is noted that the same reference numerals or letters will be
15 used to designate like or equivalent elements having the same function. A detailed description of known functions and constructions unnecessarily obscuring the subject matter of the present invention have been omitted for clarity.

Referring now to Figure 1 there is illustrated a biasing arrangement for a MOS transistor
20 antifuse 11 in accordance with an exemplary embodiment of the present invention. In this embodiment, the antifuse is a transistor antifuse where one conductive element is formed by the source 14, drain 12 and body 13 which are electrically connected and a second conductive element is formed by the gate 16 with the gate oxide forming the interposed dielectric. The transistor antifuse 11 is programmed or "blown" by applying a sufficient field or "blow" voltage
25 across the gate oxide via the body 13 and the gate 16. The blow process results in a damaged

5 gate-oxide or dielectric, which reduces the electrical resistance across the dielectric. The magnitude of the voltage needed to program the antifuse depends on several factors among which the thickness of the gate oxide should be considered.

As the blow voltage is applied, quasi breakdown events are initiated in the gate oxide
10 resulting in the formation of local charge centers or 'traps' 22 (Figure 2A). When a sufficient number of traps are created they tend to join together, due to the applied field as a conductive filament 21, as exemplified in Figure 2A. This conductive filament enables current to flow thus drawing energy into the system from the power source. Sometimes this filament may disappear due to this energy dissipation but only to reappear at a different location. After a number of such
15 events, there is a catastrophic event (illustrated as a plot diagram in Figure 2B) that causes the formation of a stable filament resulting in the final low resistance state.

Figure 2B shows the oxide current over a period of time with a blow voltage applied across the gate and the body. The several spikes in the current are due to the appearance and
20 subsequent disappearance of the filaments. The final large spike indicates the catastrophic event caused by the formation of a stable filament. After programming (blown), the resistance between the gate 16 and body 13 is reduced from a typical starting resistance of 10^{12} ohms (un-programmed or unblown). However, the conductive filament 22 between the antifuse terminals is

5 sometimes only marginally conductive, leaving a relatively high resistance, which is difficult to detect by evaluation circuits.

Referring now to Figure 3 there is illustrated a field effect transistor (FET) antifuse 300 with associated circuitry for applying a programming voltage across the dielectric in accordance with an exemplary embodiment of the present invention. As shown, circuitry couples the body 10 370, drain 320 and the source 340 to a power supply. In addition, a capacitor 350 or other similar electric energy storage device is included external to the FET antifuse 300 and serially coupled to the drain 320, body 370 and the source 340. The body 370 of the FET antifuse 300 can be connected to an integrated capacitor made on the same substrate. Further, the body 370 is 15 electrically isolated from the substrate or other circuitry on the same chip by an isolation layer 380.

In this embodiment of the invention, the FET antifuse 300 is programmed by the application of a positive voltage on the gate 360 so that a field appears across the gate-oxide 310. 20 The capacitor 350, which has been pre-charged to a set negative voltage, increases the field appearing across the gate-oxide 310 in addition to being a reservoir of some energy prior to the blow operation. When the gate voltage is applied, the generation of the first links across the gate-oxide 310 provides a path for the immediate discharge, of the energy stored in the capacitor 350, across the oxide 310. This additional energy enables the formation of additional links and/or

5 increases the diameter of the first links that are formed across the oxide 310. The magnitude of the additional energy is related to the capacitance and the pre-charge voltage as:

$$E = \frac{1}{2} C V_{dd}^2.$$

Where E is the total energy available, C is the capacitance and V_{dd} is the pre-charge voltage.

The magnitude of the pre-charge voltage used should be such that it does not damage the
10 dielectric of an unselected fuse. Further, it is constrained by the nature of the isolation layer 380. Typical values could range between -1.5V and -2.5V. The magnitude of the capacitance achievable depends on the area and the type of capacitor used. Typical values ranges between 1 nanoFarad and 300 nanoFarads.

15 In addition, the capacitor 350 can be adapted to be common to an array of antifuses (further discussed herein) thus decreasing the total area occupied by the antifuses. Further, the capacitor 350 can be integrated with the FET antifuse in a standard CMOS process used for the manufacture of integrated circuits. A suitable way to integrate a capacitor of necessary capacity within close proximity to the antifuse is the by the use of devices such as Metal Insulator Metal
20 Capacitors (MIMCAP) or Deep Trench (DT) capacitors.

For the programming operation , V_{dd} is applied to capacitor 350 which precharges it to a predetermined voltage level. The maximum desirable value of V_{dd} is limited by the thickness of the gate oxide, as an excessively large voltage could damage the gate oxide even prior to

5 programming and by the type of isolation 380 of the transistor. In this embodiment, Vdd is in the range of approximately -1.5 to -2.5 V and the gate oxide ranges between 20 angstroms to 35 angstroms. Further, a bias voltage (hereinafter referred to as Vblow) is applied to the gate 360 in which Vblow is preferably in the range of 5V to 8V. Although the same field in the oxide can be obtained by using the same voltages but of the opposite polarity, it is believed that the
10 programming is enhanced with this particular choice of the polarity.

Following the application of Vblow, the first conductive links are formed in the gate-oxide 310. It is important to note that the voltage Vdd in itself, without Vblow, is not high enough to start this process, for in such a case the ability to select a specific antifuse to be
15 programmed would be lost. The stored energy in the capacitor 350 is instantaneously discharged across the damaged gate-oxide 310, which forms additional conductive links and/or causes the increase of the diameter of the first formed conductive links. With this programming approach, the resistance of the antifuse 300 is lowered to a range of approximately 10^3 to 10^4 ohms while without the capacitor typical final resistances range from 10^6 to 10^8 ohms. The additional
20 conductive links and/or increased diameter of the first formed conductive links also improve the reliability and consistency of the blow operation.

Referring now to Figure 4 there is illustrated an arrangement for applying a programming voltage across the dielectric of a select one of a plurality of field effect transistor antifuses in

5 accordance with an exemplary embodiment of the present invention. The circuitry is adapted to couple, in parallel, a plurality of FET antifuses with a common capacitor 350. V_{blow} and V_{dd} are chosen such that only those antifuses to which V_{blow} is applied are programmed. V_{dd} is applied to the body 370 of all the antifuses and also serves to precharge the capacitor 350. V_{dd} can be applied through a switch 410. V_{blow} can be selectively applied to different ones of the
10 FET gates 360 (e.g. by suitable logic circuitry) so that only those antifuses that are selected are blown. Note that only two antifuses are explicitly shown, however, many other antifuses can be included, as indicated in Figure 4. In the programmed antifuse, conductive filaments are formed, while in the remaining antifuses they are not, as the field across their gate oxides is lower.

15 The above described capacitor arrangements can be easily integrated into the standard process used in the manufacture of CMOS memory devices. Generally, such memory devices are made of individual memory cells and include redundant cells for faulty memory cell replacement. A test program can locate faulty memory cells and subsequently appropriately coupled antifuses, such as described above, are blown so that they enable the replacement of the faulty cells with the
20 redundant cells. A collection of antifuses can also be used as Programmable Read Only Memory elements (PROM) or for customizable chips (Field Programmable Gate Arrays).

5 It should be noted that although the present embodiments have been described in terms of programming a FET transistor antifuse, the present invention can be implemented with other types of antifuses in which a dielectric is interposed between conductive elements.

10 Although a preferred embodiment of the method, apparatus, and system of the present invention has been illustrated in the accompanied drawings and described in the foregoing Detailed Description, it is understood that the invention is not limited to the embodiments disclosed, but is capable of numerous rearrangements, modifications, and substitutions without departing from the spirit of the invention as set forth and defined by the following claims.

5

WHAT IS CLAIMED IS:

1. A method of programming an antifuse comprising a dielectric disposed between conductive elements, said method comprising:

10 storing electrical energy in a storage device coupled to one of said conductive elements;
and

applying a programming voltage to a further one of said conductive elements;

releasing said stored electrical energy across said dielectric via said one and said further one conductive elements responsive to said applied programming voltage.

15

2. The method of Claim 1 further comprising forming a conductive filament through said dielectric responsive to said applied programming voltage.

3. The method of Claim 2, wherein said releasing step further comprises passing a
20 current through one of said conductive filament and a further conductive filament.

4. The method of Claim 1 further comprising reducing a resistance between said one and said further one conductive elements of said antifuse to a range of approximately 10^3 to 10^4 ohms.

5

5. The method of Claim 1, wherein said programming voltage is in a range of approximately 5 to 8 volts.

6. The method of Claim 1, wherein said antifuse is a field effect transistor antifuse, said dielectric is gate oxide of said field effect transistor antifuse, said one conductive element is a gate of said field effect transistor antifuse, and said further one conductive element is a drain, source and body of said field effect transistor antifuse, wherein said drain, source and body are electrically coupled.

7. The method of Claim 6, wherein said storage device is a capacitor precharged to a predetermined voltage by applying a power supply to said body of said field effect transistor.

5 8. An apparatus comprising:
an antifuse having a dielectric disposed between a plurality of conductive elements;
an input coupled to one of said plurality of conductive elements and adapted to permit
application of a programming voltage; and
a storage device coupled to a further one of said plurality of conductive elements and
10 operable to store electric energy, said storage device further operable to release said stored
electric energy to said antifuse responsive to application of said programming voltage.

9. The apparatus of Claim 8, wherein said storage device is a capacitor.

15 10. The apparatus of Claim 8, wherein said antifuse is responsive to said programming
voltage for forming a conductive link through said dielectric, and wherein said storage device is
operable to pass a current through one of said conductive link and a further conductive link.

20 11. The apparatus of Claim 10, wherein a resistance between said one and said further
one conductive elements is reduced to a range of approximately 10^3 to 10^4 ohms responsive to
said storage device passing a current through one of said conductive link and said further
conductive link.

5 12. The apparatus of Claim 8, wherein said antifuse is a field effect transistor, said one
conductive element is a gate of said field effect transistor, said dielectric is gate oxide of said field
effect transistor, and said further one conductive element is an electrically coupled arrangement
of a drain, source and body of said field effect transistor.

10 13. The apparatus of Claim 12 further including at least one further field effect
transistor antifuse, and wherein said storage device is coupled to a body of each of said field
effect transistor antifuses and operable to release said stored electrical energy to a select one of
said field effect transistor antifuses.

15 14. The apparatus of Claim 13, wherein selection of said field effect transistor antifuse
is operable by application of said programming voltage.

5 15. A system for use with a plurality of addressable memory cells, said system comprising:

 a plurality of programmable antifuses each having a dielectric disposed between a plurality of conductive elements and operable to provide remapping of a memory cell address;

 an input structure coupled to one of said plurality of conductive elements for each antifuse
10 and adapted to permit a programming of any selected one of said programmable antifuses by application of a programming voltage thereto; and

 a storage device coupled to a further one of said plurality of conductive elements for each antifuse and operable to store electric energy, said storage device further operable to release said stored electric energy to a selected programmable antifuse responsive to said applied
15 programming voltage.

 16. The system of Claim 15, wherein said antifuses are responsive to said programming voltage for forming a conductive link through said dielectric, and wherein said storage device is operable to pass a current through one of said conductive link and a further
20 conductive link.

5 17. The system of Claim 15, wherein a resistance between said one and said further one conductive elements is reduced to a range of approximately 10^3 to 10^4 ohms responsive to said storage device passing a current through one of said conductive link and said further conductive link.

10 18. The system of Claim 15, wherein said antifuse is a field effect transistor, said one conductive element is a gate of said field effect transistor, said dielectric is gate oxide of said field effect transistor, and said further one conductive element is an electrically coupled arrangement of a drain, source and body of said field effect transistor.

15 19. The system of Claim 18, wherein said storage device is a capacitor precharged to a predetermined voltage by applying a power supply to said body of said field effect transistors.

 20. The system of Claim 15, wherein said programming voltage is in a range of approximately 5 to 8 volts.

20