TITLE OF THE INVENTION

Semiconductor device and production method therefor

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001]

The present invention relates to a semiconductor device.

2. Description of the Background Art

[0002]

A degree of integration in a semiconductor device, particularly in an integrated circuit using a MOS transistor, has been increasing year by year. Along with the increase in the degree of integration, miniaturization of the MOS transistor used therein has progressed to a nano region. The progress in miniaturization of the MOS transistor, which constitutes an inverter circuit as a basic circuitry for digital circuits, gives rise to a problem, such as difficulty in suppressing a leak current, which causes deterioration in reliability due to hot carrier effects and poses an impediment to sufficiently reducing a circuit occupancy area while meeting a requirement of ensuring a necessary current magnitude. With a view to solving this problem, there have been proposed a surrounding gate transistor (SGT) having a structure in which a source, a gate and a drain are arranged in a direction perpendicular to a substrate, wherein the gate is formed to surround an island-shaped semiconductor layer, and a CMOS inverter circuit using the SGT (SGT-based CMOS inverter) (see, for example, the following Non-Patent Document 1).

[0003]

FIG. 1 is a circuit diagram showing an inverter. The inverter comprises a pMOS transistor and an nMOS transistor. In the inverter circuit, the pMOS transistor is required to have a gate width two times greater than that of the nMOS transistor, because a hole mobility is one-half of an electron mobility. Therefore, a conventional SGT-based CMOS inverter is made up using two pMOS SGTs and one nMOS SGT. In other words, the conventional SGT-based CMOS inverter circuit is made up using a total of three island-shaped semiconductors.

[0004]

[Non-Patent Document 1] S. Watanabe, K. Tsuchida, D. Takashima, Y. Oowaki, A. Nitayama, K. Hieda, H. Takato, K. Sunouchi, F. Horiguchi, K. Ohuchi, F. Masuoka, H. Hara, "A Novel Circuit Technology with Surrounding Gate Transistors (SGT's) for Ultra High Density DRAM's," IEEE JSSC, Vol. 30, No. 9, 1995

SUMMARY OF THE INVENTION

[0005]

It is therefore an object of the present invention to allow an inverter to be made up using a single island-shaped semiconductor, so as to provide a semiconductor device comprising a highly-integrated SGT-based CMOS inverter circuit.

[0006]

In order to achieve the above object, according to a first aspect of the present invention, there is provided a semiconductor device which comprises: a first island-shaped semiconductor layer; a first gate dielectric film located on and in contact with at least a part of a periphery of the first island-shaped semiconductor layer; a gate electrode having one surface in contact with the first gate dielectric film; a second gate dielectric film in contact with the other surface of the gate electrode; a second semiconductor layer in contact with the second gate dielectric film; a first first-conductive-type high-concentration semiconductor layer disposed on top of the first island-shaped semiconductor layer; a second first-conductive-type high-concentration semiconductor layer disposed underneath the first island-shaped semiconductor layer; a first second-conductive-type high-concentration semiconductor layer disposed on top of the second semiconductor layer; and a second second-conductive-type high-concentration semiconductor layer disposed underneath the second semiconductor layer.

[0007]

According to a second aspect of the present invention, there is provided a semiconductor device which comprises: an island-shaped semiconductor layer; a first gate dielectric film surrounding a periphery of the island-shaped semiconductor layer; a gate electrode surrounding a periphery of the first gate dielectric film; a second gate dielectric

film surrounding a periphery of the gate electrode; a tubular semiconductor layer surrounding a periphery of the second gate dielectric film; a first first-conductive-type high-concentration semiconductor layer disposed on top of the island-shaped semiconductor layer; a second first-conductive-type high-concentration semiconductor layer disposed underneath the island-shaped semiconductor layer; a first second-conductive-type high-concentration semiconductor layer disposed on top of the tubular semiconductor layer; and a second second-conductive-type high-concentration semiconductor layer disposed underneath the tubular semiconductor layer;

[0008]

According to a third aspect of the present invention, there is provided a semiconductor device which comprises: an island-shaped semiconductor layer; a first gate dielectric film surrounding a periphery of the island-shaped semiconductor layer; a gate electrode surrounding a periphery of the first gate dielectric film; a second gate dielectric film surrounding a periphery of the gate electrode; a tubular semiconductor layer surrounding a periphery of the second gate dielectric film; a first first-conductive-type high-concentration semiconductor layer disposed on top of the island-shaped semiconductor layer; a second first-conductive-type high-concentration semiconductor layer disposed underneath the island-shaped semiconductor layer; a first second-conductive-type high-concentration semiconductor layer disposed on top of the tubular semiconductor layer; a second second-conductive-type high-concentration semiconductor layer disposed underneath the tubular semiconductor layer; a third first-conductive-type high-concentration semiconductor layer disposed underneath the second first-conductive-type high-concentration semiconductor layer and the second second-conductive-type high-concentration semiconductor layer; a first semiconductor-metal compound layer formed in a part of sidewalls of the second second-conductive-type high-concentration semiconductor layer and the third first-conductive-type high-concentration semiconductor layer; a second semiconductor-metal compound layer formed in an upper portion of the first first-conductive-type high-concentration semiconductor layer; and a third semiconductor-metal compound layer formed in an upper portion of the first second-conductive-type high-concentration semiconductor layer.

[0009]

According to a fourth aspect of the present invention, there is provided a semiconductor device which comprises: an island-shaped semiconductor layer; a first gate dielectric film surrounding a periphery of the island-shaped semiconductor layer; a gate electrode surrounding a periphery of the first gate dielectric film; a second gate dielectric film surrounding a periphery of the gate electrode; a tubular semiconductor layer surrounding a periphery of the second gate dielectric film; a first n+-type semiconductor layer disposed on top of the island-shaped semiconductor layer; a second n+-type semiconductor layer disposed underneath the island-shaped semiconductor layer; a first p+-type semiconductor layer disposed on top of the tubular semiconductor layer; and a second p+-type semiconductor layer disposed underneath the tubular semiconductor layer.

[0010]

According to a fifth aspect of the present invention, there is provided a semiconductor device which comprises: an island-shaped semiconductor layer; a first gate dielectric film surrounding a periphery of the island-shaped semiconductor layer; a gate electrode surrounding a periphery of the first gate dielectric film; a second gate dielectric film surrounding a periphery of the gate electrode; a tubular semiconductor layer surrounding a periphery of the second gate dielectric film; a first n+-type semiconductor layer disposed on top of the island-shaped semiconductor layer; a second n+-type semiconductor layer disposed underneath the island-shaped semiconductor layer; a first p+-type semiconductor layer disposed on top of the tubular semiconductor layer; a second p+-type semiconductor layer disposed underneath the tubular semiconductor layer; a third n+-type semiconductor layer disposed underneath the second n+-type semiconductor layer and the second p+-type semiconductor layer; a first semiconductor-metal compound layer formed in a part of sidewalls of the second p+-type semiconductor layer and the third n+-type semiconductor layer; a second semiconductor-metal compound layer formed in an upper portion of the first n+-type semiconductor layer; and a third semiconductor-metal compound layer formed in an upper portion of the first p+-type semiconductor layer.

[0011]

Preferably, the semiconductor device according to the fourth or fifth aspect of the

present invention satisfies the following relation: $Wp \approx 2Wn$, wherein Wp is an inner circumferential length of the tubular semiconductor layer, and Wn is an outer circumferential length of the island-shaped semiconductor layer.

[0012]

Preferably, the semiconductor device according to the fourth or fifth aspect of the present invention satisfies the following relation: $Rp \approx 2Rn$, wherein Rp is an inner radius of the tubular semiconductor layer, and Rn is a radius of the island-shaped semiconductor layer.

[0013]

Preferably, the semiconductor device according to the fourth or fifth aspect of the present invention satisfies the following relation: $Lp \approx Ln$, wherein Lp is a channel length of the tubular semiconductor layer, and Ln is a channel length of the island-shaped semiconductor layer.

[0014]

In the semiconductor device according to the fourth or fifth aspect of the present invention, it is preferable that the first gate dielectric film is a dielectric film allowing an nMOS transistor to function as an enhancement type, wherein the nMOS transistor comprises the island-shaped semiconductor layer, the first gate dielectric film surrounding the periphery of the island-shaped semiconductor layer, the gate electrode surrounding the periphery of the first gate dielectric film, the first n+-type semiconductor layer disposed on top of the island-shaped semiconductor layer and the second n+-type semiconductor layer disposed underneath the island-shaped semiconductor layer, and the second gate dielectric film is a dielectric film allowing a pMOS transistor to function as an enhancement type, wherein the pMOS transistor comprises the gate electrode, the second gate dielectric film surrounding the periphery of the gate electrode, the tubular semiconductor layer surrounding the periphery of the second gate dielectric film, the first p+-type semiconductor layer disposed on top of the tubular semiconductor layer and the second p+-type semiconductor layer disposed underneath the tubular semiconductor layer. Further, it is preferable that the gate electrode is made of a material allowing each of the nMOS transistor and the pMOS transistor to function as an enhancement type.

[0015]

Preferably, in the semiconductor device according to the fifth aspect of the present invention, each of the first to third semiconductor-metal compound layers is a silicon-metal compound layer.

[0016]

In the semiconductor device according to the fourth or fifth aspect of the present invention, it is preferable that the island-shaped semiconductor layer is an island-shaped silicon layer, and the tubular semiconductor layer is a tubular silicon layer. Further, it is preferable that each of the first and second n+-type semiconductor layers or each of the first to third n+-type semiconductor layers is an n+-type silicon layer, and each of the first and second p+-type semiconductor layers is a p+-type silicon layer.

[0017]

More preferably, the island-shaped semiconductor layer is a p-type or non-doped island-shaped silicon layer, and the tubular semiconductor layer is an n-type or non-doped tubular silicon layer.

[0018]

According to a fifth aspect of the present invention, there is provided a method of producing the above semiconductor device. The method comprises the step of implanting arsenic into a p-type or non-doped silicon layer formed on an oxide film, to form the third n+-type silicon layer.

[0019]

Preferably, the method according to a fifth aspect of the present invention further comprises the steps of: forming a resist for forming the n-type silicon layer, on the p-type or non-doped silicon layer; implanting phosphorus into the p-type or non-doped silicon layer to form the n-type silicon layer in a part of the p-type or non-doped silicon layer; stripping away the resist; and subjecting the silicon layers to a heat treatment.

[0020]

Preferably, the method according to a fifth aspect of the present invention further comprises the steps of: depositing an oxide film on the p-type or non-doped silicon layer or on the p-type or non-doped silicon layer and the n-type silicon layer; depositing a nitride

film on the oxide film; forming a resist for forming the island-shaped silicon layer; etching the nitride film and the oxide film to form a nitride film-based hard mask for forming the island-shaped silicon layer; stripping away the resist; depositing an oxide film; etching the oxide film to form an oxide film-based sidewall which defines a position of a gate-forming region to be subsequently formed; depositing an nitride film; and etching the nitride film to form a nitride film-based sidewall which defines a position of the tubular silicon layer to be subsequently formed.

[0021]

Preferably, the above method further comprises the steps of: after the step of etching the nitride film, forming a resist for forming an output terminal region; etching the n-type or non-doped silicon layer to form an output terminal region; stripping away the resist; etching away the oxide film-based sidewall; and etching the p-type or non-doped silicon layer and the n-type or non-doped silicon layer to form the island-shaped silicon layer and the tubular silicon layer.

[0022]

Preferably, the method further comprises the steps of: after the step of etching the p-type or non-doped silicon layer and the n-type or non-doped silicon layer, stripping away the nitride film and the oxide film; depositing an oxide film; etching the oxide film to form an oxide film-based sidewall for protecting a channel during ion implantation in a subsequent step; forming a resist for forming the first n+-type silicon layer and the second n+-type silicon layer; implanting arsenic into the island-shaped silicon layer to form the first n+-type silicon layer and the second n+-type silicon layer; stripping away the resist; forming a resist for forming the first p+-type silicon layer and the second p+-type silicon layer; implanting boron into the tubular silicon layer to form the first p+-type silicon layer and the second p+-type silicon layer; stripping away the resist; and subjecting the first and second n+-type silicon layers and the first and second p+-type silicon layers to a heat treatment.

[0023]

Preferably, the method further comprises the steps of: after the step of subjecting the first and second n+-type silicon layers and the first and second p+-type silicon layers to a

heat treatment, depositing an oxide film and then flattening and etching-back the oxide film to expose the first n+-type silicon layer and the first p+-type silicon layer; forming a resist for etching the oxide film in the gate-forming region; etching the oxide film in the gate-forming region; stripping away the resist; depositing a high-k film comprising a hafnium oxide film to be formed as the first and second gate dielectric films; depositing a metal film comprising a titanium nitride film or a tantalum nitride film to be formed as the gate electrode, and then flattening the metal film; depositing a nitride film; forming a resist for forming a gate pad; etching the nitride film; stripping away the resist; etching the metal film to form the gate electrode; depositing a nitride film; etching the nitride film to form a nitride film-based sidewall; and etching the high-k film to form the first and second gate dielectric films.

[0024]

Preferably, the method further comprises the steps of: after the step of etching the nitride film, forming a resist for etching the oxide film; dry-etching the oxide film; stripping away the resist; wet-etching the oxide film to expose the second p+-type silicon layer; depositing a nitride film; etching the nitride film to form a nitride film-based sidewall; wet-etching the oxide film to expose the third n+-type silicon layer; and depositing a metal comprising nickel or cobalt and then subjecting the metal film to a heat treatment, whereafter an unreacted metal film is removed, whereby the first silicon-metal compound layer, the second silicon-metal compound layer, and the third silicon-metal compound layer, are formed, respectively, in a part of sidewalls of the second p+-type silicon layer and the third n+-type silicon layer, an upper portion of the first n+-type silicon layer, and an upper portion of the first p+-type silicon layer.

[0025]

Preferably, the method further comprises the steps of: after the step of depositing a metal, forming an oxide film as an interlayer film; forming a first contact hole, a second contact hole and a third contact hole on the second silicon-metal compound layer, the third silicon-metal compound layer and the gate electrode, respectively; forming a fourth contact hole to expose the first silicon-metal compound layer; depositing a metal comprising tungsten to form four contacts; and forming an input terminal, an output terminal, a Vss

power supply line and a Vdd power supply line.

[0026]

As above, the semiconductor device according to the first aspect of the present invention comprises: a first island-shaped semiconductor layer; a first gate dielectric film located on and in contact with at least a part of a periphery of the first island-shaped semiconductor layer; a gate electrode having one surface in contact with the first gate dielectric film; a second gate dielectric film in contact with the other surface of the gate electrode; a second semiconductor layer in contact with the second gate dielectric film; a first first-conductive-type high-concentration semiconductor layer disposed on top of the first island-shaped semiconductor layer; a second first-conductive-type high-concentration semiconductor layer disposed underneath the first island-shaped semiconductor layer; a first second-conductive-type high-concentration semiconductor layer disposed on top of the second semiconductor layer; and a second second-conductive-type high-concentration semiconductor layer disposed underneath the second semiconductor layer. This makes it possible to provide a semiconductor device comprising a highly-integrated SGT-based CMOS inverter circuit.

[0027]

The semiconductor device according to the second aspect of the present invention comprises: an island-shaped semiconductor layer; a first gate dielectric film surrounding a periphery of the island-shaped semiconductor layer; a gate electrode surrounding a periphery of the first gate dielectric film; a second gate dielectric film surrounding a periphery of the gate electrode; a tubular semiconductor layer surrounding a periphery of the second gate dielectric film; a first first-conductive-type high-concentration semiconductor layer disposed on top of the island-shaped semiconductor layer; a second first-conductive-type high-concentration semiconductor layer disposed underneath the island-shaped semiconductor layer; a first second-conductive-type high-concentration semiconductor layer disposed on top of the tubular semiconductor layer; and a second second-conductive-type high-concentration semiconductor layer disposed underneath the tubular semiconductor layer. This also makes it possible to provide a semiconductor device comprising a highly-integrated SGT-based CMOS inverter circuit.

[0028]

The semiconductor device according to the third aspect of the present invention comprises: an island-shaped semiconductor layer; a first gate dielectric film surrounding a periphery of the island-shaped semiconductor layer; a gate electrode surrounding a periphery of the first gate dielectric film; a second gate dielectric film surrounding a periphery of the gate electrode; a tubular semiconductor layer surrounding a periphery of the second gate dielectric film; a first first-conductive-type high-concentration semiconductor layer disposed on top of the island-shaped semiconductor layer; a second first-conductive-type high-concentration semiconductor layer disposed underneath the island-shaped semiconductor layer; a first second-conductive-type high-concentration semiconductor layer disposed on top of the tubular semiconductor layer; a second second-conductive-type high-concentration semiconductor layer disposed underneath the tubular semiconductor layer; a third first-conductive-type high-concentration semiconductor layer disposed underneath the second first-conductive-type high-concentration semiconductor layer and the second second-conductive-type high-concentration semiconductor layer; a first semiconductor-metal compound layer formed in a part of sidewalls of the second second-conductive-type high-concentration semiconductor layer and the third first-conductive-type high-concentration semiconductor layer; a second semiconductor-metal compound layer formed in an upper portion of the first first-conductive-type high-concentration semiconductor layer; and a third semiconductor-metal compound layer formed in an upper portion of the first second-conductive-type high-concentration semiconductor layer. This also makes it possible to provide a semiconductor device comprising a highly-integrated SGT-based CMOS inverter circuit.

[0029]

The semiconductor device according to the fourth aspect of the present invention comprises: an island-shaped semiconductor layer; a first gate dielectric film surrounding a periphery of the island-shaped semiconductor layer; a gate electrode surrounding a periphery of the first gate dielectric film; a second gate dielectric film surrounding a periphery of the gate electrode; a tubular semiconductor layer surrounding a periphery of

the second gate dielectric film; a first n+-type semiconductor layer disposed on top of the island-shaped semiconductor layer; a second n+-type semiconductor layer disposed underneath the island-shaped semiconductor layer; a first p+-type semiconductor layer disposed on top of the tubular semiconductor layer; and a second p+-type semiconductor layer disposed underneath the tubular semiconductor layer. This also makes it possible to provide a semiconductor device comprising a highly-integrated SGT-based CMOS inverter circuit.

[0030]

The semiconductor device according to the fifth aspect of the present invention comprises: an island-shaped semiconductor layer; a first gate dielectric film surrounding a periphery of the island-shaped semiconductor layer; a gate electrode surrounding a periphery of the first gate dielectric film; a second gate dielectric film surrounding a periphery of the gate electrode; a tubular semiconductor layer surrounding a periphery of the second gate dielectric film; a first n+-type semiconductor layer disposed on top of the island-shaped semiconductor layer; a second n+-type semiconductor layer disposed underneath the island-shaped semiconductor layer; a first p+-type semiconductor layer disposed on top of the tubular semiconductor layer; a second p+-type semiconductor layer disposed underneath the tubular semiconductor layer; a third n+-type semiconductor layer disposed underneath the second n+-type semiconductor layer and the second p+-type semiconductor layer; a first semiconductor-metal compound layer formed in a part of sidewalls of the second p+-type semiconductor layer and the third n+-type semiconductor layer; a second semiconductor-metal compound layer formed in an upper portion of the first n+-type semiconductor layer; and a third semiconductor-metal compound layer formed in an upper portion of the first p+-type semiconductor layer. This also makes it possible to provide a semiconductor device comprising a highly-integrated SGT-based CMOS inverter circuit.

[0031]

In a preferred embodiment of the present invention, the semiconductor device satisfies the following relation: $Wp \approx 2Wn$, wherein Wp is an inner circumferential length of the tubular semiconductor layer, and Wn is an outer circumferential length of the

island-shaped semiconductor layer. This also makes it possible to provide a semiconductor device comprising a highly-integrated SGT-based CMOS inverter circuit wherein a pMOS transistor has a gate width which is two times greater than that of an nMOS transistor.

[0032]

In a preferred embodiment of the present invention, the semiconductor device satisfies the following relation: $Rp \approx 2Rn$, wherein Rp is an inner radius of the tubular semiconductor layer, and Rn is a radius of the island-shaped semiconductor layer. This also makes it possible to provide a semiconductor device comprising a highly-integrated SGT-based CMOS inverter circuit wherein a pMOS transistor has a gate width which is two times greater than that of an nMOS transistor.

[0033]

In a preferred embodiment of the present invention, the semiconductor device satisfies the following relation: $Lp \approx Ln$, wherein Lp is a channel length of the tubular semiconductor layer, and Ln is a channel length of the island-shaped semiconductor layer. This makes it possible to provide a semiconductor device comprising a highly-integrated SGT-based CMOS inverter circuit.

[0034]

In a preferred embodiment of the present invention, the first gate dielectric film is a dielectric film allowing an nMOS transistor to function as an enhancement type, wherein the nMOS transistor comprises the island-shaped semiconductor layer, the first gate dielectric film surrounding the periphery of the island-shaped semiconductor layer, the gate electrode surrounding the periphery of the first gate dielectric film, the first n+-type semiconductor layer disposed on top of the island-shaped semiconductor layer and the second n+-type semiconductor layer disposed underneath the island-shaped semiconductor layer, and the second gate dielectric film is a dielectric film allowing a pMOS transistor to function as an enhancement type, wherein the pMOS transistor comprises the gate electrode, the second gate dielectric film surrounding the periphery of the gate electrode, the tubular semiconductor layer surrounding the periphery of the second gate dielectric film, the first p+-type semiconductor layer disposed on top of the tubular semiconductor

layer and the second p+-type semiconductor layer disposed underneath the tubular semiconductor layer. Further, the gate electrode is made of a material allowing each of the nMOS transistor and the pMOS transistor to function as an enhancement type. This makes it possible to form each of the nMOS transistor and the pMOS transistor as an enhancement type.

[0035]

The method according to the fifth aspect of the present invention comprises the step of implanting arsenic into a p-type or non-doped silicon layer formed on an oxide film, to form the third n+-type silicon layer. This makes it possible to form the third n+-type silicon layer.

[0036]

In a preferred embodiment of the present invention, the method further comprises the steps of: forming a resist for forming the n-type silicon layer, on the p-type or non-doped silicon layer; implanting phosphorus into the p-type or non-doped silicon layer to form the n-type silicon layer in a part of the p-type or non-doped silicon layer; stripping away the resist; and subjecting the silicon layers to a heat treatment. This makes it possible to form the n-type silicon layer.

[0037]

In a preferred embodiment of the present invention, the method further comprises the steps of: depositing an oxide film on the p-type or non-doped silicon layer or on the p-type or non-doped silicon layer and the n-type silicon layer; depositing a nitride film on the oxide film; forming a resist for forming the island-shaped silicon layer; etching the nitride film and the oxide film to form a nitride film-based hard mask for forming the island-shaped silicon layer; stripping away the resist; depositing an oxide film; etching the oxide film to form an oxide film-based sidewall which defines a position of a gate-forming region to be subsequently formed; depositing an nitride film; and etching the nitride film to form a nitride film-based sidewall which defines a position of the tubular silicon layer to be subsequently formed. This makes it possible to form a hard mask for forming the island-shaped silicon layer and a hard mask for forming the tubular silicon layer.

[0038]

In a preferred embodiment of the present invention, the method further comprises the steps of: after the step of etching the nitride film, forming a resist for forming an output terminal region; etching the n-type or non-doped silicon layer to form an output terminal region; stripping away the resist; etching away the oxide film-based sidewall; and etching the p-type or non-doped silicon layer and the n-type or non-doped silicon layer to form the island-shaped silicon layer and the tubular silicon layer. This makes it possible to form the output terminal region, the island-shaped silicon layer and the tubular silicon layer.

[0039]

In a preferred embodiment of the present invention, the method further comprises the steps of: after the step of etching the p-type or non-doped silicon layer and the n-type or non-doped silicon layer, stripping away the nitride film, the nitride film-based sidewall and the oxide film; depositing an oxide film; etching the oxide film to form an oxide film-based sidewall for protecting a channel during ion implantation in a subsequent step; forming a resist for forming the first n+-type silicon layer and the second n+-type silicon layer; implanting arsenic into the island-shaped silicon layer to form the first n+-type silicon layer and the second n+-type silicon layer; stripping away the resist; forming a resist for forming the first p+-type silicon layer and the second p+-type silicon layer; implanting boron into the tubular silicon layer to form the first p+-type silicon layer and the second p+-type silicon layer; stripping away the resist; and subjecting the first and second n+-type silicon layers and the first and second p+-type silicon layers to a heat treatment. This makes it possible to form the first n+-type silicon layer, the second n+-type silicon layer, the first p+-type silicon layer and the second p+-type silicon layer.

[0040]

In a preferred embodiment of the present invention, the method further comprises the steps of: after the step of subjecting the first and second n+-type silicon layers and the first and second p+-type silicon layers to a heat treatment, depositing an oxide film and then flattening and etching-back the oxide film to expose the first n+-type silicon layer and the first p+-type silicon layer; forming a resist for etching the oxide film in the gate-forming region; etching the oxide film in the gate-forming region; stripping away the resist; depositing a high-k film comprising a hafnium oxide film to be formed as the first and

second gate dielectric films; depositing a metal film comprising a titanium nitride film or a tantalum nitride film to be formed as the gate electrode, and then flattening the metal film; depositing a nitride film; forming a resist for forming a gate pad; etching the nitride film; stripping away the resist; etching the metal film to form the gate electrode; depositing a nitride film; etching the nitride film to form a nitride film-based sidewall; and etching the high-k film to form the first and second gate dielectric films. This makes it possible to form the first and second gate dielectric films and the gate electrode.

[0041]

In a preferred embodiment of the present invention, the method further comprises the steps of: after the step of etching the nitride film, forming a resist for etching the oxide film; dry-etching the oxide film; stripping away the resist; wet-etching the oxide film to expose the second p+-type silicon layer; depositing a nitride film; etching the nitride film to form a nitride film-based sidewall; wet-etching the oxide film to expose the third n+-type silicon layer; and depositing a metal comprising nickel or cobalt and then subjecting the metal film to a heat treatment, whereafter an unreacted metal film is removed, whereby the first silicon-metal compound layer, the second silicon-metal compound layer, and the third silicon-metal compound layer, are formed, respectively, in a part of sidewalls of the second p+-type silicon layer and the third n+-type silicon layer, an upper portion of the first n+-type silicon layer, and an upper portion of the first p+-type silicon layer. This makes it possible to form the first silicon-metal compound layer, the second silicon-metal compound layer, and the third silicon-metal compound layer, are formed, respectively, in a part of the sidewalls of the second p+-type silicon layer and the third n+-type silicon layer, the upper portion of the first n+-type silicon layer, and the upper portion of the first p+-type silicon layer.

[0042]

In a preferred embodiment of the present invention, the method further comprises the steps of: after the step of depositing a metal, forming an oxide film as an interlayer film; forming a first contact hole, a second contact hole and a third contact hole on the second silicon-metal compound layer, the third silicon-metal compound layer and the gate electrode, respectively; forming a fourth contact hole to expose the first silicon-metal

compound layer; depositing a metal comprising tungsten to form four contacts; and forming an input terminal, an output terminal, a Vss power supply line and a Vdd power supply line. This makes it possible to form the four contacts, the input terminal, the output terminal, the Vss power supply line and the Vdd power supply line.

BRIEF DESCRIPTION OF THE DRAWINGS

[0043]

FIG. 1 is a circuit diagram showing an inverter.

FIGS. 2(a) to 2(c) show a structure of a semiconductor device according to one embodiment of the present invention, wherein FIG. 2(a), FIG. 2(b) and FIG. 2(c) are a top plan view of the semiconductor device, a sectional view taken along the line X-X' in FIG. 2(a), and a sectional view taken along the line Y-Y' in FIG. 2(a).

FIG. 3 is a sectional top plan view taken at the position Z in FIG. 2(b).

FIGS. 4(a) to 4(c) show a step in one example of a production method for the semiconductor device according to the embodiment, wherein FIG. 4(a), FIG. 4(b) and FIG. 4(c) are a top plan view, a sectional view taken along the line X-X' in FIG. 2(a), and a sectional view taken along the line Y-Y' in FIG. 2(a).

FIGS. 5(a) to 5(c) show a step in the example of the production method for the semiconductor device according to the embodiment, wherein FIG. 5(a), FIG. 5(b) and FIG. 5(c) are a top plan view, a sectional view taken along the line X-X' in FIG. 5(a), and a sectional view taken along the line Y-Y' in FIG. 5(a).

FIGS. 6(a) to 6(c) show a step in the example of the production method for the semiconductor device according to the embodiment, wherein FIG. 6(a), FIG. 6(b) and FIG. 6(c) are a top plan view, a sectional view taken along the line X-X' in FIG. 6(a), and a sectional view taken along the line Y-Y' in FIG. 6(a).

FIGS. 7(a) to 7(c) show a step in the example of the production method for the semiconductor device according to the embodiment, wherein FIG. 7(a), FIG. 7(b) and FIG. 7(c) are a top plan view, a sectional view taken along the line X-X' in FIG. 7(a), and a sectional view taken along the line Y-Y' in FIG. 7(a).

FIGS. 8(a) to 8(c) show a step in the example of the production method for the

semiconductor device according to the embodiment, wherein FIG. 8(a), FIG. 8(b) and FIG. 8(c) are a top plan view, a sectional view taken along the line X-X' in FIG. 8(a), and a sectional view taken along the line Y-Y' in FIG. 8(a).

FIGS. 9(a) to 9(c) show a step in the example of the production method for the semiconductor device according to the embodiment, wherein FIG. 9(a), FIG. 9(b) and FIG. 9(c) are a top plan view, a sectional view taken along the line X-X' in FIG. 9(a), and a sectional view taken along the line Y-Y' in FIG. 9(a).

FIGS. 10(a) to 10(c) show a step in the example of the production method for the semiconductor device according to the embodiment, wherein FIG. 10(a), FIG. 10(b) and FIG. 10(c) are a top plan view, a sectional view taken along the line X-X' in FIG. 10(a), and a sectional view taken along the line Y-Y' in FIG. 10(a).

FIGS. 11(a) to 11(c) show a step in the example of the production method for the semiconductor device according to the embodiment, wherein FIG. 11(a), FIG. 11(b) and FIG. 11(c) are a top plan view, a sectional view taken along the line X-X' in FIG. 11(a), and a sectional view taken along the line Y-Y' in FIG. 11(a).

FIGS. 12(a) to 12(c) show a step in the example of the production method for the semiconductor device according to the embodiment, wherein FIG. 12(a), FIG. 12(b) and FIG. 12(c) are a top plan view, a sectional view taken along the line X-X' in FIG. 12(a), and a sectional view taken along the line Y-Y' in FIG. 12(a).

FIGS. 13(a) to 13(c) show a step in the example of the production method for the semiconductor device according to the embodiment, wherein FIG. 13(a), FIG. 13(b) and FIG. 13(c) are a top plan view, a sectional view taken along the line X-X' in FIG. 13(a), and a sectional view taken along the line Y-Y' in FIG. 13(a).

FIGS. 14(a) to 14(c) show a step in the example of the production method for the semiconductor device according to the embodiment, wherein FIG. 14(a), FIG. 14(b) and FIG. 14(c) are a top plan view, a sectional view taken along the line X-X' in FIG. 14(a), and a sectional view taken along the line Y-Y' in FIG. 14(a).

FIGS. 15(a) to 15(c) show a step in the example of the production method for the semiconductor device according to the embodiment, wherein FIG. 15(a), FIG. 15(b) and FIG. 15(c) are a top plan view, a sectional view taken along the line X-X' in FIG. 15(a), and

a sectional view taken along the line Y-Y' in FIG. 15(a).

FIGS. 16(a) to 16(c) show a step in the example of the production method for the semiconductor device according to the embodiment, wherein FIG. 16(a), FIG. 16(b) and FIG. 16(c) are a top plan view, a sectional view taken along the line X-X' in FIG. 16(a), and a sectional view taken along the line Y-Y' in FIG. 16(a).

FIGS. 17(a) to 17(c) show a step in the example of the production method for the semiconductor device according to the embodiment, wherein FIG. 17(a), FIG. 17(b) and FIG. 17(c) are a top plan view, a sectional view taken along the line X-X' in FIG. 17(a), and a sectional view taken along the line Y-Y' in FIG. 17(a).

FIGS. 18(a) to 18(c) show a step in the example of the production method for the semiconductor device according to the embodiment, wherein FIG. 18(a), FIG. 18(b) and FIG. 18(c) are a top plan view, a sectional view taken along the line X-X' in FIG. 18(a), and a sectional view taken along the line Y-Y' in FIG. 18(a).

FIGS. 19(a) to 19(c) show a step in the example of the production method for the semiconductor device according to the embodiment, wherein FIG. 19(a), FIG. 19(b) and FIG. 19(c) are a top plan view, a sectional view taken along the line X-X' in FIG. 19(a), and a sectional view taken along the line Y-Y' in FIG. 19(a).

FIGS. 20(a) to 20(c) show a step in the example of the production method for the semiconductor device according to the embodiment, wherein FIG. 20(a), FIG. 20(b) and FIG. 20(c) are a top plan view, a sectional view taken along the line X-X' in FIG. 20(a), and a sectional view taken along the line Y-Y' in FIG. 20(a).

FIGS. 21(a) to 21(c) show a step in the example of the production method for the semiconductor device according to the embodiment, wherein FIG. 21(a), FIG. 21(b) and FIG. 21(c) are a top plan view, a sectional view taken along the line X-X' in FIG. 21(a), and a sectional view taken along the line Y-Y' in FIG. 21(a).

FIGS. 22(a) to 22(c) show a step in the example of the production method for the semiconductor device according to the embodiment, wherein FIG. 22(a), FIG. 22(b) and FIG. 22(c) are a top plan view, a sectional view taken along the line X-X' in FIG. 22(a), and a sectional view taken along the line Y-Y' in FIG. 22(a).

FIGS. 23(a) to 23(c) show a step in the example of the production method for the

semiconductor device according to the embodiment, wherein FIG. 23(a), FIG. 23(b) and FIG. 23(c) are a top plan view, a sectional view taken along the line X-X' in FIG. 23(a), and a sectional view taken along the line Y-Y' in FIG. 23(a).

FIGS. 24(a) to 24(c) show a step in the example of the production method for the semiconductor device according to the embodiment, wherein FIG. 24(a), FIG. 24(b) and FIG. 24(c) are a top plan view, a sectional view taken along the line X-X' in FIG. 24(a), and a sectional view taken along the line Y-Y' in FIG. 24(a).

FIGS. 25(a) to 25(c) show a step in the example of the production method for the semiconductor device according to the embodiment, wherein FIG. 25(a), FIG. 25(b) and FIG. 25(c) are a top plan view, a sectional view taken along the line X-X' in FIG. 25(a), and a sectional view taken along the line Y-Y' in FIG. 25(a).

FIGS. 26(a) to 26(c) show a step in the example of the production method for the semiconductor device according to the embodiment, wherein FIG. 26(a), FIG. 26(b) and FIG. 26(c) are a top plan view, a sectional view taken along the line X-X' in FIG. 26(a), and a sectional view taken along the line Y-Y' in FIG. 26(a).

FIGS. 27(a) to 27(c) show a step in the example of the production method for the semiconductor device according to the embodiment, wherein FIG. 27(a), FIG. 27(b) and FIG. 27(c) are a top plan view, a sectional view taken along the line X-X' in FIG. 27(a), and a sectional view taken along the line Y-Y' in FIG. 27(a).

FIGS. 28(a) to 28(c) show a step in the example of the production method for the semiconductor device according to the embodiment, wherein FIG. 28(a), FIG. 28(b) and FIG. 28(c) are a top plan view, a sectional view taken along the line X-X' in FIG. 28(a), and a sectional view taken along the line Y-Y' in FIG. 28(a).

FIGS. 29(a) to 29(c) show a step in the example of the production method for the semiconductor device according to the embodiment, wherein FIG. 29(a), FIG. 29(b) and FIG. 29(c) are a top plan view, a sectional view taken along the line X-X' in FIG. 29(a), and a sectional view taken along the line Y-Y' in FIG. 29(a).

FIGS. 30(a) to 30(c) show a step in the example of the production method for the semiconductor device according to the embodiment, wherein FIG. 30(a), FIG. 30(b) and FIG. 30(c) are a top plan view, a sectional view taken along the line X-X' in FIG. 30(a), and

a sectional view taken along the line Y-Y' in FIG. 30(a).

FIGS. 31(a) to 31(c) show a step in the example of the production method for the semiconductor device according to the embodiment, wherein FIG. 31(a), FIG. 31(b) and FIG. 31(c) are a top plan view, a sectional view taken along the line X-X' in FIG. 31(a), and a sectional view taken along the line Y-Y' in FIG. 31(a).

FIGS. 32(a) to 32(c) show a step in the example of the production method for the semiconductor device according to the embodiment, wherein FIG. 32(a), FIG. 32(b) and FIG. 32(c) are a top plan view, a sectional view taken along the line X-X' in FIG. 32(a), and a sectional view taken along the line Y-Y' in FIG. 32(a).

FIGS. 33(a) to 33(c) show a step in the example of the production method for the semiconductor device according to the embodiment, wherein FIG. 33(a), FIG. 33(b) and FIG. 33(c) are a top plan view, a sectional view taken along the line X-X' in FIG. 33(a), and a sectional view taken along the line Y-Y' in FIG. 33(a).

FIGS. 34(a) to 34(c) show a step in the example of the production method for the semiconductor device according to the embodiment, wherein FIG. 34(a), FIG. 34(b) and FIG. 34(c) are a top plan view, a sectional view taken along the line X-X' in FIG. 34(a), and a sectional view taken along the line Y-Y' in FIG. 34(a).

FIGS. 35(a) to 35(c) show a step in the example of the production method for the semiconductor device according to the embodiment, wherein FIG. 35(a), FIG. 35(b) and FIG. 35(c) are a top plan view, a sectional view taken along the line X-X' in FIG. 35(a), and a sectional view taken along the line Y-Y' in FIG. 35(a).

FIGS. 36(a) to 36(c) show a step in the example of the production method for the semiconductor device according to the embodiment, wherein FIG. 36(a), FIG. 36(b) and FIG. 36(c) are a top plan view, a sectional view taken along the line X-X' in FIG. 36(a), and a sectional view taken along the line Y-Y' in FIG. 36(a).

FIGS. 37(a) to 37(c) show a step in the example of the production method for the semiconductor device according to the embodiment, wherein FIG. 37(a), FIG. 37(b) and FIG. 37(c) are a top plan view, a sectional view taken along the line X-X' in FIG. 37(a), and a sectional view taken along the line Y-Y' in FIG. 37(a).

FIGS. 38(a) to 38(c) show a step in the example of the production method for the

semiconductor device according to the embodiment, wherein FIG. 38(a), FIG. 38(b) and FIG. 38(c) are a top plan view, a sectional view taken along the line X-X' in FIG. 38(a), and a sectional view taken along the line Y-Y' in FIG. 38(a).

FIGS. 39(a) to 39(c) show a step in the example of the production method for the semiconductor device according to the embodiment, wherein FIG. 39(a), FIG. 39(b) and FIG. 39(c) are a top plan view, a sectional view taken along the line X-X' in FIG. 39(a), and a sectional view taken along the line Y-Y' in FIG. 39(a).

FIGS. 40(a) to 40(c) show a step in the example of the production method for the semiconductor device according to the embodiment, wherein FIG. 40(a), FIG. 40(b) and FIG. 40(c) are a top plan view, a sectional view taken along the line X-X' in FIG. 40(a), and a sectional view taken along the line Y-Y' in FIG. 40(a).

FIGS. 41(a) to 41(c) show a step in the example of the production method for the semiconductor device according to the embodiment, wherein FIG. 41(a), FIG. 41(b) and FIG. 41(c) are a top plan view, a sectional view taken along the line X-X' in FIG. 41(a), and a sectional view taken along the line Y-Y' in FIG. 41(a).

FIGS. 42(a) to 42(c) show a step in the example of the production method for the semiconductor device according to the embodiment, wherein FIG. 42(a), FIG. 42(b) and FIG. 42(c) are a top plan view, a sectional view taken along the line X-X' in FIG. 42(a), and a sectional view taken along the line Y-Y' in FIG. 42(a).

FIGS. 43(a) to 43(c) show a step in the example of the production method for the semiconductor device according to the embodiment, wherein FIG. 43(a), FIG. 43(b) and FIG. 43(c) are a top plan view, a sectional view taken along the line X-X' in FIG. 43(a), and a sectional view taken along the line Y-Y' in FIG. 43(a).

FIGS. 44(a) to 44(c) show a step in the example of the production method for the semiconductor device according to the embodiment, wherein FIG. 44(a), FIG. 44(b) and FIG. 44(c) are a top plan view, a sectional view taken along the line X-X' in FIG. 44(a), and a sectional view taken along the line Y-Y' in FIG. 44(a).

FIGS. 45(a) to 45(c) show a step in the example of the production method for the semiconductor device according to the embodiment, wherein FIG. 45(a), FIG. 45(b) and FIG. 45(c) are a top plan view, a sectional view taken along the line X-X' in FIG. 45(a), and

a sectional view taken along the line Y-Y' in FIG. 45(a).

FIGS. 46(a) to 46(c) show a step in the example of the production method for the semiconductor device according to the embodiment, wherein FIG. 46(a), FIG. 46(b) and FIG. 46(c) are a top plan view, a sectional view taken along the line X-X' in FIG. 46(a), and a sectional view taken along the line Y-Y' in FIG. 46(a).

FIGS. 47(a) to 47(c) show a step in the example of the production method for the semiconductor device according to the embodiment, wherein FIG. 47(a), FIG. 47(b) and FIG. 47(c) are a top plan view, a sectional view taken along the line X-X' in FIG. 47(a), and a sectional view taken along the line Y-Y' in FIG. 47(a).

FIGS. 48(a) to 48(c) show a step in the example of the production method for the semiconductor device according to the embodiment, wherein FIG. 48(a), FIG. 48(b) and FIG. 48(c) are a top plan view, a sectional view taken along the line X-X' in FIG. 48(a), and a sectional view taken along the line Y-Y' in FIG. 48(a).

FIGS. 49(a) to 49(c) show a step in the example of the production method for the semiconductor device according to the embodiment, wherein FIG. 49(a), FIG. 49(b) and FIG. 49(c) are a top plan view, a sectional view taken along the line X-X' in FIG. 49(a), and a sectional view taken along the line Y-Y' in FIG. 49(a).

FIGS. 50(a) to 50(c) show a step in the example of the production method for the semiconductor device according to the embodiment, wherein FIG. 50(a), FIG. 50(b) and FIG. 50(c) are a top plan view, a sectional view taken along the line X-X' in FIG. 50(a), and a sectional view taken along the line Y-Y' in FIG. 50(a).

FIGS. 51(a) to 51(c) show a step in the example of the production method for the semiconductor device according to the embodiment, wherein FIG. 51(a), FIG. 51(b) and FIG. 51(c) are a top plan view, a sectional view taken along the line X-X' in FIG. 51(a), and a sectional view taken along the line Y-Y' in FIG. 51(a).

FIGS. 52(a) to 52(c) show a step in the example of the production method for the semiconductor device according to the embodiment, wherein FIG. 52(a), FIG. 52(b) and FIG. 52(c) are a top plan view, a sectional view taken along the line X-X' in FIG. 52(a), and a sectional view taken along the line Y-Y' in FIG. 52(a).

FIGS. 53(a) to 53(c) show a step in the example of the production method for the

semiconductor device according to the embodiment, wherein FIG. 53(a), FIG. 53(b) and FIG. 53(c) are a top plan view, a sectional view taken along the line X-X' in FIG. 53(a), and a sectional view taken along the line Y-Y' in FIG. 53(a).

FIGS. 54(a) to 54(c) show a step in the example of the production method for the semiconductor device according to the embodiment, wherein FIG. 54(a), FIG. 54(b) and FIG. 54(c) are a top plan view, a sectional view taken along the line X-X' in FIG. 54(a), and a sectional view taken along the line Y-Y' in FIG. 54(a).

FIGS. 55(a) to 55(c) show a step in the example of the production method for the semiconductor device according to the embodiment, wherein FIG. 55(a), FIG. 55(b) and FIG. 55(c) are a top plan view, a sectional view taken along the line X-X' in FIG. 55(a), and a sectional view taken along the line Y-Y' in FIG. 55(a).

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0044]

FIGS. 2(a), 2(b), 2(c) and 3 show a structure of a semiconductor device according to one embodiment of the present invention, wherein FIG. 2(a), FIG. 2(b), FIG. 2(c) and FIG. 3 are a top plan view of the semiconductor device, a sectional view taken along the line X-X' in FIG. 2(a), a sectional view taken along the line Y-Y' in FIG. 2(a), and a sectional top plan view taken at the position Z in FIG. 2(b).

[0045]

The semiconductor device according to this embodiment comprises: an island-shaped silicon layer 104; a first gate dielectric film 105 surrounding a periphery of the island-shaped silicon layer 104; a gate electrode 106 surrounding a periphery of the first gate dielectric film 105; a second gate dielectric film 105 surrounding a periphery of the gate electrode 106; a tubular silicon layer 107 surrounding a periphery of the second gate dielectric film 105; a first n+-type silicon layer 121 disposed on top of the island-shaped silicon layer 104; a second n+-type silicon layer 103 disposed underneath the island-shaped silicon layer 104; a first p+-type silicon layer 108 disposed on top of the tubular silicon layer 107; a second p+-type silicon layer 109 disposed underneath the tubular silicon layer 107; a third n+-type silicon layer 102 disposed underneath the second n+-type silicon layer

103 and the second p+-type silicon layer 109; a first silicon-metal compound layer 110 formed in a part of sidewalls of the second p+-type silicon layer 109 and the third n+-type silicon layer 102; a second silicon-metal compound layer 112 formed in an upper portion of the first n+-type silicon layer 121; and a third silicon-metal compound layer 111 formed in an upper portion of the first p+-type silicon layer 108.

[0046]

A combination of the island-shaped silicon layer 104, the first gate dielectric film 105 surrounding the periphery of the island-shaped silicon layer 104, the gate electrode 106 surrounding the periphery of the first gate dielectric film 105, the first n+-type silicon layer 121 disposed on top of the island-shaped silicon layer 104 and the second n+-type silicon layer 103 disposed underneath the island-shaped silicon layer 104, forms an nMOS SGT 129. Further, a combination of the gate electrode 106, the second gate dielectric film 105 surrounding the periphery of the gate electrode 106, the tubular silicon layer 107 surrounding the periphery of the second gate dielectric film 105, the first p+-type silicon layer 108 disposed on top of the tubular silicon layer 107 and the second p+-type silicon layer 109 disposed underneath the tubular silicon layer 107 forms a pMOS transistor.

[0047]

A contact 122 is formed to be connected to the gate electrode 106, and an input terminal 123 is formed to be connected to the contact 122. A contact 124 is formed to be connected to the first silicon-metal compound layer 110, and an output terminal 125 is formed to be connected to the contact 124. A contact 113 is formed to be connected to the second silicon-metal compound layer 112, and a Vss power supply line 116 is formed to be connected to the contact 113. A contact 114 is formed to be connected to the third silicon-metal compound layer 111, and a Vdd power supply line 117 is formed to be connected to the contact 114. An oxide film 118 is formed as an interlayer film.

[0048]

The semiconductor device may be designed to satisfy the following relation: $Wp \approx 2Wn$, wherein Wp is an inner circumferential length of the tubular silicon layer 107, and Wn is an outer circumferential length of the island-shaped silicon layer 104. In this case, the pMOS transistor can have a gate width which is two times greater than that of the

nMOS transistor. Alternatively, the semiconductor device may be designed to satisfy the following relation: $Rp \approx 2Rn$, wherein Rp is an inner radius of the tubular silicon layer 107, and Rn is a radius of the island-shaped silicon layer 104. In this case, the pMOS transistor can also have a gate width which is two times greater than that of the nMOS transistor. In these cases, the semiconductor device is preferably designed to satisfy the following relation: $Lp \approx Ln$, wherein Lp is a channel length of the tubular silicon layer, and Ln is a channel length of the island-shaped silicon layer.

[0049]

With reference to FIGS. 4(a) to 55(c), one example of a production process for forming the structure of the semiconductor device according to this embodiment will be described below. In FIGS. 4(a) to 55(c), the same elements or components are defined by a common reference numeral or code. FIGS. 4(a), 4(b) and 4(c) to FIGS. 5(a), 5(b) and 5(c) show respective steps of the production process, wherein the figure suffixed with (a) is a top plan view, and the figure suffixed with (b) and the figure suffixed with (c) are, respectively, a sectional view taken along the line X-X' in the figure suffixed with (a) and a sectional view taken along the line Y-Y' in the figure suffixed with (a).

[0050]

Referring to FIGS. 4(a) to 4(c), arsenic (As) is implanted into a p-type or non-doped silicon layer 104 formed on an oxide layer 101 to form a third n+-type silicon layer 102 therein.

[0051]

Referring to FIGS. 5(a) to 5(c), a resist 201 for forming an n-type silicon layer is formed. In cases where an after-mentioned non-doped silicon layer 107 is used, this step is unnecessary.

[0052]

Referring to FIGS. 6(a) to 6(c), phosphorus (P) is implanted into the p-type or non-doped silicon layer 104 to form an n-type silicon layer 107. In cases where a non-doped silicon layer 107 is used, this step is unnecessary.

[0053]

Referring to FIGS. 7(a) to 7(c), the resist 201 is stripped away, and then the silicon

layers 104, 107 are subjected to a heat treatment. In cases where the non-doped silicon layer 107 is used, this step is unnecessary.

[0054]

Referring to FIGS. 8(a) to 8(c), an oxide film 202 is deposited, and then a nitride film 203 is deposited.

[0055]

Referring to FIGS. 9(a) to 9(c), a resist 204 for forming an island-shaped silicon layer is formed.

[0056]

Referring to FIGS. 10(a) to 10(c), the nitride film 203 and the oxide film 202 are etched.

[0057]

Referring to FIGS. 11(a) to 11(c), the resist 204 is stripped away.

[0058]

Referring to FIGS. 12(a) to 12(c), an oxide film 205 is deposited. Preferably, in this step, a film thickness of the oxide film 205 is set such that an oxide film-based sidewall to be formed by etching back the oxide film 205 in a next step has a width equal to a radius of the nitride film 205.

[0059]

Referring to FIGS. 13(a) to 13(c), the oxide film 205 is etched to form an oxide film-based sidewall. This oxide film-based sidewall defines a position of a gate-forming region to be formed in a subsequent step.

[0060]

Referring to FIGS. 14(a) to 14(c), a nitride film 206 is deposited. Preferably, in this step, a film thickness of the nitride film 206 is set such that a nitride film-based sidewall to be formed by etching back the nitride film 206 in a next step has a width equal to a desired thickness of an after-mentioned tubular silicon layer.

[0061]

Referring to FIGS. 15(a) to 15(c), the nitride film 206 is etched to form a nitride film-based sidewall. This nitride film-based sidewall defines a position of the tubular

silicon layer to be formed in a subsequent step.

[0062]

Referring to FIGS. 16(a) to 16(c), a resist 207 for forming an output terminal region is formed.

[0063]

Referring to FIGS. 17(a) to 17(c), the n-type or non-doped silicon layer 107 is etched to form an output terminal region.

[0064]

Referring to FIGS. 18(a) to 18(c), the resist 207 is stripped away.

[0065]

Referring to FIGS. 19(a) to 19(c), the oxide film-based sidewall 205 is etched away.

[0066]

Referring to FIGS. 20(a) to 20(c), the p-type or non-doped silicon layer 104 and the n-type or non-doped silicon layer 107 are etched to form an island-shaped silicon layer 104 and a tubular silicon layer 107.

[0067]

Referring to FIGS. 21(a) to 21(c), the nitride film 203, the nitride film-based sidewall 206 and the oxide film 202 are stripped away.

[0068]

Referring to FIGS. 22(a) to 22(c), an oxide film 208 is deposited.

[0069]

Referring to FIGS. 23(a) to 23(c), the oxide film 208 is etched to form oxide film-based sidewalls 126, 210, 209, 211 for protecting channels during ion implantation in a subsequent step.

[0070]

Referring to FIGS. 24(a) to 24(c), a resist 212 for forming first and second n+-type silicon layers is formed.

[0071]

Referring to FIGS. 25(a) to 25(c), arsenic (As) is implanted into the island-shaped silicon layer 104 to form a first n+-type silicon layer 121 and a second n+-type silicon

layer 103 in an upper portion and a lower portion thereof, respectively.

[0072]

Referring to FIGS. 26(a) to 26(c), the resist 212 is stripped away.

[0073]

Referring to FIGS. 27(a) to 27(c), a resist 213 for forming first and second p+-type silicon layers is formed.

[0074]

Referring to FIGS. 28(a) to 28(c), boron (B) is implanted into the tubular silicon layer 107 to form a first p+-type silicon layer 108 and a second p+-type silicon layer 109 in an upper portion and a lower portion thereof, respectively.

[0075]

Referring to FIGS. 29(a) to 29(c), the resist 213 is stripped away, and then a heat treatment is performed.

[0076]

Referring to FIGS. 30(a) to 30(c), an oxide film is deposited, and then subjected to flattening and etching-back to expose the first n+-type silicon layer 121 and the first p+-type silicon layer 108. During this step, an oxide film 119 is formed on an inward side of the tubular silicon layer (i.e., in a gate-forming region).

[0077]

Referring to FIGS. 31(a) to 31(c), a resist 214 for etching the oxide film in the gate-forming region is formed.

[0078]

Referring to FIGS. 32(a) to 32(c), the oxide film 119 in the gate-forming region is etched.

[0079]

Referring to FIGS. 33(a) to 33(c), the resist 214 is stripped away.

[0080]

Referring to FIGS. 34(a) to 34(c), a high-k (high-dielectric constant) film 105, such as a hafnium oxide film, to be formed as first and second gate dielectric films, is deposited. Subsequently, a metal film 106, such as a titanium nitride film or a tantalum nitride film, to

be formed as a gate electrode, is deposited and then flattened.

[0081]

Referring to FIGS. 35(a) to 35(c), a nitride film 128 is deposited.

[0082]

Referring to FIGS. 36(a) to 36(c), a resist 215 for forming a gate pad is formed.

[0083]

Referring to FIGS. 37(a) to 37(c), the nitride film 128 is etched.

[0084]

Referring to FIGS. 38(a) to 38(c), the resist 215 is stripped away.

[0085]

Referring to FIGS. 39(a) to 39(c), the metal film is etched to form a gate electrode 106.

[0086]

Referring to FIGS. 40(a) to 40(c), a nitride film 115 is deposited.

[0087]

Referring to FIGS. 41(a) to 41(c), the nitride film 115 is etched to form a nitride film-based sidewall 115.

[0088]

Referring to FIGS. 42(a) to 42(c), the high-k film is etched to form first and second gate dielectric films 105.

[0089]

Referring to FIGS. 43(a) to 43(c), a resist 216 for etching the oxide film 127 is formed.

[0090]

Referring to FIGS. 44(a) to 44(c), the oxide film 127 is dry-etched.

[0091]

Referring to FIGS. 45(a) to 45(c), the resist 216 is stripped away.

[0092]

Referring to FIGS. 46(a) to 46(c), the oxide film 127 is wet-etched to expose the second p+-type silicon layer 109.

[0093]

Referring to FIGS. 47(a) to 47(c), a nitride film 120 is deposited.

[0094]

Referring to FIGS. 48(a) to 48(c), the nitride film 120 is etched to form a nitride film-based sidewall.

[0095]

Referring to FIGS. 49(a) to 49(c), the oxide film 127 is wet-etched to expose the third n+-type silicon layer 102.

[0096]

Referring to FIGS. 50(a) to 50(c), a metal, such as nickel (Ni) or cobalt (Co), is deposited. Subsequently, the metal film is subjected to a heat treatment, and then an unreacted metal film is removed, so that a first silicon-metal compound layer 110, a second silicon-metal compound layer 112, and a third silicon-metal compound layer 111, are formed, respectively, in a part of sidewalls of the second p+-type silicon layer 109 and the third n+-type silicon layer 102, an upper portion of the first n+-type silicon layer 121, and an upper portion of the first p+-type silicon layer 108.

[0097]

Referring to FIGS. 51(a) to 51(c), an oxide film 118 is formed as an interlayer film.

[0098]

Referring to FIGS. 52(a) to 52(c), a contact hole 218, a contact hole 217, and a contact hole 219, are formed, respectively, on the second silicon-metal compound layer 112, the third silicon-metal compound layer 111, and the gate electrode 106.

[0099]

Referring to FIGS. 53(a) to 53(c), a contact hole 220 is formed to expose the first silicon-metal compound layer 110.

[0100]

Referring to FIGS. 54(a) to 54(c), a metal, such as tungsten, is deposited to form four contacts 113, 114, 122, 124.

[0101]

Referring to FIGS. 55(a) to 55(c), an input terminal 123, an output terminal 125, a

Vss power supply line 116 and a Vdd power supply line 117 are formed.

EXPLANATION OF CODES

[0102]

101: oxide film

102: third n+-type silicon layer

103: second n+-type silicon layer

104: p-type or non-doped silicon layer, island-shaped silicon layer

105: gate dielectric layer

106: gate electrode

107: n-type or non-doped silicon layer, tubular silicon layer

108: first p+-type silicon layer

109: second p+-type silicon layer

110: first silicon-metal compound layer

111: third silicon-metal compound layer

112: second silicon-metal compound layer

113: contact

114: contact

115: nitride film, nitride film-based sidewall

116: Vss power supply line

117: Vdd power supply line

118: oxide film

119: oxide film

120: nitride film, nitride film-based sidewall

121: first n+-type silicon layer

122: contact

123: input terminal

124: contact

125: output terminal

126: oxide film-based sidewall

127: oxide film

128: nitride film

129: nMOS SGT

130: pMOS SGT

201: resist

202: oxide film

203: nitride film

204: resist

205: oxide film

206: nitride film

207: resist

208: oxide film

209: oxide film-based sidewall

210: oxide film-based sidewall

211: oxide film-based sidewall

212: resist

213: resist

214: resist

215: resist

216: resist

217: contact hole

218: contact hole

219: contact hole

220: contact hole

What is claimed is:

1. A semiconductor device comprising:

a first island-shaped semiconductor layer;

a first gate dielectric film located on and in contact with at least a part of a periphery of the first island-shaped semiconductor layer;

a gate electrode having one surface in contact with the first gate dielectric film;

a second gate dielectric film in contact with the other surface of the gate electrode;

a second semiconductor layer in contact with the second gate dielectric film;

a first first-conductive-type high-concentration semiconductor layer disposed on top of the first island-shaped semiconductor layer;

a second first-conductive-type high-concentration semiconductor layer disposed underneath the first island-shaped semiconductor layer;

a first second-conductive-type high-concentration semiconductor layer disposed on top of the second semiconductor layer; and

a second second-conductive-type high-concentration semiconductor layer disposed underneath the second semiconductor layer.

2. A semiconductor device comprising:

an island-shaped semiconductor layer;

a first gate dielectric film surrounding a periphery of the island-shaped semiconductor layer;

a gate electrode surrounding a periphery of the first gate dielectric film;

a second gate dielectric film surrounding a periphery of the gate electrode;

a tubular semiconductor layer surrounding a periphery of the second gate dielectric film;

a first first-conductive-type high-concentration semiconductor layer disposed on top of the island-shaped semiconductor layer;

a second first-conductive-type high-concentration semiconductor layer disposed underneath the island-shaped semiconductor layer;

a first second-conductive-type high-concentration semiconductor layer disposed on top of the tubular semiconductor layer; and

a second second-conductive-type high-concentration semiconductor layer disposed underneath the tubular semiconductor layer.

3. A semiconductor device comprising:

an island-shaped semiconductor layer;

a first gate dielectric film surrounding a periphery of the island-shaped semiconductor layer;

a gate electrode surrounding a periphery of the first gate dielectric film;

a second gate dielectric film surrounding a periphery of the gate electrode;

a tubular semiconductor layer surrounding a periphery of the second gate dielectric film;

a first first-conductive-type high-concentration semiconductor layer disposed on top of the island-shaped semiconductor layer;

a second first-conductive-type high-concentration semiconductor layer disposed underneath the island-shaped semiconductor layer;

a first second-conductive-type high-concentration semiconductor layer disposed on top of the tubular semiconductor layer;

a second second-conductive-type high-concentration semiconductor layer disposed underneath the tubular semiconductor layer;

a third first-conductive-type high-concentration semiconductor layer disposed underneath the second first-conductive-type high-concentration semiconductor layer and the second second-conductive-type high-concentration semiconductor layer;

a first semiconductor-metal compound layer formed in a part of sidewalls of the second second-conductive-type high-concentration semiconductor layer and the third first-conductive-type high-concentration semiconductor layer;

a second semiconductor-metal compound layer formed in an upper portion of the first first-conductive-type high-concentration semiconductor layer; and

a third semiconductor-metal compound layer formed in an upper portion of the first

second-conductive-type high-concentration semiconductor layer.

4. A semiconductor device comprising:

an island-shaped semiconductor layer;

a first gate dielectric film surrounding a periphery of the island-shaped semiconductor layer;

a gate electrode surrounding a periphery of the first gate dielectric film;

a second gate dielectric film surrounding a periphery of the gate electrode;

a tubular semiconductor layer surrounding a periphery of the second gate dielectric film;

a first n+-type semiconductor layer disposed on top of the island-shaped semiconductor layer;

a second n+-type semiconductor layer disposed underneath the island-shaped semiconductor layer;

a first p+-type semiconductor layer disposed on top of the tubular semiconductor layer; and

a second p+-type semiconductor layer disposed underneath the tubular semiconductor layer.

5. A semiconductor device comprising:

an island-shaped semiconductor layer;

a first gate dielectric film surrounding a periphery of the island-shaped semiconductor layer;

a gate electrode surrounding a periphery of the first gate dielectric film;

a second gate dielectric film surrounding a periphery of the gate electrode;

a tubular semiconductor layer surrounding a periphery of the second gate dielectric film;

a first n+-type semiconductor layer disposed on top of the island-shaped semiconductor layer;

a second n+-type semiconductor layer disposed underneath the island-shaped

semiconductor layer;

a first p+-type semiconductor layer disposed on top of the tubular semiconductor layer;

a second p+-type semiconductor layer disposed underneath the tubular semiconductor layer;

a third n+-type semiconductor layer disposed underneath the second n+-type semiconductor layer and the second p+-type semiconductor layer;

a first semiconductor-metal compound layer formed in a part of sidewalls of the second p+-type semiconductor layer and the third n+-type semiconductor layer;

a second semiconductor-metal compound layer formed in an upper portion of the first n+-type semiconductor layer; and

a third semiconductor-metal compound layer formed in an upper portion of the first p+-type semiconductor layer.

6. The semiconductor device as defined in claim 4, which satisfies the following relation: $Wp \approx 2Wn$, wherein Wp is an inner circumferential length of the tubular semiconductor layer, and Wn is an outer circumferential length of the island-shaped semiconductor layer.

7. The semiconductor device as defined in claim 4, which satisfies the following relation: $Rp \approx 2Rn$, wherein Rp is an inner radius of the tubular semiconductor layer, and Rn is a radius of the island-shaped semiconductor layer.

8. The semiconductor device as defined in claim 4, which satisfies the following relation: $Lp \approx Ln$, wherein Lp is a channel length of the tubular semiconductor layer, and Ln is a channel length of the island-shaped semiconductor layer.

9. The semiconductor device as defined in claim 4, wherein:

the first gate dielectric film is a dielectric film allowing an nMOS transistor to function as an enhancement type, wherein the nMOS transistor comprises the

island-shaped semiconductor layer, the first gate dielectric film surrounding the periphery of the island-shaped semiconductor layer, the gate electrode surrounding the periphery of the first gate dielectric film, the first n+-type semiconductor layer disposed on top of the island-shaped semiconductor layer and the second n+-type semiconductor layer disposed underneath the island-shaped semiconductor layer; the second gate dielectric film is a dielectric film allowing a pMOS transistor to function as an enhancement type, wherein the pMOS transistor comprises the gate electrode, the second gate dielectric film surrounding the periphery of the gate electrode, the tubular semiconductor layer surrounding the periphery of the second gate dielectric film, the first p+-type semiconductor layer disposed on top of the tubular semiconductor layer and the second p+-type semiconductor layer disposed underneath the tubular semiconductor layer; and

the gate electrode is made of a material allowing each of the nMOS transistor and the pMOS transistor to function as an enhancement type.

10. The semiconductor device as defined in claim 5, wherein each of the first to third semiconductor-metal compound layers is a silicon-metal compound layer.

11. The semiconductor device as defined in claim 4, wherein:

the island-shaped semiconductor layer is an island-shaped silicon layer;

the tubular semiconductor layer is a tubular silicon layer;

each of the first and second n+-type semiconductor layers or each of the first to third n+-type semiconductor layers is an n+-type silicon layer; and

each of the first and second p+-type semiconductor layers is a p+-type silicon layer.

12. The semiconductor device as defined in claim 11, wherein:

the island-shaped semiconductor layer is a p-type or non-doped island-shaped silicon layer; and

the tubular semiconductor layer is an n-type or non-doped tubular silicon layer.

13. A method of producing the semiconductor device as defined in claim 12, comprising

the step of implanting arsenic into a p-type or non-doped silicon layer formed on an oxide film, to form the third n+-type silicon layer.

14. The method as defined in claim 13, which further comprises the steps of: forming a resist for forming the n-type silicon layer, on the p-type or non-doped silicon layer; implanting phosphorus into the p-type or non-doped silicon layer to form the n-type silicon layer in a part of the p-type or non-doped silicon layer; stripping away the resist; and subjecting the silicon layers to a heat treatment.

15. The method as defined in claim 13, which further comprises the steps of: depositing an oxide film on the p-type or non-doped silicon layer or on the p-type or non-doped silicon layer and a n-type silicon layer; depositing a nitride film on the oxide film; forming a resist for forming the island-shaped silicon layer; etching the nitride film and the oxide film to form a nitride film-based hard mask for forming the island-shaped silicon layer; stripping away the resist; depositing an oxide film; etching the oxide film to form an oxide film-based sidewall which defines a position of a gate-forming region to be subsequently formed; depositing an nitride film; and etching the nitride film to form a nitride film-based sidewall which defines a position of the tubular silicon layer to be subsequently formed.

16. The method as defined in claim 15, which further comprises the steps of: after the step of etching the nitride film, forming a resist for forming an output terminal region; etching the n-type or non-doped silicon layer to form an output terminal region; stripping away the resist; etching away the oxide film-based sidewall; and etching the p-type or non-doped silicon layer and the n-type or non-doped silicon layer to form the island-shaped silicon layer and the tubular silicon layer.

17. The method as defined in claim 16, which further comprises the steps of: after the step of etching the p-type or non-doped silicon layer and the n-type or non-doped silicon layer, stripping away the nitride film, the nitride film-based sidewall and the oxide film; depositing an oxide film; etching the oxide film to form an oxide film-based sidewall for

protecting a channel during ion implantation in a subsequent step; forming a resist for forming the first n+-type silicon layer and the second n+-type silicon layer; implanting arsenic into the island-shaped silicon layer to form the first n+-type silicon layer and the second n+-type silicon layer; stripping away the resist; forming a resist for forming the first p+-type silicon layer and the second p+-type silicon layer; implanting boron into the tubular silicon layer to form the first p+-type silicon layer and the second p+-type silicon layer; stripping away the resist; and subjecting the first and second n+-type silicon layers and the first and second p+-type silicon layers to a heat treatment.

18. The method as defined in claim 17, which further comprises the steps of: after the step of subjecting the first and second n+-type silicon layers and the first and second p+-type silicon layers to a heat treatment, depositing an oxide film and then flattening and etching-back the oxide film to expose the first n+-type silicon layer and the first p+-type silicon layer; forming a resist for etching the oxide film in the gate-forming region; etching the oxide film in the gate-forming region; stripping away the resist; depositing a high-k film comprising a hafnium oxide film to be formed as the first and second gate dielectric films; depositing a metal film comprising a titanium nitride film or a tantalum nitride film to be formed as the gate electrode, and then flattening the metal film; depositing a nitride film; forming a resist for forming a gate pad; etching the nitride film; stripping away the resist; etching the metal film to form the gate electrode; depositing a nitride film; etching the nitride film to form a nitride film-based sidewall; and etching the high-k film to form the first and second gate dielectric films.

19. The method as defined in claim 18, which further comprises the steps of: after the step of etching the nitride film, forming a resist for etching the oxide film; dry-etching the oxide film; stripping away the resist; wet-etching the oxide film to expose the second p+-type silicon layer; depositing a nitride film; etching the nitride film to form a nitride film-based sidewall; wet-etching the oxide film to expose the third n+-type silicon layer; and depositing a metal comprising nickel or cobalt and then subjecting the metal film to a heat treatment, whereafter an unreacted metal film is removed, whereby the first silicon-metal

compound layer, the second silicon-metal compound layer, and the third silicon-metal compound layer, are formed, respectively, in a part of sidewalls of the second p+-type silicon layer and the third n+-type silicon layer, an upper portion of the first n+-type silicon layer, and an upper portion of the first p+-type silicon layer.

20. The method as defined in claim 19, which further comprises the steps of: after the step of depositing a metal, forming an oxide film as an interlayer film; forming a first contact hole, a second contact hole and a third contact hole on the second silicon-metal compound layer, the third silicon-metal compound layer and the gate electrode, respectively; forming a fourth contact hole to expose the first silicon-metal compound layer; depositing a metal comprising tungsten to form four contacts; and forming an input terminal, an output terminal, a Vss power supply line and a Vdd power supply line.