Description

Title of Invention: POWER ~~CONVERSION DEVICE~~CONVERTER

Technical Field

[0001] The present invention relates to a power converter including a power buffer circuit.

Background Art

[0002] A full-wave rectifying circuit is typically used to obtain a DC voltage from a single-phase AC voltage input from a single-phase AC power supply. Output of the full-wave rectifying circuit, however, has power pulsations having a frequency twice the frequency of the single-phase AC voltage. To reduce the power pulsations, a power buffer circuit for buffering a power is required between an output of the full-wave rectifying circuit and a load. A capacitive element, for example, referred to as a smoothing capacitor is required for buffering of a power.

[0003] Non-patent Document 1 discloses a technique for connecting a buffer capacitor to a smoothing capacitor via a current-reversible chopper to absorb a pulsating power. This technique reduces the electrostatic capacitance of the smoothing capacitor and further allows voltage ripples on a buffer side to significantly reduce the total electrostatic capacitance required for smoothing.

[0004] Non-patent Document 2 discloses a technique for connecting a buffer capacitor to a DC link via a switching element while removing the smoothing capacitor of Non-patent Document 1. A direct conversion circuit that generates a voltage source by using this technique, and generates a high-frequency link along with a power supply voltage is shown.

[0005] Non-patent Document 3 further discloses a technique for converting an input waveform into a sinusoidal waveform, and increasing efficiency.

[0009] In power conversion using the technique shown in Non-patent Document 1, a voltage of the buffer capacitor is not required to be controlled to be constant, and thus can be set to be smaller than a normal smoothing capacitor in required electrostatic capacitance, regardless of a direct conversion type or an indirect conversion type.

[0010] However, the amplitude of the pulsating power is as great as that of a constant component of a power. A value of an allowable ripple current required by the buffer capacitor is thus high. On the other hand, it is desirable to use an electrolytic capacitor as the buffer capacitor in view of device miniaturization and cost restraints. Due to the use of the electrolytic capacitor as the buffer capacitor, even the buffer capacitor has to have an electrostatic capacitance that is larger than an actually-required electrostatic capacitance and is approximately equal to the electrostatic capacitance of the normal smoothing capacitor to meet the value of the allowable ripple current.

[0011] Besides, Non-patent Document 4 shows a single-phase to three-phase direct conversion circuit not including an active power buffer circuit. The relation between an input current and output power ripples is shown herein. The need to provide a pulsating power having a frequency twice a power supply frequency to an output power is shown to convert an input waveform into a sinusoidal waveform.

[0012] In a household air conditioner of a 1.5 kW class, for example, speed ripples involved in pulsations of a load torque are expected to be suppressed to be approximately 10% by the moment of inertia of a motor. However, the stress of a compressor support system increases as a pulsating torque increases with increasing power capacity. It is therefore clear that power capacity that can be used has an upper limit.

[0013] ~~It is an object~~ Embodiments of the present application seek to make, in a power converter including an active power buffer circuit, a power buffered by the power buffer circuit smaller than a pulsating power, and to thereby reduce the electrostatic capacitance and the power

capacity of the power buffer circuit. This may leads to expansion of the range of the power capacity in a case where the load pulsates.

Means for Solving the Problems

[0014] According to an aspect of the present invention, there is provided ~~A~~a power converter according to the present invention includes: a DC link (7) that includes a first power supply line (LH) and a second power supply line (LL); a converter (3) that receives a single-phase AC voltage (Vin), and outputs a pulsating power (Pin) to the DC link; an inverter (5) that receives a power from the DC link, and outputs an AC current (Iu, Iv and Iw); and a power buffer circuit (4) that receives a charge power (Pl) from the DC link, and outputs a discharge power (Pc) to the DC link.

[0015] ~~In a first aspect of the power converter, w~~When at least the pulsating power exceeds a predetermined value, a variation (Pc – Pl) of the discharge power to the charge power is smaller than an AC component (Pin^) of the pulsating power.

[0016] ~~A second aspect of the power converter a~~According to an embodiment of the present invention ~~is the first aspect, wherein,~~ an input power (Pdc) input from the DC link (7) into the inverter (5) takes a value (Pin + Pc − Pl) obtained by subtracting the charge power from a sum of the pulsating power and the discharge power. When at least the pulsating power exceeds the predetermined value, the charge power (Pl) takes a value (k·Pin) which is a constant (k) (where the constant is a positive number less than 1/2) times the pulsating power (Pin), and the discharge power (Pc) takes a value (2k·Pin^ + Pl) obtained by adding the charge power to (−2) times the AC component (Pin^) of the pulsating power multiplied by the constant.

[0017] ~~A third aspect of the power converter a~~According to an embodiment of the present invention ~~is the second aspect, wherein,~~ the converter (3) applies a rectified voltage (Vrec) obtained by full-wave rectifying the single-phase AC voltage (Vm·sin(ωt)) to the DC link (7) so that a higher electric potential is applied to the first power supply line (LH) than the second

power supply line (LL), and allows, when at least the pulsating power exceeds the predetermined value, a current ($(1 - k)\cdot Im\cdot|\sin(\omega t)|$) obtained by multiplying a first current by a value ($1 - k$) obtained by subtracting the constant from 1 to flow through the DC link, the first current being a current ($Im\cdot|\sin(\omega t)|$) obtained by dividing the pulsating power (Pin) by the rectified voltage (Vrec). The power buffer circuit (4) includes: a discharge circuit (4a) that includes a capacitor (C4) and a first switch (Sc and D42) that is connected in series to the capacitor between the first power supply line and the second power supply line so as to be closer to the first power supply line than the capacitor is; and a charge circuit (4b) that charges the capacitor. When at least the pulsating power exceeds the predetermined value, the power buffer circuit (4) receives a charge current ($il = k\cdot Im\cdot|\sin(\omega t)|$) which is the constant times the first current, and outputs a discharge current (ic) that is a current (Pc/Vc) obtained by dividing the discharge power (Pc) by a both-end voltage (Vc) across the capacitor.

[0018] ~~A fourth aspect of the power converter a~~According to an embodiment of the present invention ~~is the second aspect, wherein,~~ the converter (3) applies a rectified voltage (Vrec) obtained by full-wave rectifying the single-phase AC voltage (Vin) to the DC link (7) so that a higher electric potential is applied to the first power supply line (LH) than the second power supply line (LL). The power buffer circuit (4) includes: a discharge circuit (4a) that includes a capacitor (C4) and a first switch (Sc and D42) that is connected in series to the capacitor between the first power supply line and the second power supply line so as to be closer to the first power supply line than the capacitor is; and a charge circuit (4b) that charges the capacitor. A rectifying duty (drec) that is a duty at which the converter is in conduction with the DC link (7) takes a value ($Vdc/Vm\cdot|\sin(\omega t)|$) obtained by dividing a product of a predetermined voltage (Vdc) and a square ($\sin^2(\omega t)$) of a sine value of a phase (ωt) of the single-phase AC voltage by the rectified voltage (Vrec). A discharge

duty (dc) that is a duty at which the capacitor discharges takes a value ($Vdc/Vc \cdot \cos^2(\omega t)$) obtained by dividing a product of the predetermined voltage and a square ($\cos^2(\omega t)$) of a cosine value of the phase by a both-end voltage (Vc) across the capacitor.

[0019] ~~A fifth aspect of the power converter a~~According to an embodiment of the present invention ~~is any one of the second to fourth aspects, wherein~~, the constant (k) is independent of the AC current (Iu, Iv and Iw).

[0020] ~~A sixth aspect of the power converter a~~According to an embodiment of the present invention ~~is any one of the second to fourth aspects, wherein~~, the constant (k) is inversely proportional to a magnitude of the AC current (Iu, Iv and Iw).

[0021] ~~In any one of the first to sixth aspects, for example,~~ According to an embodiment of the present invention, the predetermined value is set so as to be smaller than a maximum rated power of the pulsating power.

[0022] ~~Alternatively, in any one of the first to seventh aspects, for example,~~ According to an embodiment of the present invention, when the pulsating power is equal to or smaller than a predetermined value, the variation (Pc – Pl) of the discharge power to the charge power is equal to the AC component (Pin^) of the pulsating power.

[0023] ~~Alternatively, in any one of the first to eighth aspects, for example,~~ According to an embodiment of the present invention, when the pulsating power exceeds a predetermined value, the variation (Pc – Pl) of the discharge power to the charge power is independent of the pulsating power.

Effects of Invention

[0024] According to the first aspect of the power converter according to the present invention, the variation of the discharge power to the charge power, which is a power buffered by the power buffer circuit, is smaller than the AC component of the pulsating power. The power capacity of the power buffer circuit can thus be reduced compared with a conventional technique.

[0025] ~~According to the second aspect of the power converter according to the present invention, t~~The power buffered by the power buffer circuit ~~is~~ may be twice a value obtained by multiplying the AC component of the pulsating power ~~multiplied~~ by the constant. Since the constant is less than 1/2, the power buffered ~~in the first aspect is~~ may be smaller than that buffered by a conventional power buffer circuit, and ~~the second aspect~~ leads to achievement of the ~~first~~ aspect.

[0026] ~~According to the third aspect of the power converter according to the present invention, a~~ A period in which a zero-phase current flows through the inverter can be reduced to thereby increase a period in which a voltage applied to a DC link voltage is used.

[0027] The sum of the product of the rectifying duty and the rectified voltage and the product of the discharge duty and the both-end voltage corresponds to an average value of a DC voltage used by the inverter. ~~In the fourth aspect of the power converter according to the present invention, t~~The sum matches the predetermined voltage, and can be set to a constant value independently of a phase of the single-phase AC voltage.

[0028] ~~According to the fifth aspect of the power converter according to the present invention, a~~A ripple current of the capacitor can be reduced in a light-load range, and the life of the power converter can be increased.

[0029] ~~According to the sixth aspect of the power converter according to the present invention, w~~When a torque of a motor serving as the load of the power converter is small, vibrations of the motor in a low-rpm region can be reduced.

[0030] Objects, features~~, aspects~~ and advantages of the present invention will become more apparent from the following detailed description and the accompanying drawings.

Brief Description of Drawings

[0031] ~~[FIG. 1] A~~ FIG. 1 is a block diagram showing configuration of a direct power converter according to an embodiment~~.~~;

[FIG. 2] A FIG. 2 is a block diagram showing a power balance in the direct power converter according to the embodiment.;

[FIG. 3] A FIG. 3 is a graph showing the relation among an input power, the electrostatic capacitance of a capacitor, and a ripple current in the direct power converter.;

[FIG. 4] A FIG. 4 is a circuit diagram showing an equivalent circuit of a circuit shown in FIG. 1.;

[FIG. 5] A FIGS. 5 and 6 are graphs showing operation of the direct power converter according to the embodiment.;

~~[FIG. 6] A graph showing operation of the direct power converter according to the embodiment.~~

[FIG. 7] A FIG. 7 is a graph showing a virtual DC voltage.;

[FIG. 8] A FIG. 8 is a graph showing virtual operation of the direct power converter according to the embodiment.;

[FIG. 9] A FIGS. 9 and 10 are graphs showing operation of the direct power converter according to the embodiment.;

~~[FIG. 10] A graph showing operation of the direct power converter according to the embodiment.~~

[FIG. 11] A FIG. 11 is a block diagram showing an example of configuration for performing control to achieve a DC current.; and

[FIG. 12] A FIG. 12 is a circuit diagram showing a modification of the direct power converter shown in FIG. 1.

Description of Embodiment

[0032] A. Configuration of Direct Power Converter

connected in parallel to the switching elements Svp, Swp, Sun, Svn, and Swn. AC currents Iu, Iv, and Iw are respectively output from the output terminals Pu, Pv, and Pw, and constitute a three-phase AC current. IGBTs are used as the switching elements Sup, Svp, Swp, Sun, Svn, and Swn, for example.

[0045] An inductive load 6 is a rotary machine, for example, and is shown by an equivalent circuit representing an inductive load. Specifically, a reactor Lu and a resistor Ru are connected in series to each other, and one end of the series body is connected to the output terminal Pu. The same applies to a reactor Lv and a resistor Rv and to a reactor Lw and a resistor Rw. Respective opposite ends of these series bodies are connected to one another.

[0046] B. Control Method

(b-1) Basic Concept of Power Reduction

An instantaneous input power Pin input into the converter 3 is expressed by the following formula (1) with an input power factor being 1. Note that a crest value Vm and a power supply angular velocity ω of the single-phase AC voltage Vin, a crest value Im of the input current Iin, and time t are introduced. The product ωt of the power supply angular velocity ω and the time t represents a phase of the single-phase AC voltage Vin. An AC waveform is understood as the product of a sine value of the phase ωt of the AC waveform and a crest value.

[0047] ~~[Math 1]~~

$$\begin{aligned} Pin &= Vm \cdot Im \cdot \sin^2(\omega t) \\ &= \frac{1}{2} Vm \cdot Im - \frac{1}{2} Vm \cdot Im \cdot \cos(2\omega t) \quad \cdots (1) \end{aligned}$$

[0048] The instantaneous input power Pin has an AC component $(-1/2) \cdot Vm \cdot Im \cdot \cos(2\omega t)$ (hereinafter, also referred to as an "AC component Pin^") shown

[0053] Therefore, described is which technique can reduce the buffering power Pbuf to reduce the power capacity of the power buffer circuit 4.

[0054] It is of course undesirable to set the buffering power Pbuf to completely zero as a power input into the inverter 5 pulsates with the second term of the right-hand side of the formula (1), and there is no need to reduce the power capacity of the power buffer circuit 4 in the first place. The buffering power Pbuf is determined by the following formula (2) by introducing a positive constant k less than 1/2. In other words, achievement of such buffering power Pbuf leads to reduction in power capacity of the power buffer circuit.

[0055] ~~[Math 2]~~

$$Pbuf = k \cdot Vm \cdot Im \cdot \cos(2\omega t) \quad \cdots(2)$$

[0056] This means that a difference between powers provided and received between the power buffer circuit 4 and the DC power supply lines LH and LL satisfies the formula (2). In other words, if the absolute value of a power (Pc − Pl) that is a variation of the discharge power Pc to the charge power Pl is smaller than the absolute value of the AC component Pin^, the power capacity of the power buffer circuit 4 can be reduced compared with a conventional technique.

[0057] By introducing the constant k less than 1/2 as described above, the buffering power Pbuf can be selected to be small compared with the techniques disclosed in Non-patent Documents 2 and 3. This results in the following advantages of the power buffer circuit 4.

[0058] (b-2) Description of Advantages in Discharge Circuit 4a

In this section, reduction of the buffering power Pbuf allows the use of an electrolytic capacitor as the capacitor C4 and achieving the discharge circuit 4a inexpensively is described.

[0059] FIG. 3 is a graph showing the relation between the electrostatic capacitance (also simply referred to as a "capacitor capacity") (a left vertical axis) of the capacitor used or required in the direct power converter receiving and processing an input power (an average value of the instantaneous input power Pin: a horizontal axis) and a ripple current and an allowable value (a right vertical axis) of the ripple current in the capacitor.

[0060] Symbols H1 and H2 each represent the capacitor capacity used in a case where a single-phase power factor correction circuit is used. The symbols H1 and H2 respectively ~~are~~ represent data in cases of using air conditioners having air conditioning abilities of 6 kW and 11.2 kW. The power factor correction circuit can herein be understood to have configuration in which the switch Sc has been shorted and removed from the power buffer circuit 4, and a connection point of the reactor L4 and the converter 3 is not directly connected to the inverter 5. In this configuration, the diode D40 and the reactor L4 connected in series to each other are provided between the converter 3 and the inverter 5 in the DC power supply line LH, and the capacitor C4 is connected in parallel to the inverter 5 between the DC power supply lines LH and LL.

[0061] In view of the fact that Pdc = Pin − Pin^ holds when k = 1/2, the electrostatic capacitance C required for the capacitor C4 can be obtained from Non-patent Document 3 by the following formula (3). Note that a maximum value Vcmax and a minimum value Vcmin of the both-end voltage Vc are introduced.

[0062] ~~[Math 3]~~

$$C = \frac{Vm \cdot Im}{\omega(Vc\max^2 - Vc\min^2)} \quad \cdots(3)$$

[0063] On a graph G1, calculated values required for capacitor capacities when k = 1/2 (i.e., the buffering power Pbuf is equal to the absolute value of the AC component Pin^) are plotted. Note that the maximum value Vcmax = 400 + 50 = 450 (V) and the

passing through the charge circuit 4b is the charge power Pl, which corresponds to the buffering power Pbuf expressed by the formula (2) in a case where ~~this~~ the buffering power Pbuf is positive (see FIG. 2).

[0069] The power capacity required for the charge circuit 4b decreases as the buffering power Pbuf decreases. By reducing the buffering power Pbuf, a current il (this can be understood as a charge current input into the charge circuit 4b) flowing through the reactor L4 is reduced, and thus the power capacity required for the reactor L4 is also reduced.

[0070] (b-4) Specific Examples of Charge Power Pl and Discharge Power Pc

In and after this section, the above-mentioned charge power Pl and discharge power Pc are respectively determined by the formulas (4) and (5) as examples.

[0071] ~~[Math 4]~~

$$Pl = k \cdot Vm \cdot Im \cdot \sin^2(\omega t) \quad \cdots(4)$$

[0072] ~~[Math 5]~~

$$\begin{aligned} Pc &= k \cdot Vm \cdot Im \cdot \cos^2(\omega t) \\ &= k \cdot Vm \cdot Im \cdot \cos(2\omega t) + Pl \quad \cdots(5) \end{aligned}$$

[0073] This means that the charge power Pl is a power which is the constant k times the pulsating power Pin, and the discharge power Pc is a power obtained by adding the charge power Pl to (−2) times the AC component Pin^ multiplied by the constant k.

[0074] The charge power Pl can be understood as a power k·Pin distributed from the pulsating power Pin to the power buffer circuit 4 via the DC link 7 at a distribution ratio of the constant k. The constant k is thus hereinafter also referred to as a buffer distribution ratio k.

[0075] It is obvious from the formulas (4) and (5) and Pbuf = Pc − Pl that the formula (2) is satisfied.

[0076] In contrast to Patent Document 1 and Non-patent Document 2 in which the charge power Pl and the discharge power Pc are provided and received between the power buffer circuit 4 and the DC link 7 in the exclusive periods of the power supply phase, the exclusive periods of the power supply phase for ~~them~~ the charge power Pl and the discharge power Pc are not set.

[0077] However, discharge is dominant over charge in a period (hereinafter, also referred to as a "discharge dominant period") in which Pc > Pl (i.e., Pbuf > 0), and charge is dominant over discharge in a period (hereinafter, also referred to as a "charge dominant period") in which Pc < Pl (i.e., Pbuf < 0). As can be understood from the formulas (4) and (5), a period in which $(n+1/4)\pi \leq \omega t \leq (n+3/4)\pi$ is the charge dominant period, and a period in which $(n+3/4)\pi \leq \omega t \leq (n+5/4)\pi$ is the discharge dominant period (n is an integer: the same applies hereinafter).

[0078] By determining the charge power Pl and the discharge power Pc as described above, a description of the power capacity required for the charge circuit 4b can be more quantitatively than the previous section.

[0079] An average value of a power, input into a conventional power factor correction circuit, i.e., input into the reactor, per period of the power supply frequency can be obtained from the formula (6) in view of the formula (1).

[0080] ~~[Math 6]~~

$$\frac{\mathrm{Vm}\cdot\mathrm{Im}}{2\pi}\int_0^{2\pi}\frac{1}{2}(1-\cos 2\theta)\mathrm{d}\theta=\frac{\mathrm{Vm}\cdot\mathrm{Im}}{2} \quad \cdots(6)$$

[0081] On the other hand, when the power buffer circuit 4 is used, the charge power Pl is input into ~~this~~the power buffer circuit. In view of the formula (4), an average value of a power, input into the power buffer circuit 4, i.e., input into the charge circuit 4b, per period of the power supply frequency can be obtained from the formula (7).

[0082] ~~[Math 7]~~

$$\frac{Vm \cdot Im}{2\pi}\int_0^{2\pi}\left|k \cdot \sin^2 2\theta\right| d\theta = \frac{Vm \cdot Im}{2} \cdot k \quad \cdots(7)$$

[0083] As can be understood from comparison between the formulas (6) and (7), the power capacity required for the charge circuit 4b is k times compared with the power factor correction circuit. By setting the buffer distribution ratio k to less than 1/2, the power capacity required for the charge circuit 4b is reduced to be smaller than one half of the power capacity~~that~~ in the power factor correction circuit.

[0084] (b-5) Current Distribution Dependent on Constant k

In this section, a technique for setting a current irec1 flowing from the converter 3 to the inverter 5 out of a current irec output from the converter 3 dependently on the buffer distribution ratio k is described.

[0085] The rectified voltage Vrec expressed by the formula (8) is applied to an output side of the converter 3.

[0086] ~~[Math 8]~~

$$Vrec = |Vin| = Vm \cdot |\sin(\omega t)| \quad \cdots(8)$$

[0087] The following formula (9) holds as Prec = Pin − Pl.

[0088] ~~[Math 9]~~

$$Prec = (1-k) \cdot Vm \cdot Im \cdot \sin^2(\omega t) = |Vin| \cdot irec1 \quad \cdots(9)$$

[0089] The current irec1 is thus expressed by the following formula (10).

[0090] ~~[Math 10]~~

$$irec1 = (1-k) \cdot Im \cdot |\sin(\omega t)| \quad \cdots(10)$$

[0091] The formula (1) is based on the premise that the input current Iin is expressed by Im·sin(ωt), i.e., has a sinusoidal waveform, and thus the current il satisfies the following formula (11). As can be seen from FIG. 2, this is because the current irec output from the converter 3 is equal to the sum of the current irec1 and the current il.

[0092] ~~[Math 11]~~

$$il = k \cdot Im \cdot |\sin(\omega t)| \quad \cdots(11)$$

[0093] A peak value of the current il is thus k·Im. In view of the fact that the peak value of the current input into the conventional power factor correction circuit is Im, it is understood that the power capacity required for the reactor L4 is reduced compared with a conventional technique.

[0094] When a discharge current ic flowing from the capacitor C4 to the inverter 5 is introduced, the discharge power Pc output from the power buffer circuit 4 is expressed by the product Vc·ic. In order for the discharge power Pc to satisfy the formula (5), the discharge current ic thus satisfies the following formula (12).

[0095] ~~[Math 12]~~

$$ic = \frac{Pc}{Vc} = \frac{k \cdot Vm \cdot Im}{2Vc}(1 + \cos(2\omega t)) \quad \cdots(12)$$

[0096] FIG. 4 shows an equivalent circuit of the circuit shown in FIG. 1. The equivalent circuit is introduced in Patent Document 1, for example. In the equivalent circuit, the current irec1 is equivalently expressed as a current irec1 passing through a switch Srec when the switch Srec is conductive. Similarly, the discharge current ic is equivalently expressed as a current ic passing through the switch Sc when the switch Sc is conductive. A current flowing through the inverter 5 to the inductive load 6 when the output terminals Pu, Pv and Pw are connected in common to any one of the DC power supply lines LH and LL in the inverter 5 is also equivalently expressed as a zero-phase current iz flowing through a switch Sz when the switch Sz is conductive. FIG. 4 also shows the reactor L4, the diode D40 and the switch Sl constituting the charge circuit 4b, and additionally shows the current il flowing through the reactor L4.

[0097] In the equivalent circuit thus obtained, the following formula holds by introducing duties drec, dc, and dz at which the switches Srec, Sc, and Sz are respectively conductive and a DC current Idc input into the inverter 5.

[0098] ~~[Math 13]~~

$$\begin{bmatrix} irec \\ ic \\ iz \end{bmatrix} = \begin{bmatrix} drec & 1 \\ dc & 0 \\ dz & 0 \end{bmatrix} \cdot \begin{bmatrix} Idc \\ il \end{bmatrix} \quad \cdots(13)$$

[0099] The currents irec1, ic and iz are obtained by multiplying the DC current Idc by the duties drec, dc and dz, respectively, and thus are average values in switching cycles of the respective switches Srec, Sc and Sz.

[0100] The DC current Idc is the sum of the currents irec1, ic, and iz ~~conducted~~ flowing through by the respective switches Srec, Sc and Sz, and thus the following formula holds. Note that $0 \leq drec \leq 1$, $0 \leq dc \leq 1$, and $0 \leq dz \leq 1$.

[0101] ~~[Math 14]~~

$$drec + dc + dz = 1 \quad \cdots(14)$$

[0102] The duties drec, dc and dz can thus be considered as current distribution ratios of the DC current Idc to the respective currents irec1, ic, and iz. The duty drec is hereinafter also referred to as a rectifying duty drec, as the duty drec is a duty at which a period in which the converter 3 is connected to the DC link 7, and allows a current to flow through the inverter 5 is set. The duty dc may be hereinafter also referred to as a discharge duty dc as the duty dc is a duty at which the capacitor C4 discharges. The duty dz may be hereinafter also referred to as a zero duty dz as the duty dz is a duty at which the zero-phase current iz always flows through the inverter 5 regardless of a voltage output from the inverter 5.

[0103] The rectifying duty drec and the discharge duty dc are respectively set by the following formulas (15) and (16) from the formulas (10), (12) and (13).

[0104] ~~[Math 15]~~

$$drec = (1-k)\cdot\frac{Im}{Idc}\cdot\left|\sin(\omega t)\right| \quad \cdots(15)$$

[0105] ~~[Math 16]~~

$$dc = k\cdot\frac{Vm}{2Vc}\cdot\frac{Im}{Idc}\cdot(1+\cos(2\omega t)) \quad \cdots(16)$$

[0106] That is to say, the formulas (10), (12), (15) and (16) are used to meet the demand for the power balance, and the formula (11) is used to further meet the demand for making the input current Iin ~~be~~ have a sinusoidal waveform and satisfaction of the formula (1) on which the above-mentioned formulas are based.

[0107] In a case where the diode bridge is used as the converter 3, the converter 3 cannot actively be switched at the rectifying duty drec expressed by the formula (15). By switching the inverter 5 and the switch Sc respectively in accordance with the zero duty dz and the discharge duty dc determined by the formulas (14), (15) and (16), the current irec1 expressed by the formula (10) can be obtained.

[0108] The inverter 5 cannot utilize the DC voltage at the DC link 7 in a period in which the zero-phase current iz flows. A virtual DC voltage (hereinafter, referred to as a "virtual DC voltage") Vdc in a period in which the inverter 5 can perform power conversion out of the DC voltage across the DC power supply lines LH and LL can be considered as follows.

[0109] ~~[Math 17]~~

$$Vdc = Vrec\cdot drec + Vc\cdot dc + 0\cdot dz \quad \cdots(17)$$

[0110] This can be understood as a voltage applied to the DC link 7 as an average of the maximum value of a voltage that the inverter 5 can output, in a period in which switching of the switches Sc and Sl and the inverter 5 is controlled. In FIG. 4, the virtual DC voltage Vdc is understood as a voltage generated across a current source Idc (which flows the DC current Idc) representing the inverter 5 and a load thereof.

[0111] A ratio R (= Vdc/Vm) of the virtual DC voltage Vdc to the crest value Vm is hereinafter referred to as a voltage utilization ratio. It is understood from the formulas (13), (14) and (16) that, by reducing the zero duty dz, a period in which the inverter 5 flows the zero-phase current can be reduced, and a period in which a voltage applied to a DC link voltage is utilized can be thereby increased. This leads to an increase in voltage utilization ratio R.

[0112] Incidentally, the input power Pdc input from the DC link 7 into the inverter 5 is the product of the virtual DC voltage Vdc and the DC current Idc. Since the inverter 5 obtains, from the DC link 7, the input power Pdc (= Pin + Pc − Pl) obtained by subtracting the charge power Pl from the sum of the pulsating power Pin and the discharge power Pc, the following formula (18) holds.

[0113] ~~[Math 18]~~

$$Idc = \frac{Pin + Pc - Pl}{Vdc} = \frac{Vm \cdot Im}{2}(1-(1-2k)\cos(2\omega t)) \cdot \frac{1}{Vdc} \quad \cdots(18)$$

[0114] Note that neither the virtual DC voltage Vdc nor the DC current Idc is limited in the settings having described so far. This means that, once the buffer distribution ratio k is determined, the duties drec, dc, and dz can be set regardless of settings of the virtual DC voltage Vdc and the DC current Idc as long as the virtual DC voltage Vdc and the DC current Idc~~these~~ satisfy the formula (18).

[0115] Requirements for an increase in voltage utilization ratio R as a new effect is now described. As described above, the voltage utilization ratio R can be increased by reducing the zero duty dz, and a lower limit of the zero duty dz is zero. The duties drec and dc when the virtual DC voltage Vdc is the highest per buffer distribution ratio k can be obtained when the zero duty dz is zero.

[0116] If the zero duty dz is zero, the formula (19) is obtained from the formulas (14), (15) and (16).

[0117] ~~[Math 19]~~

$$\frac{\mathrm{Im}}{\mathrm{Idc}}\left\{(1-\mathrm{k})\cdot\left|\sin(\omega t)\right|+\frac{\mathrm{k}\cdot\mathrm{Vm}}{2\mathrm{Vc}}(1+\cos(2\omega t))\right\}=1 \quad \cdots(19)$$

[0118] The both-end voltage Vc can herein be considered to be approximately constant (vary by approximately 5%, for example, as described above) even if charge and discharge are performed by the power buffer circuit 4. The DC current Idc when the virtual DC voltage Vdc is the highest per buffer distribution ratio k is determined from the formula (19). As a result, the duties drec and dc when the virtual DC voltage Vdc is the highest per buffer distribution ratio k are determined from the formulas (15) and (16). The virtual DC voltage Vdc in this case is determined by the formulas (18) and (19).

[0119] The DC current Idc when the virtual DC voltage Vdc is the highest as described above takes a minimum value in view of the formula (18). This is desirable to reduce power ratings of the switching elements Sup, Svp, Swp, Sun, Svn and Swn and the diodes Dup, Dvp, Dwp, Dun, Dvn and Dwn used in the inverter 5.

[0120] FIGs. 5 and 6 are graphs showing operation of the direct power converter shown in FIG. 1, and show the operation in a case where the duties drec, dc, and dz (= 0) are set to satisfy the formulas (14) to (19). Note that k = 1/6 in FIG. 5, and k = 1/2 is set in FIG. 6.

[0121] In each of FIGs. 5 and 6, the duties drec, dc and dz are shown in the first tier, the virtual DC voltage Vdc, a first component drec·Vrec and a second component dc·Vc of the virtual DC voltage Vdc~~thereof~~, and the DC current Idc are shown in the second tier, the current irec (being equal to the absolute value of the input current Iin) output from the converter 3 and the currents irec1, il and ic are shown in the third tier, and the powers Pin, Pc, Pbuf and Prec are shown in the fourth tier. In each of the graphs, the horizontal axis represents the phase ωt with "degree" as the unit.

[0122] Note that the first component drec·Vrec of the virtual DC voltage Vdc is a voltage appearing in the first term of the formula (17), and indicates contribution of the converter 3 to the virtual DC voltage Vdc. The second component dc·Vc of the virtual DC voltage Vdc is a voltage appearing in the second term of the formula (17), and indicates contribution of the capacitor C4 to the virtual DC voltage Vdc. Calculation is performed on the assumption that Vm = 1, Im = $\sqrt{2}$, and Vc = 1.5Vm = 1.5 for convenience sake.

[0123] Since k = 1/2 in FIG. 6, pulsations (in the second term of the rightmost-hand side of the formula (1)) of the pulsating power are all cancelled by the power buffer circuit 4. The input power Pdc input into the inverter 5 is thus maintained constant. In this case, irec1 = il holds from the formulas (10) and (11).

[0124] FIG. 7 is a graph showing the virtual DC voltage Vdc in cases where k = 1/2, 1/4 or 1/6, and dz = 0. This means that the virtual DC voltage Vdc determined by the formulas (18) and (19) is shown.

[0125] As can be understood from the formula (15), drec = 0 holds when ωt = nπ, and thus dc = 1 holds by setting dz = 0. Thus, Vdc = Vc (= 1.5) holds when the phase ωt is 0 degrees, 180 degrees, and 360 degrees in FIG. 7. As can be understood from the

formula (16), dc = 0 holds when $\omega t = (2n-1)\pi/2$, and thus drec = 1 holds by setting dz = 0. Thus, Vdc = Vm (= 1) holds when the phase ωt is 90 degrees and 270 degrees in FIG. 7.

[0126] As can be understood from these graphs, the voltage utilization ratio R higher than the voltage utilization ratio $(1/\sqrt{2})$ introduced in Non-patent Document 2 and Patent Document 1 can be obtained.

[0127] In a case where dz is not set to zero, the virtual DC voltage Vdc can be set to a constant value. A specific example thereof and an upper limit of the virtual DC voltage Vdc as constant are described below.

[0128] As can easily be understood from FIG. 7, the virtual DC voltage Vdc increases with increasing buffer distribution ratio k, and thus a case where k = 1/2 is considered. In this case, the virtual DC voltage Vdc approximately takes the crest value Vm or more in a whole section of the phase ωt, but takes the crest value Vm or less when the phase ωt is in a range of 30 degrees to 150 degrees and in a range of 210 degrees to 330 degrees. Even when k = 1/2 and dz = 0, the virtual DC voltage Vdc cannot be set to a constant value equal to or more than the crest value Vm.

[0129] FIG. 8 is a graph showing operation of the direct power converter in a case where dz < 0 is virtually allowed, and Vdc = Vm holds when k = 1/2 while satisfying the formulas (15) and (16). As in FIGs. 5 to 7, calculation is herein performed on the assumption that Vm = 1, $Im = \sqrt{2}$, and Vc = 1.5Vm = 1.5. With reference to FIG. 7, it is understood that dz < 0 holds when the phase ωt is in the range of 30 degrees to 150 degrees and in the range of 210 degrees to 330 degrees.

[0130] A maximum value of the virtual DC voltage Vdc that is constant is thus obtained by setting dz = 0 as follows. Since the virtual DC voltage Vdc is the highest when k = 1/2 as described above, a condition to satisfy drec + dc = 1 in this case is

considered. The formula (20) holds by substituting k = 1/2 in the formula (19). Note that x = |sin(ωt)| is introduced.

[0131] ~~[Math 20]~~

$$drec + dc = \frac{1}{2} \cdot \left[x + \frac{Vm}{Vc}(1 - x^2) \right] = 1 \quad \cdots(20)$$

[0132] Pdc = Vm·Im/2 holds as Pdc = Vdc·Idc and k = 1/2, and thus the formula (21) is obtained.

[0133] ~~[Math 21]~~

$$Vdc = \frac{Vm}{2} \cdot \frac{Im}{Idc} = \frac{Vm}{x + \frac{Vm}{Vc}(1 - x^2)} \quad \cdots(21)$$

[0134] The phase ωt providing the maximum value of the virtual DC voltage Vdc provides a minimum value of a denominator of the right-hand side of the formula (21). Therefore, the phase ωt when a value of the formula (22) indicating a derivative of the denominator is zero should be obtained.

[0135] ~~[Math 22]~~

$$\frac{d}{d(\omega t)} \left[|\sin(\omega t)| + \frac{Vm}{Vc}(1 - \sin^2(\omega t)) \right] = \cos(\omega t) \cdot \left[1 - \frac{2Vm}{Vc} \sin(\omega t) \right] \quad \cdots(22)$$

[0136] In this case, x = Vc/(2·Vm). In the above-mentioned example, it is understood that the maximum value of the virtual DC voltage Vdc that is constant is approximately 0.96Vm as Vc = 1.5Vm.

[0137] FIG. 9 is a graph showing operation of the direct power converter in a case where Vc = 1.5Vm = 1.5 and Vdc = 0.96Vm = 0.96 (Vm = 1). It is understood that dz ≥ 0 holds in a whole section of the phase ωt.

[0138] When the buffer distribution ratio k is fixed to 1/2 as described above, by fixing the duties in accordance with the formulas (14), (15) and (16), the virtual DC voltage Vdc can be set to be constant. It is understood that, with the technique, the voltage utilization ratio R can be set to $\alpha/(1+\alpha\cdot\alpha/4)$ (where $\alpha = Vc/Vm$) by setting x to $Vc/(2\cdot Vm)$ in the formula (21) by reducing the zero duty dz.

[0139] A condition that a ratio α should satisfy to let the voltage utilization ratio $R = \alpha/(1+\alpha\cdot\alpha/4)$ be larger than the voltage utilization ratio $(1/\sqrt{2})$ introduced in Non-patent Document 2 and Patent Document 1 is $2\sqrt{2} - 2 < \alpha < 2\sqrt{2} + 2$. The both-end voltage Vc is charged to be higher than the crest value Vm, and the ratio α is larger than 1. To set the virtual DC voltage Vdc to be constant, $\alpha \leq 2$ holds as $x = |\sin(\omega t)| = \alpha/2$. The condition is thus satisfied, and the voltage utilization ratio R larger than the voltage utilization ratio $(1/\sqrt{2})$ introduced in Non-patent Document 2 and Patent Document 1 can be obtained.

[0140] It is understood that the voltage utilization ratio R takes a maximum value of 1 when a value obtained by differentiating the voltage utilization ratio R with respect to the ratio α is zero, i.e., $\alpha = 2$. That is, the maximum value of 1 of the voltage utilization ratio R can be obtained by setting the both-end voltage Vc to be twice the crest value Vm.

[0141] (b-6) Setting of Duties Independent of Constant k

In this section, a technique for setting the duties drec, dc, and dz independently of the buffer distribution ratio k is described. In this section, the duties drec and dc are respectively set by the formulas (23) and (24). The zero duty dz is determined by the formulas (23), (24) and (14).

[0142] ~~[Math 23]~~

$$\begin{aligned} \text{drec} &= \frac{\text{Vdc}}{\text{Vm}}\left|\sin(\omega t)\right| \\ &= \frac{\text{Vdc}}{\text{Vrec}}\cdot\sin^2(\omega t) \quad \cdots(23) \end{aligned}$$

[0143] ~~[Math 24]~~

$$\begin{aligned} \text{dc} &= \frac{\text{Vdc}}{\text{Vc}}\cdot\cos^2(\omega t) \\ &= \frac{\text{Vdc}}{2\text{Vc}}(1+\cos(2\omega t)) \quad \cdots(24) \end{aligned}$$

[0144] The rectifying duty drec can be expressed as a value obtained by dividing the product of the square of the sine value of the phase ωt and the virtual DC voltage Vdc by the rectified voltage Vrec, for example. The discharge duty dc can be expressed as a value obtained by dividing the product of the square of a cosine value of the phase ωt and the virtual DC voltage Vdc by the both-end voltage Vc, for example.

[0145] It is clear from the formula (25) that the rectifying duty drec and the discharge duty dc thus set satisfy the formula (17).

[0146] ~~[Math 25]~~

$$\begin{aligned} \text{drec}\cdot\text{Vrec} + \text{dc}\cdot\text{Vc} &= \text{Vdc}\left|\sin(\omega t)\right|\cdot\left|\sin(\omega t)\right| + \text{Vdc}\cdot\cos^2(\omega t) \\ &= \text{Vdc} \quad \cdots(25) \end{aligned}$$

[0147] The virtual DC voltage Vdc can thus arbitrarily be set, e.g., to a constant value independent of the phase ωt, while the rectifying duty drec and the discharge duty dc are set to values independent of the buffer distribution ratio k.

[0148] In this setting, the DC current Idc is expressed by the formula (18) as the relation Pdc = Vdc·Idc = Pin + Pc – Pl holds.

[0149] It is assumed that the input current Iin is expressed by Im·sin(ωt), i.e., the input current Iin has a sinusoidal waveform, and thus the current il satisfies the following formula (26) dependently on the DC current Idc.

[0150] ~~[Math 26]~~

$$il = Im \cdot |\sin(\omega t)| - drec \cdot Idc$$
$$= (Im - \frac{Vdc}{Vm} \cdot Idc) \cdot |\sin(\omega t)| \quad \cdots (26)$$

[0151] The above-mentioned description shows that the rectifying duty drec and the discharge duty dc are set to the values independent of the buffer distribution ratio k, and the virtual DC voltage Vdc can be set to be constant. However, the virtual DC voltage Vdc that is constant has an upper limit. As described in the previous section, the formula (27) holds from the formulas (23) and (24) by considering drec + dc = 1 and introducing x = |sin(ωt)|.

[0152] ~~[Math 27]~~

$$drec + dc = \frac{Vdc}{Vm} \cdot x + \frac{Vdc}{Vc} \cdot (1 - x^2) = 1 \quad \cdots (27)$$

[0153] The formula (28) is thus obtained, and is the same as the formula (21). In the above-mentioned example, it is understood that the maximum value of the virtual DC voltage Vdc that is constant is approximately 0.96Vm as Vc = 1.5Vm.

[0154] ~~[Math 28]~~

$$Vdc = \frac{1}{\frac{x}{Vm} + \frac{1 - x^2}{Vc}} = \frac{Vm}{x + \frac{Vm}{Vc}(1 - x^2)} \quad \cdots (28)$$

[0155] A graph showing operation of the direct power converter obtained when k = 1/2 thus matches the graph of FIG. 9 described in the previous section. For example, the formula (26) matches the formula (11) with k = 1/2 in the formula (18).

[0156] In this section, however, the duties drec, dc, and dz are set independently of the buffer distribution ratio k, and thus the buffer distribution ratio k is reduced, and the virtual DC voltage Vdc can be controlled to be constant while the formula (28) is satisfied.

[0157] FIG. 10 is a graph showing operation of the direct power converter in a case where Vc = 1.5Vm = 1.5 and Vdc = 0.96Vm = 0.96 (Vm = 1). It is understood that dz ≥ 0 holds in a whole section of the phase ωt. The formulas (10) and (11) do not hold in contrast to the technique described in the previous section as k is herein 1/6, which is different from 1/2. Specifically, the current irec1 is expressed by the formula (29) with reference to the formulas (13), (18) and (23).

[0158] ~~[Math 29]~~

$$\begin{aligned} \text{irec1} &= \text{drec} \cdot \text{Idc} = \frac{\text{Vdc}}{\text{Vm}} \left|\sin(\omega t)\right| \cdot \frac{\text{Vm} \cdot \text{Im}}{2\text{Vdc}} (1 - (1 - 2k)\cos(2\omega t)) \\ &= \frac{\text{Im}}{2} \left|\sin(\omega t)\right| \cdot (1 - (1 - 2k)\cos(2\omega t)) \quad \cdots (29) \end{aligned}$$

[0159] (b-7) Setting of DC Current Idc

Not only the duties drec, dc, and dz but also the DC current Idc is required to be set based on the formula (18) in a case where any of the techniques described in the above-mentioned sections (b-5) and (b-6) is used. An example to achieve the formula (18) used for the DC current Idc is described in this section.

[0160] As for operation of a normal AC load, a case where well-known dq-axis control is performed is taken as an example. A power formula on the dq axes is typically expressed by the formula (30). Symbols V* and I respectively represent a command value of a voltage applied to the AC load and a current flowing through the AC load. They are both alternating, and thus a dot indicating that they are each expressed as a complex number is attached to each of the symbols V* and I. Note that a q-axis voltage ideally follows a command value Vq* thereof, and a d-axis voltage ideally follows a command value Vd* thereof.

[0161] ~~[Math 30]~~

$$P + jQ = \dot{V}^* \cdot \dot{I} = Vd^* \cdot Id + Vq^* \cdot Iq + j(Vq^* \cdot Id - Vd^* \cdot Iq) \quad \cdots (30)$$

[0162] A power supplied from the DC power supply lines LH and LL to the inverter 5 does not have a reactive power, and thus the power is expressed by the formula (31) by ignoring the second term of the formula (30).

[0163] [Math 31]

$$Pdc = Vd* \cdot Id + Vq* \cdot Iq \quad \cdots(31)$$

[0164] On the other hand, the formula (32) holds from the formula (18) as Pdc = Vdc·Idc.

[0165] [Math 32]

$$Pdc = \frac{Vm \cdot Im}{2}(1-(1-2k)\cos(2\omega t))$$
$$= \frac{Vm \cdot Im}{2} - \frac{(1-2k) \cdot Vm \cdot Im}{2}\cos(2\omega t) \quad \cdots(32)$$

[0166] Control to achieve the formula (18) can thus be performed by performing control so that an AC component of the formula (31) and the second term of the rightmost-hand side of the formula (32) match each other. FIG. 11 is a block diagram showing an example of configuration to perform the above-mentioned control. This configuration is provided, for example, in configuration shown as a controller 10 in FIG. 1.

[0167] A part of the configuration of FIG. 11 showing a well-known technique is briefly described. A current phase command value β* is input to obtain trigonometric function values cosβ* and −sinβ*, and, from these and a current command value Ia*, a q-axis current command value Iq* and a d-axis current command value Id* are generated. On the assumption that the inductive load 6 is a rotary machine, the q-axis voltage command value Vq* and the d-axis voltage command value Vd* are obtained based on a rotation angular velocity ωm of the rotary machine, a field magnetic flux Φa of the rotary machine, d-axis inductance Ld and q-axis inductance Lq of the rotary machine, the q-axis

current command value Iq* and the d-axis current command value Id*, and a q-axis current Iq and a d-axis current Id. Voltage command values Vu*, Vv*, and Vw* for controlling the inverter 5 are generated from the q-axis voltage command value Vq* and the d-axis voltage command value Vd*.

[0168] In the configuration shown in FIG. 1, for example, a velocity detector 9 detects the AC currents Iu, Iv and Iw flowing through the inductive load 6, and, based on these, the rotation angular velocity ωm, the q-axis current Iq and the d-axis current Id are provided to the controller 10.

[0169] The controller 10 obtains, based on the voltage command values Vu*, Vv*, and Vw*, signals SSup, SSvp, SSwp, SSun, SSvn and SSwn (see FIG. 1) for respectively controlling operation of the switching elements Sup, Svp, Swp, Sun, Svn and Swn of the inverter 5 through arithmetic processing, which is not shown (see, for example, Patent Document 1).

[0170] The controller 10 also generates signals SSc and SSl for respectively controlling operation of the switches Sc and Sl, which are generated based on the duties drec, dc, dz, and dl (see, for example, Patent Document 1).

[0171] A processor 71 for performing control so that the AC component of the formula (31) and the second term of the rightmost-hand side of the formula (32) match each other is described below. The processor 71 includes a DC power calculator 711, a pulsating component extractor 712, a pulsating component calculator 713, a subtracter 714, an adder 715 and a PI processor 716.

[0172] The DC power calculator 711 receives the q-axis voltage command value Vq* and the d-axis voltage command value Vd* and the q-axis current Iq and the d-axis current Id, calculates the input power Pdc based on the above-mentioned formula (31), and provides the input power Pdc~~it~~ to the pulsating component extractor 712.

CLAIMS

1. A power converter comprising:

a DC link (7) that includes a first power supply line (LH) and a second power supply line (LL);

a converter (3) that receives a single-phase AC voltage (Vin), and outputs a pulsating power (Pin) to said DC link;

an inverter (5) that receives a power from said DC link, and outputs an AC current (Iu, Iv and Iw); and

a power buffer circuit (4) that receives a charge power (Pl) from said DC link, and outputs a discharge power (Pc) to said DC link, wherein

when at least said pulsating power exceeds a predetermined value, a variation (Pc − Pl) of said discharge power to said charge power is smaller than an AC component (Pin^) of said pulsating power.

2. The power converter according to claim 1, wherein

an input power (Pdc) input from said DC link (7) into said inverter (5) takes a value (Pin + Pc − Pl) obtained by subtracting said charge power from a sum of said pulsating power and said discharge power, and

when at least said pulsating power exceeds said predetermined value, said charge power (Pl) takes a value (k·Pin) which is a constant (k) (where said constant is a positive number less than 1/2) times said pulsating power (Pin), and said discharge power (Pc) takes a value (2k·Pin^ + Pl) obtained by adding said charge power to (−2) times said AC component (Pin^) of said pulsating power multiplied by said constant.

3. The power converter according to claim 2, wherein

said converter ~~(3)~~

applies a rectified voltage ~~(Vrec)~~ obtained by full-wave rectifying said single-phase AC voltage ~~(Vm·sin(ωt))~~ to said DC link ~~(7)~~ so that a higher electric potential is applied to said first power supply line ~~(LH)~~ than said second power supply line ~~(LL)~~, and

allows, when at least said pulsating power exceeds said predetermined value, a current ~~((1 − k)·Im·|sin(ωt)|)~~ obtained by multiplying a first current by a value ~~(1 − k)~~ obtained by subtracting said constant from 1 to flow through said DC link, said first current being a current ~~(Im·|sin(ωt)|)~~ obtained by dividing said pulsating power ~~(Pin)~~ by said rectified voltage ~~(Vrec)~~,

said power buffer circuit ~~(4)~~ includes:

a discharge circuit ~~(4a)~~ that includes a capacitor ~~(C4)~~ and a first switch ~~(Sc and D42)~~ that is connected in series to said capacitor between said first power supply line and said second power supply line so as to be closer to said first power supply line than said capacitor is; and

a charge circuit ~~(4b)~~ that charges said capacitor, and

when at least said pulsating power exceeds said predetermined value, said power buffer circuit ~~(4)~~ receives a charge current ~~(il = k·Im·|sin(ωt)|)~~ which is said constant times said first current, and outputs a discharge current ~~(ic)~~ that is a current ~~(Pc/Vc)~~ obtained by dividing said discharge power ~~(Pc)~~ by a both-end voltage ~~(Vc)~~ across said capacitor.

4. The power converter according to claim 2, wherein

said converter ~~(3)~~ applies a rectified voltage ~~(Vrec)~~ obtained by full-wave rectifying said single-phase AC voltage ~~(Vin)~~ to said DC link ~~(7)~~ so that a higher electric

potential is applied to said first power supply line (LH) than said second power supply line (LL),

said power buffer circuit (4) includes:

a discharge circuit (4a) that includes a capacitor (C4) and a first switch (Sc and D42) that is connected in series to said capacitor between said first power supply line and said second power supply line so as to be closer to said first power supply line than said capacitor is; and

a charge circuit (4b) that charges said capacitor,

a rectifying duty (drec) that is a duty at which said converter is in conduction with said DC link (7) takes a value (Vdc/Vm·|sin(ωt)|) obtained by dividing a product of a predetermined voltage (Vdc) and a square ($\sin^2(\omega t)$) of a sine value of a phase (ωt) of said single-phase AC voltage by said rectified voltage (Vrec), and

a discharge duty (dc) that is a duty at which said capacitor discharges takes a value (Vdc/Vc·$\cos^2(\omega t)$) obtained by dividing a product of said predetermined voltage and a square ($\cos^2(\omega t)$) of a cosine value of said phase by a both-end voltage (Vc) across said capacitor.

5. The power converter according to any one of claims 2 to 4, wherein

said constant (k) is independent of said AC current (Iu, Iv and Iw).

6. The power converter according to any one of claims 2 to 4, wherein

said constant (k) is inversely proportional to a magnitude of said AC current (Iu, Iv and Iw).

7. The power converter according to any one of claims 1 to 6, wherein

said predetermined value is set so as to be smaller than a maximum rated power of said pulsating power.

8. The power converter according to any one of claims 1 to 7, wherein

when said pulsating power is equal to or smaller than a predetermined value, said variation ~~(Pc—Pl)~~ of said discharge power to said charge power is equal to said AC component ~~(Pin^)~~ of said pulsating power.

9. The power converter according to any one of claims 1 to 8, wherein

when said pulsating power exceeds a predetermined value, said variation (Pc – Pl) of said discharge power to said charge power is independent of said pulsating power.