algorithm can be meaningfully executed on a processor, e.g., to classify an image or speech sample, during the evaluation stage, the neural network must first be trained. The training stage can be time consuming and requires intensive computation.

## SUMMARY

**[0005]** There is disclosed a hybrid analog-digital processor comprising: circuitry comprising an analog processor, wherein the circuitry is configured to perform a mathematical operation using a plurality of passes, wherein for each of the plurality of passes, the circuitry is configured to: determine one or more scaling factors for the pass based on a set of parameters representing a portion of a matrix; scale at least some parameters of the set of parameters based on the one or more scaling factors to produce a scaled set of parameters; program the analog processor based on the scaled set of parameters; generate a plurality of input analog signals based on an input data set; generate a plurality of output analog signals based on the plurality of input analog signals and the scaled set of parameters; generate a partial output data set based on the plurality of output analog signals; and scale the partial output data set based on the one or more scaling factors to produce a scaled partial output data set, wherein the circuitry is further configured to generate an accumulated output data set by accumulating the scaled partial output data sets generated by at least two of the plurality of passes, wherein the accumulated output data set represents a result of the mathematical operation.

**[0006]** In some embodiments, generating a plurality of output analog signals based on the plurality of input analog signals and the scaled set of parameters comprises performing a matrix-matrix multiplication based on the plurality of input analog signals and the scaled set of parameters.

**[0007]** In some embodiments, generating a plurality of output analog signals based on the plurality of input analog signals and the scaled set of parameters comprises performing a convolution based on the plurality of input analog signals and the scaled set of parameters.

**[0008]** In some embodiments, programming the analog processor based on the scaled set of parameters comprises setting respective gains or attenuations for a plurality of analog amplifiers or attenuators of the analog processor based on the scaled set of parameters.

**[0009]** In some embodiments, the analog processor comprises a photonic processor comprising a plurality of programmable photonic devices, and wherein programming the analog processor

based on the scaled set of parameters comprises setting respective characteristics for the plurality of programmable photonic devices based on the scaled set of parameters.

**[0010]** In some embodiments, the programmable photonic devices comprise Mach-Zehnder interferometers, and wherein setting respective characteristics for the plurality of programmable photonic devices based on the scaled set of parameters comprises: setting respective optical characteristics for the plurality of Mach-Zehnder interferometers based on the scaled set of parameters.

**[0011]** In some embodiments, the programmable photonic devices comprise optical resonators, and wherein setting respective characteristics for the plurality of programmable photonic devices based on the scaled set of parameters comprises: setting respective optical characteristics for the plurality of optical resonators based on the scaled set of parameters.

**[0012]** In some embodiments, the circuitry comprises a plurality of digital-to-analog converters (DACs), and the plurality of DACs are configured to generate the plurality of input analog signals based on the input data set.

**[0013]** In some embodiments, the circuitry comprises a plurality of analog-to-digital converters (ADCs), and the plurality of ADCs are configured to generate the partial output data set based on the plurality of output analog signals.

**[0014]** In some embodiments, the plurality of ADCs comprise n-bit ADCs, with n equal to or less than 12.

**[0015]** In some embodiments, accumulating the scaled partial output data sets generated by at least two of the plurality of passes comprises: for at least some of the passes, summing the scaled partial output data set generated by the pass with the scaled partial output data set generated by a previous pass.

**[0016]** In some embodiments, programming the analog processor comprises: programming, based on the scaled set of parameters, the analog processor with a plurality of matrices that, collectively, represent an arbitrary matrix.

**[0017]** In some embodiments, programming the analog processor with a plurality of matrices comprises: programming, based on the scaled set of parameters, the analog processor with a plurality of matrices that, collectively, represent the arbitrary matrix based on a singular value decomposition (SVD) of the arbitrary matrix.

**[0018]** In some embodiments, programming the analog processor with a plurality of matrices comprises: programming, based on the scaled set of parameters, the analog processor with a

plurality of matrices that, collectively, represent the arbitrary matrix based on a dilation of the arbitrary matrix.

**[0019]** In some embodiments, scaling at least some of the set of parameters based on the one or more scaling factors comprises dividing at least some of the set of parameters by the one or more scaling factors, and scaling the partial output data set based on the one or more scaling factors comprises multiplying the partial output data set by the one or more scaling factors.

**[0020]** In some embodiments, for each of the plurality of passes, the circuitry is further configured to determine the one or more scaling factors based on a tile of the matrix that is associated with the pass.

**[0021]** In some embodiments, for each of the plurality of passes, the circuitry is further configured to determine the one or more scaling factors based on one or more rows of the matrix.

**[0022]** In some embodiments, for each of the plurality of passes, the circuitry is further configured to determine the one or more scaling factors based on one or more singular values of the matrix.

**[0023]** In some embodiments, the one or more scaling factors comprise a first scaling factor and a second scaling factor, and scaling at least some parameters of the set of parameters based on the one or more scaling factors comprises: scaling a first subset of the set of parameters based on the first scaling factor, and scaling a second subset of the set of parameters based on the second scaling factor.

**[0024]** There is disclosed a method for performing a mathematical operation using a plurality of passes through an analog processor, the method comprising: for each of the plurality of passes: determining one or more scaling factors for the pass based on a set of parameters representing a portion of a matrix; scaling at least some parameters of the set of parameters based on the one or more scaling factors to produce a scaled set of parameters; programming the analog processor based on the scaled set of parameters; generating a plurality of input analog signals based on an input data set; generating a plurality of output analog signals based on the plurality of input analog signals and the scaled set of parameters; generating a partial output data set based on the plurality of output analog signals; and scaling the partial output data set based on the one or more scaling factors to produce a scaled partial output data set; and generating an accumulated output data set by accumulating the scaled partial output data sets generated by at least two of the plurality of passes, wherein the accumulated output data set represents a result of the mathematical operation.

**[0025]** In some embodiments, generating a plurality of output analog signals based on the plurality of input analog signals and the scaled set of parameters comprises performing a matrix-matrix multiplication based on the plurality of input analog signals and the scaled set of parameters.

**[0026]** In some embodiments, generating a plurality of output analog signals based on the plurality of input analog signals and the scaled set of parameters comprises performing a convolution based on the plurality of input analog signals and the scaled set of parameters.

**[0027]** In some embodiments, programming the analog processor based on the scaled set of parameters comprises setting respective gains or attenuations for a plurality of analog amplifiers or attenuators of the analog processor based on the scaled set of parameters.

**[0028]** In some embodiments, the analog processor comprises a photonic processor comprising a plurality of programmable photonic devices, and wherein programming the analog processor based on the scaled set of parameters comprises setting respective characteristics for the plurality of programmable photonic devices based on the scaled set of parameters.

**[0029]** In some embodiments, the programmable photonic devices comprise Mach-Zehnder interferometers, and wherein setting respective characteristics for the plurality of programmable photonic devices based on the scaled set of parameters comprises: setting respective optical characteristics for the plurality of Mach-Zehnder interferometers based on the scaled set of parameters.

**[0030]** In some embodiments, the programmable photonic devices comprise optical resonators, and wherein setting respective characteristics for the plurality of programmable photonic devices based on the scaled set of parameters comprises: setting respective optical characteristics for the plurality of optical resonators based on the scaled set of parameters.

**[0031]** In some embodiments, generating the plurality of input analog signals based on the input data set comprises providing the input data set as input to a plurality of digital-to-analog converters (DACs).

**[0032]** In some embodiments, generating the partial output data set based on the plurality of output analog signals the circuitry comprises providing the plurality of output analog signals as inputs to a plurality of analog-to-digital converters (ADCs).

**[0033]** In some embodiments, the plurality of ADCs comprise n-bit ADCs, with n equal to or less than 12.

**[0034]** In some embodiments, accumulating the scaled partial output data sets generated by at least two of the plurality of passes comprises: for at least some of the passes, summing the

scaled partial output data set generated by the pass with the scaled partial output data set generated by a previous pass.

**[0035]** In some embodiments, programming the analog processor comprises: programming, based on the scaled set of parameters, the analog processor with a plurality of matrices that, collectively, represent an arbitrary matrix.

**[0036]** In some embodiments, programming the analog processor with a plurality of matrices comprises: programming, based on the scaled set of parameters, the analog processor with a plurality of matrices that, collectively, represent the arbitrary matrix based on a singular value decomposition (SVD) of the arbitrary matrix.

**[0037]** In some embodiments, programming the analog processor with a plurality of matrices comprises: programming, based on the scaled set of parameters, the analog processor with a plurality of matrices that, collectively, represent the arbitrary matrix based on a dilation of the arbitrary matrix.

**[0038]** In some embodiments, scaling at least some of the set of parameters based on the one or more scaling factors comprises dividing at least some of the set of parameters by the one or more scaling factors, and scaling the partial output data set based on the one or more scaling factors comprises multiplying the partial output data set by the one or more scaling factors.

**[0039]** In some embodiments, determining the one or more scaling factors comprises determining the one or more scaling factors based on a tile of the matrix that is associated with the pass.

**[0040]** In some embodiments, determining the one or more scaling factors comprises determining the one or more scaling factors based on one or more rows of the matrix.

**[0041]** In some embodiments, determining the one or more scaling factors comprises determining the one or more scaling factor based on one or more singular values of the matrix.

**[0042]** In some embodiments, the one or more scaling factors comprise a first scaling factor and a second scaling factor, and scaling at least some parameters of the set of parameters based on the one or more scaling factors comprises: scaling a first subset of the set of parameters based on the first scaling factor, and scaling a second subset of the set of parameters based on the second scaling factor.

**[0043]** There is disclosed a hybrid analog-digital processor comprising: a digital-to-analog converter (DAC) unit comprising a plurality of DACs; an analog processor arranged to perform matrix-matrix multiplication and coupled to outputs of the DAC

unit; an analog-to-digital (ADC) unit comprising a plurality of ADCs and coupled to outputs of the analog

processor; a digital scaling unit coupled to outputs of the ADC unit; and a digital accumulator coupled to outputs of the digital scaling unit, wherein the digital accumulator comprises a memory unit and a digital adder.

**[0044]** In some embodiments, the hybrid analog-digital processor further comprises an amplification or attenuation unit coupled between the DAC unit and the ADC unit.

**[0045]** In some embodiments, the analog processor comprises a photonic processor comprising a plurality of programmable photonic devices.

**[0046]** In some embodiments, the programmable photonic devices comprise Mach-Zehnder interferometers.

**[0047]** In some embodiments, the programmable photonic devices comprise optical resonators.

**[0048]** In some embodiments, the analog processor is programmed with a plurality of matrices that, collectively, represent an arbitrary matrix.

**[0049]** In some embodiments, the plurality of matrices collectively represent the arbitrary matrix based on a singular value decomposition (SVD) of the arbitrary matrix.

**[0050]** In some embodiments, the plurality of matrices collectively represent the arbitrary matrix based on a dilation of the arbitrary matrix.

**[0051]** According to a first aspect of the present invention, there is provided a hybrid analog-digital processor configured to perform a mathematical operation, comprising: circuitry comprising an analog processor and an analog scaling unit, wherein the circuitry is configured to: generate a plurality of input analog signals based on an input data set; set a gain of the analog scaling unit based on a scaling factor; program the analog processor with a set of parameters representing a matrix; generate a plurality of output analog signals based on the plurality of input analog signals and the set of parameters; generate a plurality of amplified output analog signals by amplifying, using the analog scaling unit, the plurality of input analog signals and/or the plurality of output analog signals; and generate an output data set based on the plurality of amplified output analog signals.

**[0052]** In some embodiments, the analog scaling unit comprises an analog amplifier or attenuator.

**[0053]** In some embodiments, the hybrid analog-digital processor is further configured to perform a multi-pass computation based on the mathematical operation, wherein the circuitry is further configured to: set the gain of the analog scaling unit to a first value during a first pass of the multi-pass computation; and set the gain of the analog scaling unit to a second value, different from the first value, during a second pass of the multi-pass computation.

**[0054]** In some embodiments, generating a plurality of output analog signals based on the plurality of input analog signals and the set of parameters comprises performing a matrix-matrix multiplication based on the plurality of input analog signals and the set of parameters.

**[0055]** In some embodiments, generating a plurality of output analog signals based on the plurality of input analog signals and the set of parameters comprises performing a convolution based on the plurality of input analog signals and the set of parameters.

**[0056]** In some embodiments, the circuitry comprises a plurality of analog-to-digital converters (ADCs), and the plurality of ADCs are configured to generate the output data set based on the plurality of output analog signals.

**[0057]** In some embodiments, the plurality of ADCs comprise n-bit ADCs, with n equal to or less than 12.

**[0058]** In some embodiments, programming the analog processor comprises: programming, based on the set of parameters, the analog processor with a plurality of matrices that, collectively, represent an arbitrary matrix.

**[0059]** In some embodiments, programming the analog processor with a plurality of matrices comprises: programming, based on the set of parameters, the analog processor with a plurality of matrices that, collectively, represent the arbitrary matrix based on a singular value decomposition (SVD) of the arbitrary matrix.

**[0060]** In some embodiments, programming the analog processor with a plurality of matrices comprises: programming, based on the scaled set of parameters, the analog processor with a plurality of matrices that, collectively, represent the arbitrary matrix based on a dilation of the arbitrary matrix.

**[0061]** In some embodiments, the circuitry is further configured to determine the scaling factor based on the set of parameters and the input data set.

**[0062]** In some embodiments, determining the scaling factor comprises determining the scaling factor based on statistics bounds on the set of parameters and statistical bounds on the input data set.

**[0063]** According to a second aspect of the present invention, there is provided a method for performing a mathematical operation, the method comprising: generating a plurality of input analog signals based on an input data set; setting a gain of an analog scaling unit based on a scaling factor; programming an analog processor with a set of parameters representing a matrix; generating a plurality of output analog signals based on the

plurality of input analog signals and the set of parameters; generating a plurality of amplified output analog signals by amplifying, using the analog scaling unit, the

plurality of input analog signals and/or the plurality of output analog signals; and generating an output data set based on the plurality of amplified output analog signals.

**[0064]** In some embodiments, the analog scaling unit comprises an analog amplifier or attenuator.

**[0065]** In some embodiments, the hybrid analog-digital processor is further configured to perform a multi-pass computation based on the mathematical operation, wherein the circuitry is further configured to: set the gain of the analog scaling unit to a first value during a first pass of the multi-pass computation; and set the gain of the analog scaling unit to a second value, different from the first value, during a second pass of the multi-pass computation.

**[0066]** In some embodiments, generating a plurality of output analog signals based on the plurality of input analog signals and the set of parameters comprises performing a matrix-matrix multiplication based on the plurality of input analog signals and the set of parameters.

**[0067]** In some embodiments, generating a plurality of output analog signals based on the plurality of input analog signals and the set of parameters comprises performing a convolution based on the plurality of input analog signals and the set of parameters.

**[0068]** In some embodiments, the circuitry comprises a plurality of analog-to-digital converters (ADCs), and the plurality of ADCs are configured to generate the output data set based on the plurality of output analog signals.

**[0069]** In some embodiments, the plurality of ADCs comprise n-bit ADCs, with n equal to or less than 12.

**[0070]** In some embodiments, programming the analog processor comprises: programming, based on the set of parameters, the analog processor with a plurality of matrices that, collectively, represent an arbitrary matrix.

**[0071]** In some embodiments, programming the analog processor with a plurality of matrices comprises: programming, based on the set of parameters, the analog processor with a plurality of matrices that, collectively, represent the arbitrary matrix based on a singular value decomposition (SVD) of the arbitrary matrix.

**[0072]** In some embodiments, programming the analog processor with a plurality of matrices comprises: programming, based on the scaled set of parameters, the analog processor with a plurality of matrices that, collectively, represent the arbitrary matrix based on a dilation of the arbitrary matrix.

**[0073]** In some embodiments, the method further comprises determining the scaling factor based on the set of parameters and the input data set.

**[0074]** In some embodiments, determining the scaling factor comprises determining the scaling factor based on statistics bounds on the set of parameters and statistical bounds on the input data set.

**[0075]** There is disclosed a hybrid analog-digital processor comprising: circuitry comprising a photonic processor, wherein the circuitry is configured to perform a mathematical operation using a plurality of passes, wherein for each of the plurality of passes, the circuitry is configured to: determine one or more scaling factors for the pass based on a set of parameters representing a portion of a matrix; scale at least some parameters of the set of parameters based on the one or more scaling factors to produce a scaled set of parameters; program the photonic processor based on the scaled set of parameters; generate a plurality of input optical signals based on an input data set; generate a plurality of output optical signals based on the plurality of input optical signals and the scaled set of parameters; generate a partial output data set based on the plurality of output optical signals; and scale the partial output data set based on the one or more scaling factors to produce a scaled partial output data set, wherein the circuitry is further configured to generate an accumulated output data set by accumulating the scaled partial output data sets generated by at least two of the plurality of passes, wherein the accumulated output data set represents a result of the mathematical operation.

**[0076]** In some embodiments, the photonic processor comprises a plurality of programmable photonic devices, and wherein programming the analog processor based on the scaled set of parameters comprises setting respective characteristics for the plurality of programmable photonic devices based on the scaled set of parameters.

**[0077]** In some embodiments, the programmable photonic devices comprise optical resonators, and wherein setting respective characteristics for the plurality of programmable photonic devices based on the scaled set of parameters comprises: setting respective optical characteristics for the plurality of optical resonators based on the scaled set of parameters.

**[0078]** In some embodiments, the optical resonators comprise optical ring or disk resonators, and wherein setting the respective optical characteristics for the plurality of optical resonators comprises: setting respective resonant frequencies for the plurality of optical ring or disk resonators based on the scaled set of parameters.

**[0079]** In some embodiments, the programmable photonic devices comprise Franz-Keldysh modulators, and wherein setting respective characteristics for the plurality of programmable photonic devices based on the scaled set of parameters comprises: setting respective absorptions for the plurality of Franz-Keldysh modulators based on the scaled set of parameters.

**[0080]** In some embodiments, the photonic processor comprises: a first array of interconnected variable beam splitters (VBSs) comprising a first plurality of optical inputs and a first plurality of optical outputs; a second array of interconnected VBSs comprising a second plurality of optical inputs and a second plurality of optical outputs; and a plurality of controllable optical elements, each of the plurality of these controllable optical elements coupling a single one of the first plurality of optical outputs of the first array to a respective single one of the second plurality of optical inputs of the second array.

**[0081]** In some embodiments, programming the photonic processor based on the scaled set of parameters comprises programing the plurality of controllable optical elements based on the scaled set of parameters.

**[0082]** In some embodiments, each of the VBSs of the first and second array comprises a Mach-Zehnder interferometer comprising: a first beam splitter;

**[0083]** a second beam splitter; and at least one phase modulator configured to modulate a phase of light of an optical mode that couples the first beam splitter and the second beam splitter.

**[0084]** In some embodiments, each of the controllable optical elements comprises a variable attenuator and at least one phase modulator.

**[0085]** In some embodiments, generating a plurality of output optical signals based on the plurality of input optical signals and the scaled set of parameters comprises performing a matrix-matrix multiplication based on the plurality of input optical signals and the scaled set of parameters.

**[0086]** In some embodiments, programming the photonic processor comprises: programming, based on the scaled set of parameters, the photonic processor with a plurality of matrices that, collectively, represent an arbitrary matrix.

**[0087]** There is disclosed a hybrid analog-digital processor comprising: a digital-to-analog converter (DAC) unit comprising a plurality of DACs; a photonic processor arranged to perform matrix-matrix multiplication and coupled to outputs of the DAC unit; an analog-to-digital (ADC) unit comprising a plurality of ADCs and coupled to outputs of the photonic processor; a digital scaling unit coupled to outputs of the ADC unit; and a digital accumulator coupled to outputs of the digital scaling unit, wherein the digital accumulator comprises a memory unit and a digital adder.

**[0088]** In some embodiments, the hybrid analog-digital processor further comprises an optical amplification or attenuation unit coupled between the DAC unit and the ADC unit.

**[0089]** In some embodiments, the photonic processor comprises a plurality of optical resonators.

**[0090]** In some embodiments, the photonic processor comprises a first array of interconnected variable beam splitters (VBSs) comprising a first plurality of optical inputs and a first plurality of optical outputs; a second array of interconnected VBSs comprising a second plurality of optical inputs and a second plurality of optical outputs; and a plurality of controllable optical elements, each of the plurality of these controllable optical elements coupling a single one of the first plurality of optical outputs of the first array to a respective single one of the second plurality of optical inputs of the second array.

**[0091]** In some embodiments, the photonic processor is programmed with a plurality of matrices that, collectively, represent an arbitrary matrix.

**[0092]** According to a third aspect of the present invention, there is provided a hybrid analog-digital processor configured to perform a mathematical operation, comprising circuitry comprising a photonic processor and at least one amplifier, wherein the circuitry is configured to: generate a plurality of input analog signals based on an input data set; set a gain of the at least one amplifier based on a scaling factor; program the photonic processor with a set of parameters representing a matrix; generate a plurality of output optical signals based on the plurality of input optical signals and the set of parameters; generate a plurality of output analog signals based on the plurality of output optical signals; generate a plurality of amplified output signals by amplifying, using the at least one amplifier, at least one among the plurality of input optical signals, the plurality of output optical signals and the plurality of output analog signals; and generate an output data set based on the plurality of amplified output signals.

**[0093]** In some embodiments, the at least one amplifier comprises an optical amplifier and an electronic amplifier, wherein amplifying, using the at least one amplifier, at least one among the plurality of input optical signals, the plurality of output optical signals and the plurality of output analog signals comprises: amplifying the plurality of input optical signals with the optical amplifier; and amplifying the plurality of output analog signals with the electronic amplifier.

**[0094]** In some embodiments, the at least one amplifier comprises a laser, and wherein setting the gain of the amplifier comprises setting a gain of the laser.

**[0095]** In some embodiments, the hybrid analog-digital processor is further configured to perform a multi-pass computation based on the mathematical operation, wherein the circuitry is further configured to: set the gain of the at least one amplifier to a first value during a first pass

of the multi-pass computation; and set the gain of the at least one amplifier to a second value, different from the first value, during a second pass of the multi-pass computation.

**[0096]** In some embodiments, generating a plurality of output analog signals based on the plurality of input analog signals and the set of parameters comprises performing a matrix-matrix multiplication based on the plurality of input analog signals and the set of parameters.

**[0097]** In some embodiments, generating a plurality of output analog signals based on the plurality of input analog signals and the set of parameters comprises performing a convolution based on the plurality of input analog signals and the set of parameters.

**[0098]** In some embodiments, the photonic processor comprises a plurality of optical resonators.

**[0099]** In some embodiments, the photonic processor comprises: a first array of interconnected variable beam splitters (VBSs) comprising a first plurality of optical inputs and a first plurality of optical outputs; a second array of interconnected VBSs comprising a second plurality of optical inputs and a second plurality of optical outputs; and a plurality of controllable optical elements, each of the plurality of these controllable optical elements coupling a single one of the first plurality of optical outputs of the first array to a respective single one of the second plurality of optical inputs of the second array.

**[00100]** In some embodiments, programming the analog processor comprises: programming, based on the set of parameters, the analog processor with a plurality of matrices that, collectively, represent an arbitrary matrix.

**[00101]** In some embodiments, programming the analog processor with a plurality of matrices comprises: programming, based on the set of parameters, the analog processor with a plurality of matrices that, collectively, represent the arbitrary matrix based on a singular value decomposition (SVD) of the arbitrary matrix.

**[00102]** In some embodiments, programming the analog processor with a plurality of matrices comprises: programming, based on the scaled set of parameters, the analog processor with a plurality of matrices that, collectively, represent the arbitrary matrix based on a dilation of the arbitrary matrix.

**[00103]** In some embodiments, the circuitry is further configured to determine the scaling factor based on the set of parameters and the input data set.

**[00104]** In some embodiments, determining the scaling factor comprises determining the scaling factor based on statistics bounds on the set of parameters and statistical bounds on the input data set.

**[00105]** There is disclosed a method of manufacturing a hybrid analog-digital processor comprising: forming a digital-to-analog converter (DAC) unit comprising a plurality of DACs; forming a photonic processor arranged to perform matrix-matrix multiplication and coupled to outputs of the DAC unit; forming an analog-to-digital (ADC) unit comprising a plurality of ADCs and coupled to outputs of the photonic processor; forming a digital scaling unit coupled to outputs of the ADC unit; and forming a digital accumulator coupled to outputs of the digital scaling unit, wherein the digital accumulator comprises a memory unit and a digital adder.

**[00106]** In some embodiments, forming the photonic processor and forming the digital accumulator comprises forming the photonic processor and the digital accumulator on a common chip.

**[00107]** In some embodiments, forming the photonic processor and forming the digital accumulator comprises: forming the photonic processor on a first chip; forming the digital accumulator on a second chip; and bonding the first chip to the second chip.

**[00108]** In some embodiments, forming the ADC unit comprises forming a plurality of n-bit ADCs, where n is less than or equal to 12.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[00109]** Various aspects and embodiments of the application will be described with reference to the following figures. It should be appreciated that the figures are not necessarily drawn to scale. Items appearing in multiple figures are indicated by the same reference number in all the figures in which they appear.

**[00110]** FIG. 1-1A is a representation of a matrix multiplication operation computed based on tiles, in accordance with some embodiments.

**[00111]** FIG. 1-1B depicts how a sub-portion of the matrix of FIG. 1-1A can be computed, in accordance with some embodiments.

**[00112]** FIG. 1-1C is a heat map illustrating a distribution of numerical values of an input matrix, in accordance with some embodiments.

**[00113]** FIG. 1-2A is a block diagram illustrating a hybrid analog-digital matrix processor, in accordance with some embodiments.

**[00114]** FIG. 1-2B is a diagram illustrating a matrix multiplication, in accordance with some embodiments.

## CLAIMS

What is claimed is:

1. A hybrid analog-digital processor configured to perform a mathematical operation, comprising:

circuitry comprising an analog processor and an analog scaling unit, wherein the circuitry is configured to:

generate a plurality of input analog signals based on an input data set;

set a gain of the analog scaling unit based on one or more scaling factors;

program the analog processor with a set of parameters representing a matrix;

generate a plurality of output analog signals based on the plurality of input analog signals and the set of parameters;

generate a plurality of amplified or attenuated output analog signals by amplifying or attenuating, using the analog scaling unit, the plurality of input analog signals and/or the plurality of output analog signals; and

generate an output data set based on the plurality of amplified or attenuated output analog signals.

2. The hybrid analog-digital processor of claim 1, wherein the hybrid analog-digital processor is further configured to perform a multi-pass computation based on the mathematical operation, wherein the circuitry is further configured to:

set the gain of the analog scaling unit to a first value during a first pass of the multi-pass computation; and

set the gain of the analog scaling unit to a second value, different from the first value, during a second pass of the multi-pass computation.

3. The hybrid analog-digital processor of claim 1, wherein generating a plurality of output analog signals based on the plurality of input analog signals and the set of parameters comprises performing a matrix-matrix multiplication based on the plurality of input analog signals and the set of parameters.

4. The hybrid analog-digital processor of claim 1, wherein generating a plurality of output analog signals based on the plurality of input analog signals and the set of parameters comprises performing a convolution based on the plurality of input analog signals and the set of parameters.

5. The hybrid analog-digital processor of claim 1, wherein the circuitry comprises a plurality of analog-to-digital converters (ADCs), and the plurality of ADCs are configured to generate the output data set based on the plurality of output analog signals, wherein the plurality of ADCs comprise n-bit ADCs, with n equal to or less than 12.

6. The hybrid analog-digital processor of claim 1, wherein programming the analog processor comprises:

programming, based on the set of parameters, the analog processor with a plurality of matrices that, collectively, represent an arbitrary matrix.

7. The hybrid analog-digital processor of claim 6, wherein programming the analog processor with a plurality of matrices comprises:

programming, based on the set of parameters, the analog processor with a plurality of matrices that, collectively, represent the arbitrary matrix based on a singular value decomposition (SVD) of the arbitrary matrix.

8. The hybrid analog-digital processor of claim 1, wherein the circuitry is further configured to determine the one or more scaling factors based on the set of parameters and the input data set.

9. The hybrid analog-digital processor of claim 1, wherein determining the one or more scaling factors comprises determining the one or more scaling factors based on statistical bounds on the set of parameters and statistical bounds on the input data set.

10. A method for performing a mathematical operation, the method comprising:

generating a plurality of input analog signals based on an input data set;

setting a gain of an analog scaling unit based on one or more scaling factors;

programming an analog processor with a set of parameters representing a matrix;

generating a plurality of output analog signals based on the plurality of input analog signals and the set of parameters;

generating a plurality of amplified or attenuated output analog signals by amplifying or attenuating, using the analog scaling unit, the plurality of input analog signals and/or the plurality of output analog signals; and

generating an output data set based on the plurality of amplified or attenuated output analog signals.

11. The method of claim 10, wherein the hybrid analog-digital processor is further configured to perform a multi-pass computation based on the mathematical operation, wherein the circuitry is further configured to:

set the gain of the analog scaling unit to a first value during a first pass of the multi-pass computation; and

set the gain of the analog scaling unit to a second value, different from the first value, during a second pass of the multi-pass computation.

12. The method of claim 10, wherein generating a plurality of output analog signals based on the plurality of input analog signals and the set of parameters comprises performing a matrix-matrix multiplication based on the plurality of input analog signals and the set of parameters.

13. The method of claim 10, wherein generating a plurality of output analog signals based on the plurality of input analog signals and the set of parameters comprises performing a convolution based on the plurality of input analog signals and the set of parameters.

14. The method of claim 10, wherein programming the analog processor comprises:

programming, based on the set of parameters, the analog processor with a plurality of matrices that, collectively, represent an arbitrary matrix.

15. The method of claim 14, wherein programming the analog processor with a plurality of matrices comprises:

programming, based on the set of parameters, the analog processor with a plurality of matrices that, collectively, represent the arbitrary matrix based on a singular value decomposition (SVD) of the arbitrary matrix.

16. The method of claim 10, further comprising determining the one or more scaling factors based on the set of parameters and the input data set.

17. The method of claim 16, wherein determining the one or more scaling factors comprises determining the one or more scaling factors based on statistical bounds on the set of parameters and statistical bounds on the input data set.

18. A hybrid analog-digital processor configured to perform a mathematical operation, comprising:

circuitry comprising a photonic processor and at least one amplifier, wherein the circuitry is configured to:

generate a plurality of input analog signals based on an input data set;

set a gain of the at least one amplifier based on one or more scaling factors;

program the photonic processor with a set of parameters representing a matrix;

generate a plurality of output optical signals based on the plurality of input optical signals and the set of parameters;

generate a plurality of output analog signals based on the plurality of output optical signals;

generate a plurality of amplified output signals by amplifying, using the at least one amplifier, at least one among the plurality of input optical signals, the plurality of output optical signals and the plurality of output analog signals; and

generate an output data set based on the plurality of amplified output signals.

19. The hybrid analog-digital processor of claim 18, wherein the at least one amplifier comprises an optical amplifier and an electronic amplifier, wherein amplifying, using the at least one amplifier, at least one among the plurality of input optical signals, the plurality of output optical signals and the plurality of output analog signals comprises:

amplifying the plurality of input optical signals with the optical amplifier; and

amplifying the plurality of output analog signals with the electronic amplifier.

20. The hybrid analog-digital processor of claim 18, wherein the at least one amplifier comprises a laser, and wherein setting the gain of the amplifier comprises setting a gain of the laser.

21. The hybrid analog-digital processor of claim 18, wherein the hybrid analog-digital processor is further configured to perform a multi-pass computation based on the mathematical operation, wherein the circuitry is further configured to:

set the gain of the at least one amplifier to a first value during a first pass of the multi-pass computation; and

set the gain of the at least one amplifier to a second value, different from the first value, during a second pass of the multi-pass computation.

22. The hybrid analog-digital processor of claim 18, wherein generating a plurality of output analog signals based on the plurality of input analog signals and the set of parameters comprises performing a matrix-matrix multiplication based on the plurality of input analog signals and the set of parameters.

23. The hybrid analog-digital processor of claim 18, wherein generating a plurality of output analog signals based on the plurality of input analog signals and the set of parameters comprises performing a convolution based on the plurality of input analog signals and the set of parameters.

24. The hybrid analog-digital processor of claim 18, wherein the photonic processor comprises a plurality of optical resonators.

25. The hybrid analog-digital processor of claim 18, wherein the photonic processor comprises:

a first array of interconnected variable beam splitters (VBSs) comprising a first plurality of optical inputs and a first plurality of optical outputs;

a second array of interconnected VBSs comprising a second plurality of optical inputs and a second plurality of optical outputs; and

a plurality of controllable optical elements, each of the plurality of these controllable optical elements coupling a single one of the first plurality of optical outputs of the first array to a respective single one of the second plurality of optical inputs of the second array.

26. The hybrid analog-digital processor of claim 18, wherein programming the analog processor comprises:

programming, based on the set of parameters, the analog processor with a plurality of matrices that, collectively, represent an arbitrary matrix.

27. The hybrid analog-digital processor of claim 26, wherein programming the analog processor with a plurality of matrices comprises:

programming, based on the set of parameters, the analog processor with a plurality of matrices that, collectively, represent the arbitrary matrix based on a singular value decomposition (SVD) of the arbitrary matrix.

28. The hybrid analog-digital processor of claim 26, wherein programming the analog processor with a plurality of matrices comprises:

programming, based on the scaled set of parameters, the analog processor with a plurality of matrices that, collectively, represent the arbitrary matrix based on a dilation of the arbitrary matrix.

29. The hybrid analog-digital processor of claim 18, wherein the circuitry is further configured to determine the one or more scaling factors based on the set of parameters and the input data set.

30. The hybrid analog-digital processor of claim 29, wherein determining the one or more scaling factors comprises determining the one or more scaling factors based on statistical bounds on the set of parameters and statistical bounds on the input data set.