

SEMICONDUCTOR DEVICE AND METHOD OF FORMATION

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Abstract of the Disclosure

Vertically stacked regions (50 or 74) of n-type and p-type conductivity are formed around bipolar (48) and field effect (72) transistors to reduce parasitic capacitance between the semiconductor device and surrounding well regions. Under reverse bias a portion of the vertically stacked region (50 or 74) is fully depleted and thus reduces the parasitic capacitance between the semiconductor device and the well region.

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FIG. 7 accompanies this abstract.