WHAT IS CLAIMED IS:

1. An integrated circuit device comprising:

a substrate having a front surface and a rear surface, opposite to each other, and a fin-type active region defined by a trench in the front surface;

a device separation layer filling the trench;

a source/drain region on the fin-type active region;

a first conductive plug arranged on the source/drain region and electrically connected to the source/drain region;

a power wiring line at least partially arranged on the rear surface of the substrate;

a buried rail connected to the power wiring line through the device separation layer and decreasing in horizontal width toward the power wiring line; and

a power via connecting the buried rail to the first conductive plug,

wherein the integrated circuit device further comprises:

a plurality of gate electrodes extending to cross the fin-type active region;

an inter-gate insulating layer covering the source/drain region and filling between the plurality of gate electrodes;

a first power hole passing through the device separation layer;

a first insulating barrier covering inner side surfaces of the first power hole and surrounding the buried rail;

a second power hole passing through the inter-gate insulating layer; and

a second insulating barrier covering inner side surfaces of the second power hole and surrounding the power via, and

wherein a thickness of the first insulating barrier on the inner side surfaces of the first power hole is greater than a thickness of the second insulating barrier on the inner side surfaces of the second power hole.

2. The integrated circuit device of claim 1, wherein the power wiring line decreases in horizontal width toward the buried rail.

3. The integrated circuit device of claim 1 or claim 2, wherein the power via passes through the inter-gate insulating layer and decreases in horizontal width toward the buried rail.

4. An integrated circuit device comprising:

a substrate having a front surface and a rear surface, opposite to each other, and a fin-type active region defined by a trench in the front surface;

a device separation layer filling the trench;

a source/drain region on the fin-type active region;

a plurality of gate electrodes extending to cross the fin-type active region;

an inter-gate insulating layer covering the source/drain region and filling between the plurality of gate electrodes;

a first conductive plug arranged on the source/drain region and electrically connected to the source/drain region;

a power wiring line at least partially arranged on the rear surface of the substrate;

a first power hole passing through the device separation layer;

a first insulating barrier covering inner side surfaces of the first power hole with a first thickness;

a buried rail surrounded by the first insulating barrier and electrically connected to the power wiring line;

a second power hole passing through the inter-gate insulating layer;

a second insulating barrier covering inner side surfaces of the second power hole with a second thickness that is less than the first thickness; and

a power via surrounded by the second insulating barrier and connecting the buried rail to the first conductive plug.

5. The integrated circuit device of claim 4, wherein each of the first power hole and the second power hole has a tapered shape in which a horizontal width thereof decreases from an upper side thereof toward a lower side thereof in a vertical direction.

6. The integrated circuit device of claim 4 or claim 5, wherein the buried rail and the power wiring line decrease in horizontal width toward each other and are integrally formed as a single body with each other.

7. The integrated circuit device of any one of claims 4 to 6, wherein:

an uppermost end of the first insulating barrier contacts a lowermost end of the second insulating barrier at a first vertical level, and

a lowermost end of the power via contacts an uppermost end of the buried rail in the first power hole at a second vertical level that is lower than the first vertical level.

8. An integrated circuit device comprising:

a substrate having a front surface and a rear surface, opposite to each other, and a fin-type active region defined by a trench in the front surface;

a device separation layer filling the trench;

a source/drain region on the fin-type active region;

a plurality of gate electrodes extending to cross the fin-type active region;

an inter-gate insulating layer covering the source/drain region and filling between the plurality of gate electrodes;

a first conductive plug arranged on the source/drain region and electrically connected to the source/drain region;

a power wiring line at least partially arranged on the rear surface of the substrate;

a first power hole passing through the device separation layer;

a first insulating barrier covering inner side surfaces of the first power hole with a first thickness;

a buried rail surrounded by the first insulating barrier and electrically connected to the power wiring line;

a second power hole passing through the inter-gate insulating layer;

a second insulating barrier covering inner side surfaces of the second power hole with a second thickness that is less than the first thickness; and

a power via surrounded by the second insulating barrier, connecting the buried rail to the first conductive plug, and decreasing in horizontal width toward the buried rail, wherein

the buried rail and the power wiring line decrease in horizontal width toward each other.

9. The integrated circuit device of claim 8, further comprising:

a through hole passing through the substrate; and

a through electrode filling the through hole, connecting between the power wiring line and the buried rail, and decreasing in horizontal width toward the buried rail, wherein

the buried rail, the through electrode, and the power wiring line are integrally formed of a same material as a single body.