CLAIMS

1. A memory sub-system comprising:

a memory sub-system controller comprising at least one host channel;

a memory device comprising a plurality of memory die; and

at least one input/output (I/O) expander circuit coupled between the at least one host channel of the memory sub-system controller and to the memory device to connect the plurality of memory die to the memory sub-system controller, the at least one I/O expander circuit comprising:

one or more I/O buffers to send and receive signals on the at least one host channel;

a selection circuit coupled to the one or more I/O buffers; and

command processing logic to enable the selection circuit to route the signals on a selected one of a plurality of expansion channels coupled to the at least one I/O expander circuit, wherein each of the plurality of expansion channels is coupled to a corresponding subset of the plurality of memory die.

2. The memory sub-system of claim 1, wherein the one or more I/O buffers comprise:

a first I/O buffer pair coupled to the at least one host channel; and

a second I/O buffer pair coupled to the selected one of the plurality of expansion channels.

3. The memory sub-system of claim 2, wherein the command processing logic is configured to:

monitor the signals received on the at least one host channel;

determine whether a signal received on the at least one host channel corresponds to a write request or a read request from the memory sub-system controller; and

selectively enable a corresponding I/O buffer of the first I/O buffer pair and a corresponding buffer of the second I/O buffer pair.

4. The memory sub-system of claim 3, wherein the signal received on the at least one host channel comprises a volume identifier and a memory address, and wherein the command processing logic is configured to:

compare the volume identifier from the signal received on the at least one host channel to an I/O expander identifier associated with the at least one I/O expander circuit;

in response to the volume identifier matching the I/O expander identifier, determine a memory die corresponding to the memory address; and

identify the selected one of the plurality of expansion channels coupled to the determined memory die.

5. The memory sub-system of claim 1, wherein the one or more I/O buffers to limit an impedance load presented on the at least one host channel to the impedance load of the corresponding subset of the plurality of memory die associated with the selected one of the plurality of expansion channels.

6. The memory sub-system of claim 1, further comprising:

a plurality of I/O expander circuits coupled to the at least one host channel, wherein each of the plurality of I/O expander circuits is coupled to four expansion channels, wherein each of the four expansion channels of each of the plurality of I/O expander circuits is coupled to a corresponding subset of four of the plurality of memory die.

7. The memory sub-system of claim 1, wherein the memory sub-system controller comprises a plurality of host channels, and further comprising:

at least one input/output expander circuit coupled to each of the plurality of host channels.

8. An input/output (I/O) expander circuit comprising:

a host port configured to couple to at least one host channel of a memory sub-system controller;

a first set of I/O buffers coupled to the host port to send and receive signals on the at least one host channel;

a selection circuit coupled to the first set of I/O buffers;

a target port configured to couple to a plurality of expansion channels, wherein each of the plurality of expansion channels is coupled to a corresponding subset of a plurality of memory die, wherein the I/O expander circuit is to connect the plurality of memory die to the memory sub-system controller; and

command processing logic to enable the selection circuit to route the signals on a selected one of the plurality of expansion channels.

9. The I/O expander circuit of claim 8, further comprising:

a second set of I/O buffers coupled to the target port to send and receive signals on the plurality of expansion channels.

10. The I/O expander circuit of claim 9, wherein the command processing logic is configured to:

monitor the signals received on the at least one host channel;

determine whether a signal received on the at least one host channel corresponds to a write request or a read request from the memory sub-system controller; and

selectively enable a corresponding I/O buffer of the first set of I/O buffers and a corresponding I/O buffer of the second set of I/O buffers.

11. The I/O expander circuit of claim 10, wherein the signal received on the at least one host channel comprises a volume identifier and a memory address, and wherein the command processing logic is configured to:

compare the volume identifier from the signal received on the at least one host channel to an I/O expander identifier associated with the at least one I/O expander circuit;

in response to the volume identifier matching the I/O expander identifier, determine a memory die corresponding to the memory address; and

identify the selected one of the plurality of expansion channels coupled to the determined memory die.

12. The I/O expander circuit of claim 8, wherein the first set of I/O buffers to limit an impedance load presented on the at least one host channel to the impedance load of the corresponding subset of the plurality of memory die associated with the selected one of the plurality of expansion channels.

13. The I/O expander circuit of claim 8, wherein the wherein the command processing logic is configured according to configuration values for on-die termination (ODT) at the host port and the target port based on a command template associated with a capacity of the plurality of memory die.

14. A memory device comprising:

a plurality of memory die; and

at least one input/output (I/O) expander circuit configured to couple to at least one host channel of a memory sub-system controller and coupled to the plurality of memory devices, the I/O expander circuit to connect the plurality of memory die to the memory sub-system controller, the at least one I/O expander circuit comprising:

one or more I/O buffers configured to send and receive signals on the at least one host channel;

a selection circuit coupled to the one or more I/O buffers; and

command processing logic to enable the selection circuit to route the signals on a selected one of a plurality of expansion channels coupled to the at least one I/O expander circuit, wherein each of the plurality of expansion channels is coupled to a corresponding subset of the plurality of memory die.

15. The memory device of claim 14, wherein the one or more I/O buffers comprise:

a first I/O buffer pair configured to couple to the at least one host channel; and

a second I/O buffer pair coupled to the selected one of the plurality of expansion channels.

16. The memory device of claim 15, wherein the command processing logic is configured to:

monitor the signals received on the at least one host channel;

determine whether a signal received on the at least one host channel corresponds to a write request or a read request from the memory sub-system controller; and

selectively enable a corresponding I/O buffer of the first I/O buffer pair and a corresponding buffer of the second I/O buffer pair.

17. The memory device of claim 16, wherein the signal received on the at least one host channel comprises a volume identifier and a memory address, and wherein the command processing logic is configured to:

compare the volume identifier from the signal received on the at least one host channel to an I/O expander identifier associated with the at least one I/O expander circuit;

in response to the volume identifier matching the I/O expander identifier, determine a memory die corresponding to the memory address; and

identify the selected one of the plurality of expansion channels coupled to the determined memory die.

18. The memory device of claim 14, wherein the one or more I/O buffers to limit an impedance load presented on the at least one host channel to the impedance load of the corresponding subset of the plurality of memory die associated with the selected one of the plurality of expansion channels.

19. The memory device of claim 14, wherein the command processing logic is configured according to configuration values for on-die termination (ODT) in least one I/O expander circuit based on a command template associated with a capacity of the plurality of memory die.

20. The memory device of claim 14, further comprising:

a plurality of I/O expander circuits configured to couple to the at least one host channel, wherein each of the plurality of I/O expander circuits is coupled to four expansion channels, wherein each of the four expansion channels of each of the plurality of I/O expander circuits is coupled to a corresponding subset of four of the plurality of memory die.