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AN INTEGRATED CIRCUIT CHIP

RELATED APPLICATIONS

This application is related to and is being filed concurrently with IBM Docket No. HQ9-95-040 entitled "A Method of Manufacturing An Insulated Gate Field Effect Transistor", USPTO Serial No. 08/688,346, and IBM Docket No. HQ9-96-053, entitled "An Insulated Gate Field Effect Transistor", USPTO Serial No. 08/688,457, both of which are assigned to the Assignee of this application.

FIELD OF THE INVENTION

This invention relates generally to the manufacturing of semiconductor devices, and more particularly to an integrated circuit formed on a semiconductor wafer.

BACKGROUND OF THE INVENTION

High performance and density are primary objectives of Integrated Circuit (IC) chip design. One way chip designers approach both of these objectives is by making devices and device features smaller. The smaller the device feature (and other circuit features), the tighter that circuit devices can be packed together and, consequently, the higher the circuit density. The tighter together the circuit devices are packed, the lower the wiring loads and, consequently, the faster the circuit, i.e., the higher the circuit performance. So, semiconductor process designers concentrate on reducing device features to make devices smaller and smaller.

Just shrinking Field Effect Transistor (FET) channel length alters device characteristics such as punch through voltage and threshold voltage (V_t) to the point where the device may be unusable. So, other device parameters such as, channel doping, source/drain doping and gate oxide thickness are altered to compensate for device characteristic changes. Normally, the channel doping profile is altered to compensate for effects of the shorter channel (short channel effects). However, changes in the doping profile raise the V_t, so the doping profile change is usually accompanied with a thinner gate oxide to lower the V_t. Thinning the gate oxide intensifies the electric field from the gate on the channel. Consequently, gate capacitance per unit area is increased, gate area is decreased, and channel transconductance is increased. Overall, circuit performance improves.

Unfortunately, as device features shrink, what had been considered superficial imperfections for older larger devices are significant flaws. Thinner gate oxide makes devices more susceptible to these flaws causing leakages and defects that reduce chip yield and impair chip reliability. Yield loss related increase in chip cost is easy to quantify because completed wafer cost must be recovered from fewer chips. Reduced reliability related cost, cost from chips failing in normal use, is a more expensive problem. These reliability failures are more expensive because they cause system down time and because of the field cost associated with finding the failing component in an assembled system containing many chips.

FIG. 1 is a cross-sectional representation of an FET built in a 64M DRAM process. There are two deep trenches 100 on either side of the FET 102 that isolate it from adjacent FETs. An oxide collar 104 along the trench 100 sidewalls 106

isolates the FET 102 from polysilicon 108 that fills the trench and is, for example, a Dynamic Random Access Memory (DRAM) cell capacitor storage plate. The gate of the FET 102 is formed by a polysilicon word line 110 that runs across a thin gate oxide layer 112 the width of the FET 102. FET current flow, from drain to source (not shown), is perpendicular to the polysilicon gate and the word line 110.

A depression 114 was formed at each side of the channel when excess oxide was removed from the collar 104. Furthermore, collar 104 oxide formation rounded the channel sides 116. Consequently, the channel 102, while nearly planar in the center, is rounded at its sides 116. The depression 114 and rounding are flaws that were considered superficial artifacts for larger featured FETs. However, for a 64M DRAM process, they are not superficial. Poly in the depression and on the rounded sides 114 enhances the E-field so that it is much more intense there than on the rest of the channel. As a result of this intensified E field, the channel sides have a lower V_t than the rest of the channel. So, the channel does not turn on at one uniform gate to source voltage (V_{gs}). Instead, the sides 114 turn on before and off after (i.e. with a smaller V_{gs}) the rest of the FET 102.

While this condition might be negligible for logic, it is unacceptable for a DRAM pass gates, because it increases pass gate channel leakage. Pass gate channel leakage allows stored charge on the storage plate to dissipate faster. This shortens DRAM retention time, i.e., the length of time that data may be stored in a DRAM cell without it needing to be reinforced or refreshed. Generally, refresh frequency is minimized because during refresh, the DRAM is unaccessible or unavailable. However, a DRAM cell with a short retention time must be refreshed more frequently than a cell with a long

retention time. Consequently, a short retention time is undesirable. Thus, it is important to minimize channel leakage and so, to make FETs with planar channels for DRAMs.

PURPOSES OF THE INVENTION

It is a purpose of the invention to selectively reduce FET channel leakage.

It is another purpose of the present invention to selectively reduce channel variations in FET threshold voltage.

It is another purpose of the present invention to increase DRAM cell retention time.

It is yet another purpose of the present invention to reduce FET feature size.

It is yet another purpose of the present invention to selectively reduce FET feature size without reducing DRAM cell retention time.

It is yet another purpose of the invention to selectively reduce FET feature size without increasing channel leakage.

It is yet another purpose of the invention to improve threshold voltage uniformity on reduced feature size FETs.

It is yet another purpose of the invention to reduce channel leakage and variations in threshold voltage without impairing DRAM cell retention time for reduced feature size FETs.

SUMMARY OF THE INVENTION

The present invention is an integrated circuit including a plurality of first FETs with uniform gate oxide and a plurality of second FETs isolated on either side by a trench. Each second FET has a dielectric layer in the isolating trench along at least one side. The dielectric layer which may be an ONO layer has an oxidation catalyst diffused into it. The oxidation catalyst may be potassium. A gate oxide along the side of the second FET in close proximity to the ONO layer is thicker than gate oxide between both sides.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a cross-sectional representation of an FET in a DRAM made by a prior art manufacturing process.

FIGs. 2A-F represent the steps in forming a preferred embodiment FET.

FIGs. 3A-C represent the steps in selectively forming FETs with enhanced gate oxide and FETs with unenhanced gate oxide on the same chip.

FIG. 4 is a plot of oxide thickness T_{ox} versus Potassium concentrate.

FIG. 5 is an image from a Transmission Electron Microscope (TEM) at a corner of an FET grown according to a prior art method.

FIGs. 6A-B are TEM images of FETs grown according to the present invention.

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FIG. 7 is a table comprising electrical parameters of FETs, grown according to the prior art with a preferred embodiment FET.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention is an FET and the process of forming the FET. The FET of the present invention has a thicker gate oxide along channel sides than on the interior of the channel. A layer of silicon Oxide-silicon Nitride-silicon Oxide (ONO) formed at the sides of the channel region includes a catalyst that enhances local oxide formation. The preferred catalyst is potassium.

FIGs. 2A-F represent the steps in forming the preferred embodiment FET which is essentially as depicted in Fig. 2F. First, in FIG. 2A, deep trenches 120 are formed in a semiconductor layer (or wafer) 122. Prior to forming trenches 120, a pad dielectric stack, represented by layer stack 121, is formed on the semiconductor layer 122. The trenches 120 are etched through the pad stack 121 and into the wafer 122 to isolate and define an FET region 124. A channel, source and drain will be formed in this defined FET region 124. Preferably, the semiconductor layer is silicon. In the preferred embodiment, the FET, when complete, is a passgate transistor of a Dynamic Random Access Memory (DRAM) cell. The DRAM cell's storage capacitor plate is formed in the trench 120.

In FIG. 2B, an ONO layer 126 is conformally formed on the pad stack 121 and in trenches 120. Although referred to as a single layer, it is understood that the ONO layer 126 is a thin nitride layer sandwiched between two thin oxide layers. The ONO layer 126 lines the trenches 120, extending vertically

along the sides of each trench 120 past the surface 128 of the wafer 122 and along the pad stack 121. Next, an N^+ polysilicon (poly) layer 130 is deposited on the ONO layer 126.

In FIG. 2C, the polysilicon layer 130 is removed from above the pad stack 121 so that polysilicon 132 remains only in the trenches 120. Preferably, the polysilicon layer 130 is removed using Chemical-Mechanical Polish (CMP). Polishing the polysilicon layer 126 also removes most of the ONO layer 124 lying on the pad stack 121 such that ONO remains mainly in the trenches 120. After CMP, residual ONO layer 124 is removed from the pad stack 121. Then, the remaining polysilicon 130 is etched by Reactive Ion Etching (RIE) such that the remaining poly 132 in the trenches is recessed beneath the wafer surface 128, preferably, by 1.3μm. The preferred slurry for removing the poly layer 130 is a poly slurry in Potassium Hydroxide, preferably < 0.1% KOH. The silicon nitride in the ONO layer 126 is a diffusion barrier to the potassium in the slurry. So, potassium diffuses into the ONO layer 126, through the outer oxide and collects at the nitride. Optionally, to enhance the level of collected potassium, the wafer may be dipped in a tank of KOH solution.

These steps of polishing the poly layer 130 with a slurry containing KOH and the optional dip are contrary to conventional semiconductor chip manufacturing practices. Normally, such a use of potassium is avoided in semiconductor chip manufacture because potassium readily diffuses into silicon. Therefore, using a KOH slurry would, effectively, poison the silicon, making it unusable for forming FETs. However, the ONO layer 126 blocks diffusion of the potassium and instead, collects the potassium along the interface between the outer oxide and the nitride.

Next, in FIG. 2D, an Oxide collar 134 is selectively formed in the trenches 120 on the poly 132, along the ONO layer 126. After forming the collars 134, another N^+ poly layer 136 is formed on the wafer 122. This second poly layer 136 re-fills the trenches 120 with polysilicon.

In FIG. 2E, the poly layer 136 is removed from the pad stack 121 using CMP and RIE such that poly 140 remains only in the trenches 120. The poly 140 in the trenches 120 is coplanar with, or, slightly recessed from the wafer surface 128. As in the previous poly removal step, the preferred slurry is a poly slurry with < 0.1% KOH. A screen oxide layer (not shown) is grown in dry O_2 on the exposed pad stack 121 and poly 140, taking care to avoid removing the potassium from along the ONO layer 128. Then, N or P wells (if required) are defined. Next an appropriate dopant(s) is (are) ion implanted for channel tailoring. Then, the implanted dopant is diffused to the wafer as desired to bulk dope the silicon substrate 122.

After diffusing the implanted dopants, the screen oxide layer and pad stack layers 121 are removed and gate oxide may be grown. The potassium along the ONO layer 126 in the trenches 120 that was collected by the nitride is a catalyst for silicon oxidation. So, as depicted in FIG. 2F, the gate oxide is thicker along the sides 142 of the channel, i.e., in close proximity to the ONO layer 126.

As represented in FIGS. 3A-C, the ONO layer may be selectively removed in non-array areas 150, prior to growing gate oxide. This results in transistors with enhanced side oxide in arrays 152 and normal transistors with unenhanced oxide in non-array areas 150. So, in FIG. 3A, all devices, both in array areas 152 and in non-array 150, are processed as

described above for the preferred embodiment transistor, through the N-well/P-well definition and bulk doping as described above with reference to FIG. 2E.

However, prior to gate oxide formation, in FIG. 3B, a masking layer 154 is formed to define shallow trenches 156 in non-array areas 150. After forming the shallow trench pattern in masking layer 154, the shallow trenches 156 are etched. The shallow trenches extend beyond the deeper trenches 120 and, so, the ONO layer is removed from the vicinity of channel areas 158, 160, 162 in the non-array area 150.

Finally, in FIG. 3C, gate oxide 164 is formed and the poly word line 146 and poly gates 166 are patterned from a poly layer formed on the gate oxide layer 164. An integrated circuit thus formed has FETs with essentially uniform gate oxide thickness in non-array areas 150 and with enhanced gate oxide in array areas 152.

EXAMPLES

FIG. 4 is a plot of increase in oxide (T_{ox}) thickness verses Potassium concentrate. Increasing the level of accumulated potassium increases the gate oxide thickness at the channel sides. Further, this increase in gate oxide thickness extends horizontally from the sides into the channel. The extent of the increased oxide thickness, both vertically and horizontally is dependent upon the level of potassium collected in the ONO layer. If the accumulated potassium level is increased sufficiently then, the gate oxide thickens across the entire device. The increase in thickness is inversely proportional to the horizontal distance from the ONO layer 124 (i.e. from the potassium catalyst).

In addition, growth temperature and growth media affect the amount of increase in local oxide thickness derived from the presence of potassium catalyst. The side to center oxide thickness difference is much more pronounced, i.e., much thicker at the device sides than in the device center, for gate oxide grown at 900°C in dry O_2 than for gate oxide grown at 800°C in wet O_2.

FIG. 5 is a Transmission Electron Microscope (TEM) image of an FET corner (a cross-section at a side) grown according to the prior art at 900°C in O_2. For this prior art FET, corner T_{ox} (T_{ox} along the side of the channel) is 8% thinner than center T_{ox} (in the center of the channel). Thus, this prior art FET has a lower corner V_t due to this thinner corner T_{ox} and due to the more intense E-field from the poly both horizontally along the top channel area and vertically along the side (in the trench).

FIG. 6A is a TEM image of an FET corner grown at 800°C in wet O_2 according to the present invention. For this preferred embodiment FET, corner T_{ox} is 30% thicker center T_{ox}. Thus, the V_t is elevated along the channel sides over that of the prior art FET. Further, the E-field is attenuated somewhat by the thicker corner T_{ox}.

FIG. 6B is a TEM image of a preferred embodiment FET corner grown at 900°C in dry O_2. For this preferred embodiment FET, the corner T_{ox} is 70% thicker than center T_{ox}. The thickened oxide along the side of this preferred FET raises the corner V_t nearly to that of the center channel V_t.

The table of FIG. 7 is a comparison of a prior art 10μm wide FET's electrical parameters with a preferred embodiment 10μm FET, each grown at the chip location on different wafers under nearly.identical conditions. Although both devices have a nearly identical center channel V_t and nearly identical on current (I_{ds}), the corner V_t of the preferred FET is nearly equal to the center channel V_t. By contrast, the corner V_t of the prior art FET is 75% that of the corner V_t of the preferred embodiment FET. So, for the preferred embodiment device, the retention yield at 256ms (the time that charge is held in a cell) is more than 2.6 times that of the prior art FET.

While the present invention is described in terms of preferred embodiments, it is understood that numerous variations and modifications will occur to a person skilled in the art without departing in spirit from the claimed invention. It is intended that the scope of the claims include those modifications and variations that fall within the spirit of the invention.

WE CLAIM:

1.- An integrated circuit chip including a plurality of first FETs with uniform gate oxide and a plurality of second FETs isolated on either side by a trench and further comprising:

a dielectric layer along a side of each said second FET in said isolating trench;

an oxidation catalyst in said dielectric layer; and,

gate oxide along said second FET side at said dielectric layer being thicker than gate oxide between both said second FET sides.

2. The integrated circuit chip of Claim 1 wherein the plurality of second FETs further include an oxide collar on each side of each of said second FETs.

3. The integrated circuit chip of Claim 1 wherein said dielectric layer is an ONO layer.

4. The integrated circuit chip of Claim 1 wherein said oxidation catalyst is potassium.

5. The integrated circuit chip of Claim 1 wherein said plurality of First FETs are isolated on either side by a trench.

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6. An integrated circuit chip including a plurality of first FETs with uniform gate oxide and a plurality of second FETs isolated on either side by a trench and further comprising:

an ONO layer along a side of each said second FET in said isolating trench;

potassium in said ONO layer; and

gate oxide along said second FET side at said ONO layer being thicker than gate oxide between both said second FET sides.

7. The integrated circuit chip of Claim 1 wherein the plurality of second FETs further include an oxide collar on each side of each of said second FETs.

8. The integrated circuit chip of Claim 6 wherein said plurality of First FETs are isolated on either side by a trench.

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