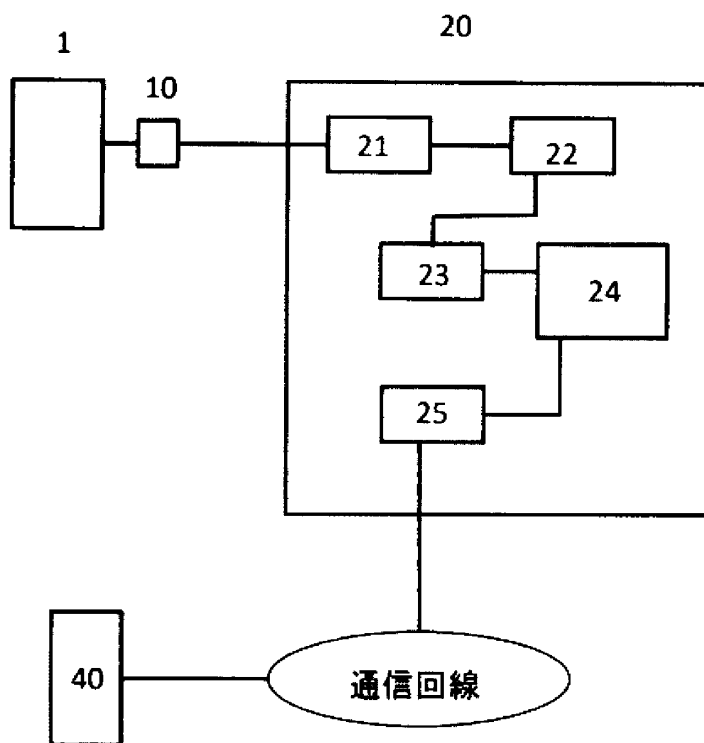


A block diagram showing a system architecture. Component 1 is a large rectangle on the left. Component 10 is a small rectangle connected to the right side of component 1. Component 20 is a large rectangle on the right, connected to the right side of component 10. Component 40 is a vertical rectangle connected to the bottom of component 20.

[図3]

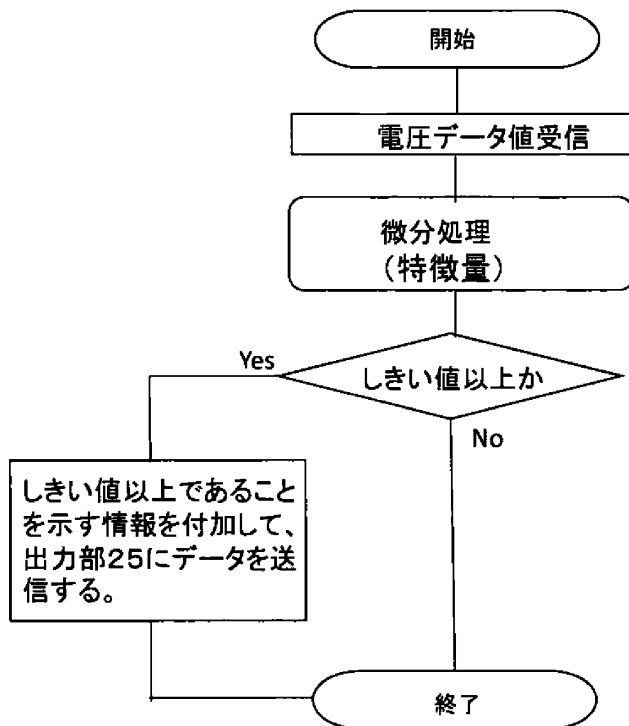


[図4]

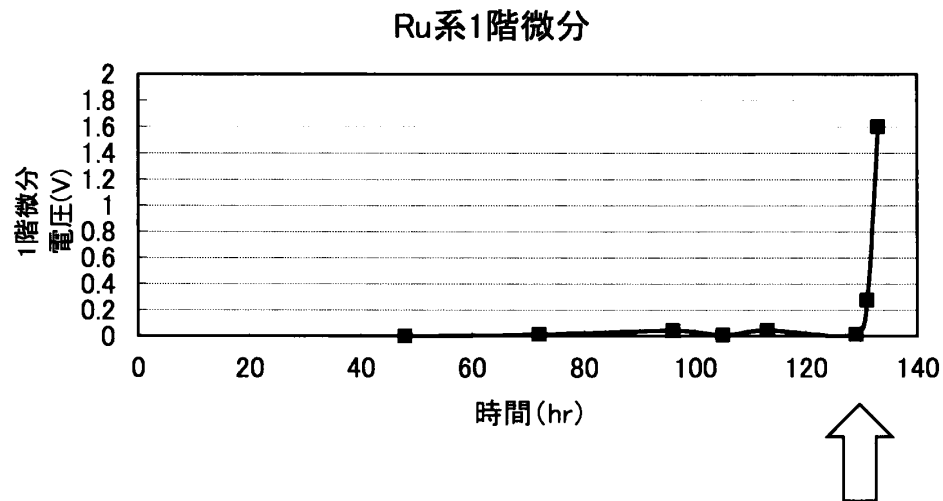
主キ一	Day	Time	積算時間 (hr)	電流 (A/cm ²)	電圧 (V)	2階微分	平均	標準偏差 (1 σ)	しきい値 (平均+3 σ)	判定結果
0001	2020/9/9	11:00:00	0	1.5	8.3	-	-	-	-	-
0002	2020/9/10	11:00:00	24	1.5	8.3	-	-	-	-	-
0003	2020/9/11	11:00:00	48	1.5	9.6	0.0005208	-	-	-	-
0004	2020/9/12	11:00:00	72	1.5	9.8	0.0012152	0.000868	0.00035	0.00191	OK

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[図5]



[図6]



[図7]

