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Title of the Invention

Wafer Level Package for Semiconductor Devices

Field of the Invention

This invention relates to a method of making a wafer level package directly on a silicon wafer that has been processed and tested at the wafer fabs. In particular, the method provides a total packaging solution at wafer level, eliminating need for further assembly and packaging steps on a silicon chip that are required before the final SMT operations. The advantage in this method being the device is diced after the wafer level packaging and assembled directly on mother boards in SMT houses.

Background of the Invention

The conventional practice of device assembly is to follow few packaging steps such as Die attach / wire bond / mold method. or Flip chip assembly method. Most conventionally assembled packages are quite reliable compared to flip chip packages. But does not allow small form factors when compared to Flip chip assembled packaging method. Flip chips are fabricated on wafer level. However, the flip chip bond pad pitches are smaller and does not match the pitch requirements of current substrate boards. Thus necessitating additional process developments for achieving reliable products. Use of flip chip on mother boards is still in question mark due to sound reliability of the product.

Chip Scale Packages (CSP) have emerged in the recent past to support the product miniaturizations that are in high demand by current consumer markets. However existing manufacturing processes for Chip Scale Packages are mostly single chip assembly type or wafer level chip scale packages that are highly priced. Also the number of Input / Output on CSP are limited and it is becoming difficult to achieve higher I/O count in current CSP manufacturing processes. Therefore developing a high pin count combined with low cost / high performance wafer level package has become a reality today. Many semiconductor industry around the globe are working aggressively in developing these wafer level packages to meet the semiconductor assembly and packaging industry road map requirements.

This invention approach is expected to meet such a requirement of miniaturized product, as it offers high I/O, combined with reduced cost at very small form factor that utilizes lesser board areas in SMT assembly and eliminates the time consuming underfill processes.

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Brief Description of Prior art

Currently few semiconductor industry have developed wafer level package that are said to be under production nature. However, the number of I/O are still less and are limited to few types of applications. Some of the current wafer level packages are described as follows:

1. Fig. 14 is a schematic diagram of a wafer level package using plated copper post method: Here in this method the original interconnect pads with smaller pitch are routed to achieve pitches that can match laminate boards using photolithography techniques. The new metal pads are grown into pillar posts using copper plating methods. The copper post height grown is typically about 100 micron thick. The wafers with copper posts are now molded with a polymeric material and cured. Wafer grinding process is carried out on the front side of the wafer to expose copper posts. Solder bumping is carried out on the copper post and the wafer is said to be fully packaged and ready for SMT assembly operations. Copper post is expected to act as a stress relieving interposer for the thermal stress that is produced during activation of integrated circuit chip.

2. Fig. 15 is a schematic diagram of a wafer level package using an elastomer between solder bump and original silicon wafer interconnect pad, The elastomer acts as a cushion in this package type and absorbs all the thermal stress that is produced during activation of the integrated circuit. This package is considered highly reliable, however, the number of I/O are still limited and depends on the chip size.

Summary of the Invention

In accordance with the Invention, a new wafer level package has been designed for fabrication as follows. For simple functionality test purposes, a daisy chain test chip to be used for package fabrication. The wafer with devices in array form are etched for trenches at the scribe lines. Conductive metal films are deposited on the wafers and patterned to move the original bond pads to the newly created trenches in the wafer. The wafers are then processed with polymer coating on the front side to increase the wafer strength. Back side of the wafer is then ground and etched using appropriate processes to expose the metal that has been deposited in the trenches around the devices. Backside metallization is carried out and patterned to route the edge interconnections as per desired lead / BGA format depending on the application. Solder masking is performed on the metal patterns and interconnect pads exposed after developing the solder mask apertures by photolithography techniques.

The wafers are then diced and individual packaged dies are assembled directly on mother / circuit boards in SMT assembly lines.

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Brief Description of Drawings

The benefits, nature and various features of the invention are to appear fully upon consideration of the illustrative embodiments to be described in detail in connection with the accompanying drawings. In the drawings:

Fig. 1and Fig. 1a shows a general functional wafer showing individual chips separated by scribe Lines (1).

Fig. 2 and Fig.2a shows a formation of trenches (3,4) at the scribe line area by appropriate etching process.

Fig. 3 shows a fully thin film sputtered (5) wafers after the trench formation at the scribe line area.

Fig. 4 shows a cross section of a chip after the metal thin film is patterned (6) and the original pad (2) location shifted to trench pad location (3,4).

Fig. 5 shows a cross section of a passivation layer (7) deposited directly on top of the wafer with metal patterns.

Fig. 6 shows a cross section of wafer that has been molded with polymeric material (8) and cured on top side of the wafer directly above passivated film (7).

Fig. 7 shows a cross section of back grinded / etched (9) wafer to reveal the thin film metal in the trench area (10).

Fig. 8 shows a cross section of a thin conductive metal film (11) sputtered at the back side of wafer after the back grinding operation.

Fig. 9 shows a cross section of thick copper film (12) plated to about 5 – 10 micron thick.

Fig. 10 shows a cross section of patterned metal film (13), which connects the top metal to bottom thin film routing.

Fig. 11 shows a cross section of electroless NiAu deposited metal (14) pattern on the back side of the wafer.

Fig. 12 shows a cross section of solder mask layer (15) on the backside of the wafer after the backside patterning is carried out.

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Fig. 13 shows a cross section of solder mask via (16) that has been opened by photolithography process.

Fig. 14 shows a cross section of dicing (17) process step after the wafer level package has been completed.

Fig. 15 shows a cross section of wafer level package prior art that had been developed by one semiconductor industry.

Fig. 16 shows a cross section of another wafer level package that had been developed by a semiconductor industry.

Detailed Description of the Invention:

Embodiment for the Invention:

Referring to the drawings, Fig. 1 and Fig. 1a is a schematic diagram of a standard wafer with number of functional die arrayed and separated by a scribe line. Fig. 2 and Fig. 2a is a schematic diagram showing about 200 micron deep trenches that are etched at the dicing streets on wafers. Each trench etched corresponds to two adjacent bonding pads of two adjacent die in the silicon wafer. Fig. 3 is a schematic diagram of the wafer that has been sputter deposited on the front top side with Aluminium or any other conductive metal films after trench etching process. Fig. 4 is a schematic diagram showing patterned metal film. Photolithography techniques were used to route the original bonding pad to the trenches at scribe line.

Fig. 5 is a schematic diagram of a passivation layer such as silicon Oxide / Nitride deposited on front top side to protect the thin metal film routed lines. Fig. 6 is a schematic diagram of a polymer epoxy molded on front top side of the wafer directly above the silicon passivation. The polymer epoxy is chosen based on specific device application. Opaque material can be chosen for normal wafers with out any image sensing features. Transparent materials are chosen for applications such as image sensors / MEMS etc. Fig. 7 is a schematic diagram of back grinded wafer (below to 250 micron) using normal backgrinding process to remove excess silicon from the back side of the wafer. Dry etch process is carried out using silicon etch gases by placing the wafers inside the etch chamber and the back side of the wafers are then etched to expose metal film at the trenches that have been deposited.

Fig. 8 is a schematic diagram of wafer sputtered with thin conductive metal films, preferably copper on the backside of the wafer. Appropriate barrier adhesion layers such

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as Ti / Cr / TiW / Ta could be sputtered before the copper films are sputtered. This thin film metal is used as a seed layer for plating a thick copper film of the order of 5 micron on the backside of the wafer. Fig. 9 is a schematic diagram of a thick copper metal film on the back side of the wafer to enable interconnection between front original pad with the back side of the wafer. Fig. 10 is a schematic diagram of a wafer patterned on the backside as per the package interconnect configuration depending on assembly requirements. The patterning could be LGA / BGA / CSP type.

Fig. 11 is a schematic diagram showing electroless NiAu plating on the exposed copper metal patterns to enable further solder bumping process on the wafer backside. Fig. 12 is a schematic diagram of showing solder masking process on the backside of the wafers, by screen printing / spin coating / lamination methods and opening the NiAu plated interconnect pads by lithographic techniques for solder connections. Fig. 13 is a schematic diagram of standard wafer dicing process to separate the individual dies from wafer after the solder masking and pad defining process steps are completed.

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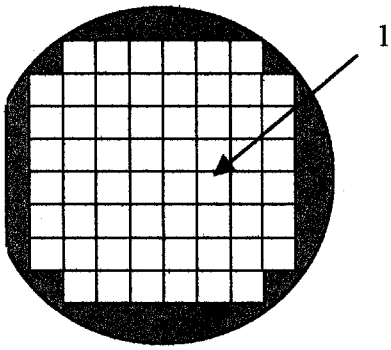


Fig. 1

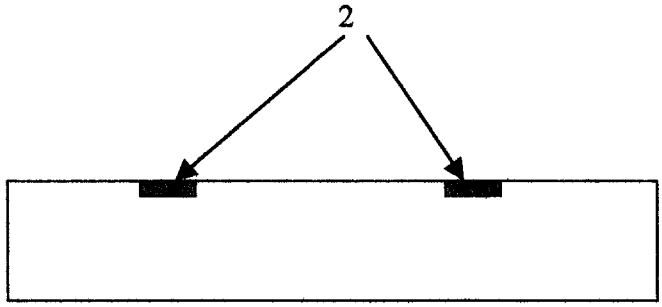


Fig. 1a

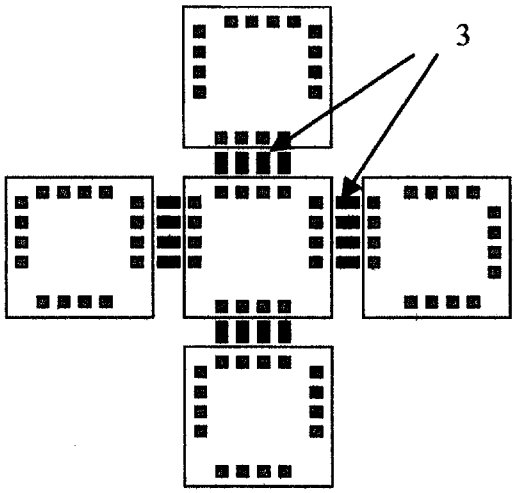


Figure – 2

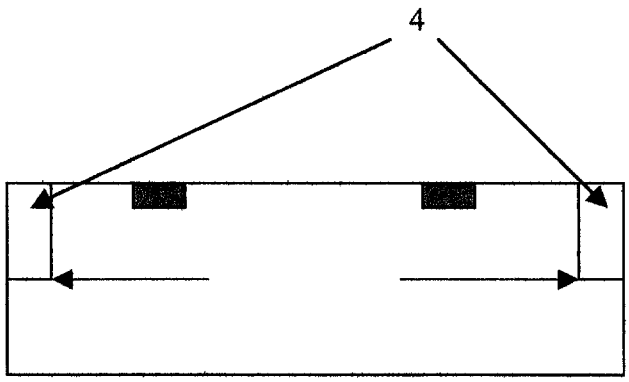


Fig. 2a

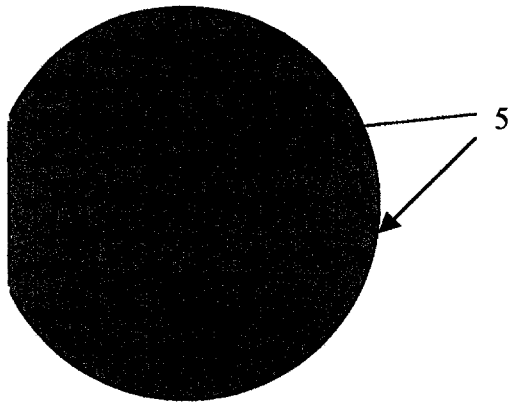


Fig. 3

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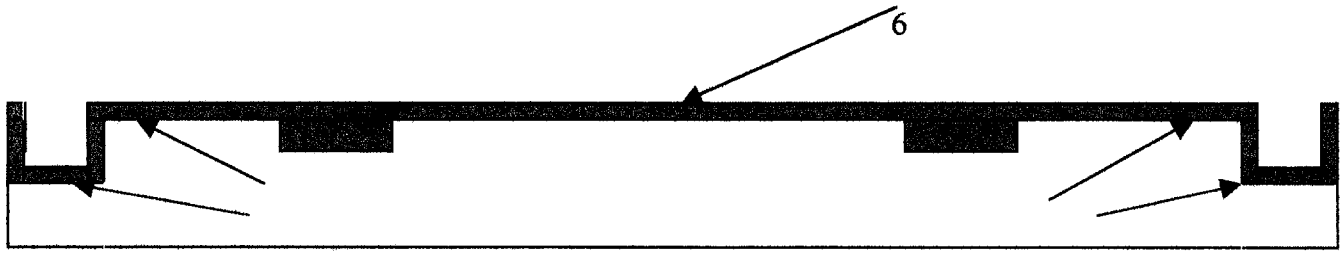


Fig. 4

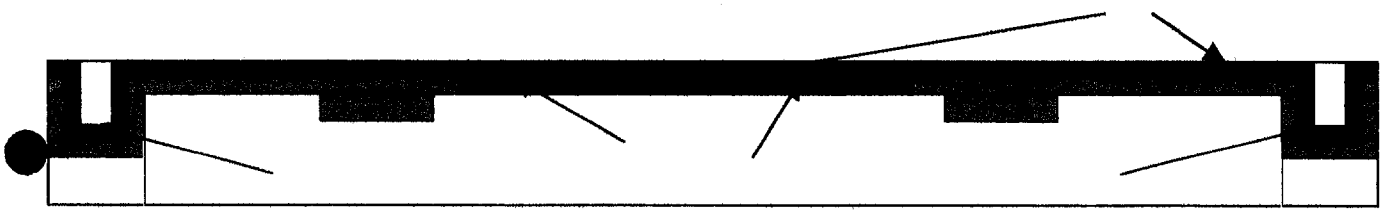


Fig. 5

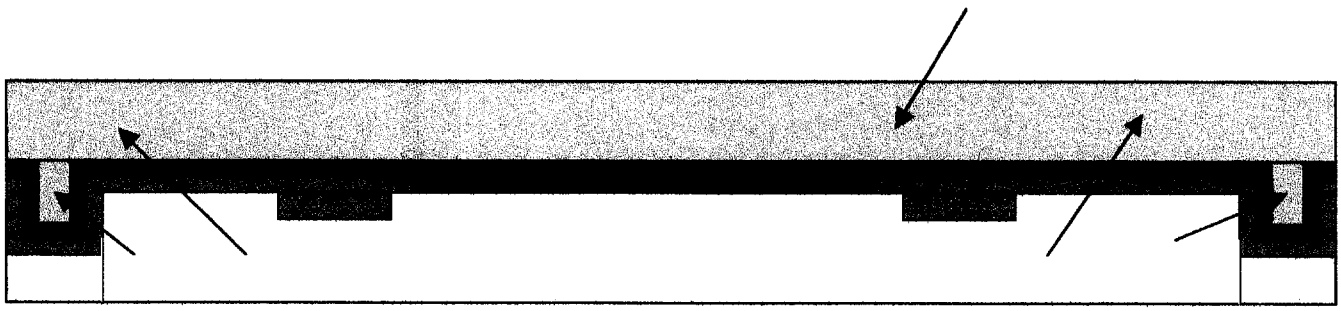


Fig. 6

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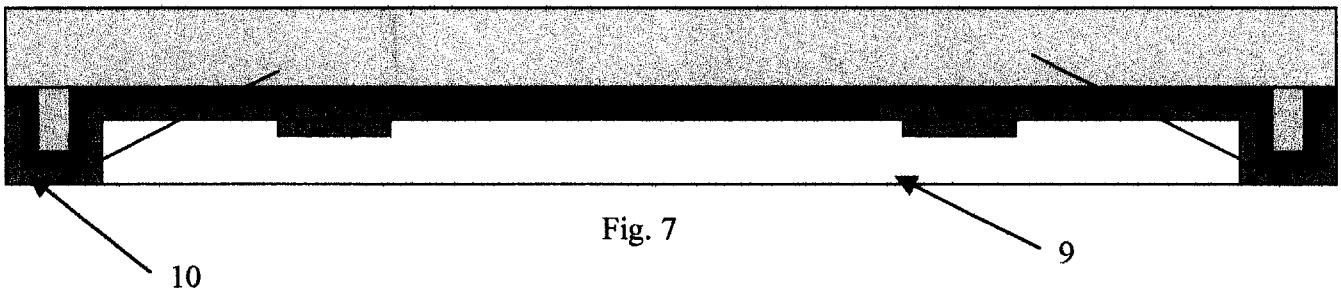


Fig. 7



Fig. 8

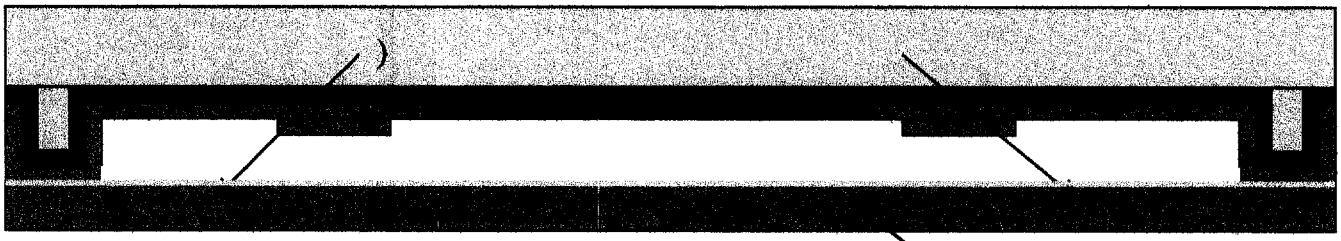


Fig. 9

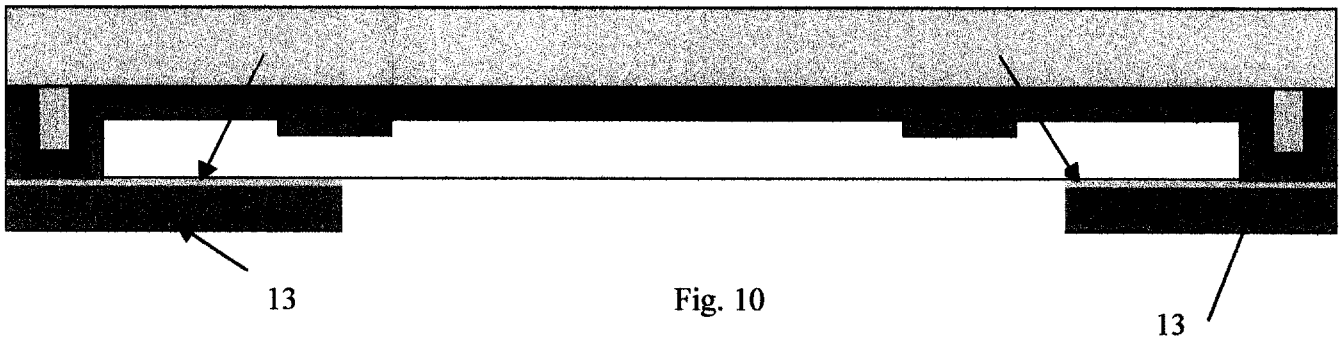


Fig. 10

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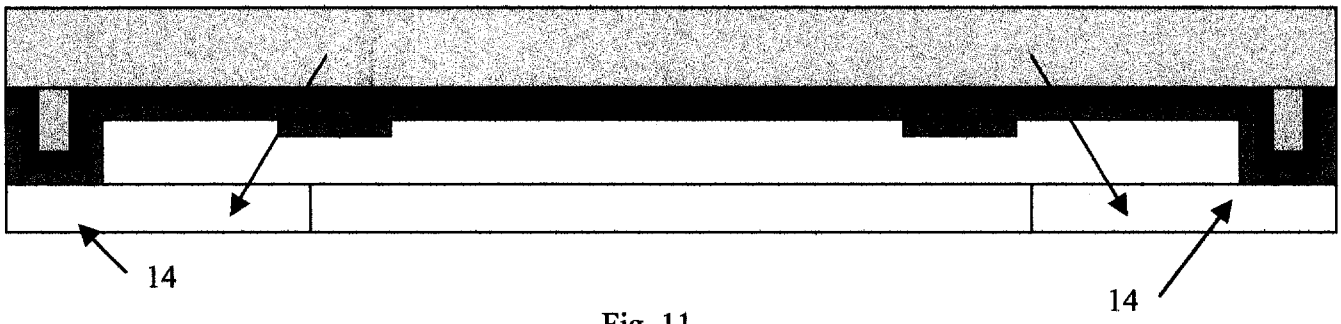


Fig. 11

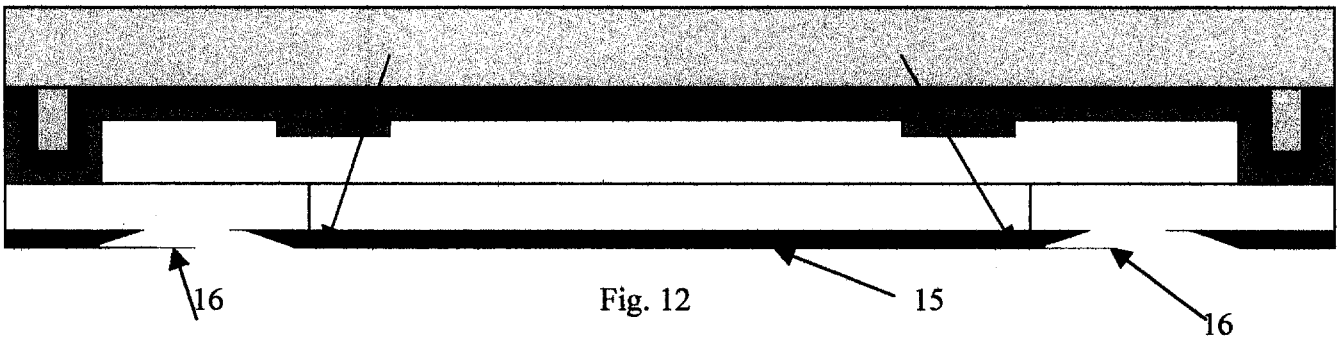


Fig. 12

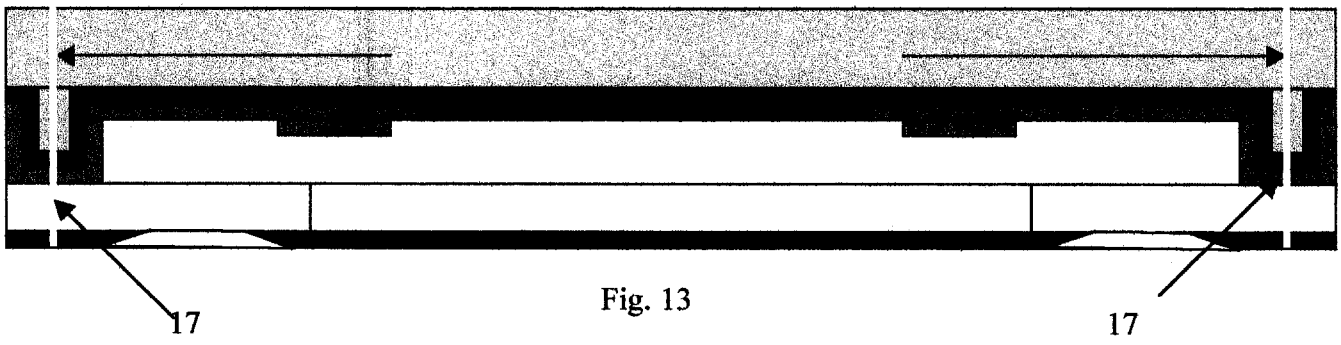


Fig. 13

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Fig. 14

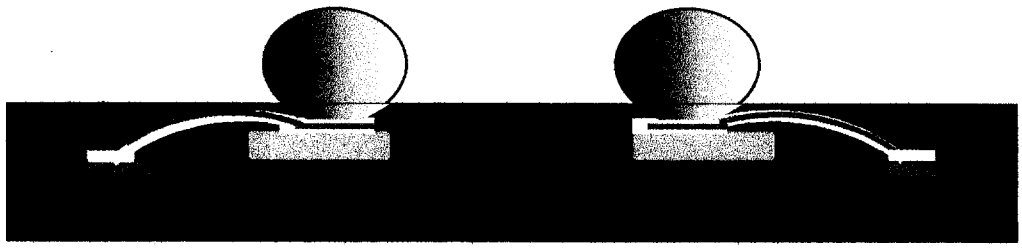


Fig. 15

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CLAIMS:

1. A method for making a wafer level package that provides a high I/O count combined with reduced form factor and low cost have been discussed.

2. The method of invention at 1 above claims trench creation at the scribe lines to a depth of maximum 250 micron.

3. The method of invention at 1 above claims conductive film patterning and routing of original bond pads to trench locations at the scribe lines.

4. The method of invention at 1 above claims conductive film be sputtered / plated / printed type.

5. The method of invention at 1 above claims covering of conductive film patterns and trenches with passivation films to protect the metal lines.

6. The method of invention at 1 above claims deposition of polymeric / elastomer material over the top side passivation.

7. The method of invention at 1 above claims the polymeric / elastomer material be an opaque or transparent in colour.

8. The method of invention at 1 above claims the polymeric / elastomer material deposited either by transfer mold / screen print process.

9. The method of invention at 1 above claims the transparent polymeric / elastomer material be used for image sensor / Optical device packaging.

10. The method of invention at 1 above claims grinding and RIE etch process to expose the metal thin film at the bottom side of the trenches.

11. The method of invention at 1 above claims backside deposition of the conductive metal films to facilitate interconnection.

12. The method of invention at 1 above claims conductive film patterning on the backside of the wafer.

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13. The method of invention at 1 above claims the conductive film patterning at the back side be etched / printed processes.

14. The method of invention at 1 above claims passivation masking and via opening on the back side of the wafer.

15. The method of invention at 1 above claims the back side passivation masking be any films of the insulating proprety.

16. The method of invention at 1 above claims wafer bumping process on the back side of wafer.

17. The method of invention as claimed in step 1 above allows a total package thickness as low as 0.4 mm.

18. The method of invention as claimed in step 1 above allows conductive film routing and bumping on the front top side of the polymeric / elastomer materials.

19. The method of invention as claimed in step 1 above allows wafer level package with high density I/O by way of process at claim 18 above.

20. The method of invention at 1 above claims low cost wafer level package for semiconductor devices including Image sensor / Optical & MEMS devices.

21. The method of invention at 1 above claims full utilization of wafer backside for Interconnect purposes.

22. The method of invention at 1 above claims reduced process steps compared to few other wafer level packaging methods.

23. The method of invention at 1 above claims wafer level package process upto 12 inch dia wafers with out any difficulty.

24. The method of invention at 1 above claims a perfect enclosed package as no silicon is exposed.

25. The method of invention at 1 above claims minimum investment on expensive Flip chip bonders as no flipping of devices are required when assembled to Substrates.

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26. The method of invention at 1 above claims use of standard die bond machines for pick and place action.

27. The method of invention at 1 above claims no underfill material applications at board assembly level as standard CSP pitches are used.

28. The method of invention at 1 above claims minimum deformation / stress related issues for build-up board / BT substrate assemblies as the die undergoes thinning, thereby increasing the resistance to thermal stress.

29. The method of invention at 1 above claims package with more I/O counts.

30. The method of invention at 1 above claims use of commonly available lead free solders for bumping process.

31. The method of invention at 1 above claims process scope for both Aluminium / Gold & Copper chips.

32. The method of invention at 1 above claims MEMS packaging.

33. The method of invention at 1 above claims Optical device packaging.

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