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SELF-ALIGNED DOUBLE-GATE MOSFET BY SELECTIVE EPITAXY AND SILICON WAFER BONDING TECHNIQUES

ABSTRACT

A structure and method of manufacturing a double-gate integrated circuit which includes forming a laminated structure having a channel layer and first insulating layers on each side of the channel layer, forming openings in the laminated structure, forming drain and source regions in the openings, removing portions of the laminated structure to leave a first portion of the channel layer exposed, forming a first gate dielectric layer on the channel layer, forming a first gate electrode (16) on the first gate dielectric layer, removing portions of the laminated structure to leave a second portion of the channel layer exposed, forming a second gate dielectric layer on the channel layer, forming a second gate electrode (22) on the second gate dielectric layer, doping the drain and source regions, using self-aligned ion implantation, wherein the first gate electrode (16) and the second gate electrode (22) are formed independent of each other.

Fig 49



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