

INVERTER BASED (RETURN-TO-ZERO) RZ + NON-RZ (NRZ) SIGNALING

TECHNICAL FIELD

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Embodiments of the invention generally relate to the field of integrated circuits and, more particularly, to systems, methods and apparatuses for inverter based return-to-zero (RZ) + Non-RZ signaling.

10 BACKGROUND

Conventional interfaces typically use either a return-to-zero signaling scheme or a non-return-to-zero signaling scheme. Return-to-zero (RZ) signaling refers to a signaling scheme in which the signal returns to zero between each pulse. The signal returns-to-zero
15 between pulses even if a number of consecutive zeros or ones occur in the signal. Since the signal returns to zero between each pulse, a separate clock signal is, typically, not needed in the RZ signaling scheme.

Non-return-to-zero (NRZ) refers to a signaling scheme in which logic highs are represented by one significant condition and logic lows are represented by another
20 significant condition with no neutral or rest condition. Since the pulses do not have a rest state, a synchronization signal is typically sent alongside the data signal.

Three dimensional (3D) die stacking refers to vertically integrating two or more die with, for example, a dense, high-speed interface. One or more of the stacked die may include a bus for which I/O needs to be performed. The bus may include a number of bit
25 lines and each bit line may have a different length. In conventional systems, bit lines are length matched using, for example, delay buffers. The use of delay buffers to length match the bit lines can significantly increase the complexity of designing a die. Delay buffers may also lower performance by increasing latency (e.g., due to inverters in the signal path).

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BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments of the invention are illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings in which like reference

numerals refer to similar elements.

Figure 1 is a high-level block diagram illustrating selected aspects of an embodiment of the invention.

5 **Figure 2** is a block diagram illustrating selected aspects of an interface circuit implemented according to an embodiment of the invention.

Figures 3A and 3B illustrate signal waveforms of an interface circuit implemented according to an embodiment of the invention.

Figure 4 is a circuit diagram of selected aspects of an interface circuit implemented according to an embodiment of the invention.

10 **Figure 5** is a circuit diagram of selected aspects of an interface circuit implemented according to an embodiment of the invention.

Figure 6 is a circuit diagram of selected aspects of an interface circuit using tri-state drivers and receivers according to an embodiment of the invention.

15 **Figure 7** is a circuit diagram of a tri-state driver implemented according to an embodiment of the invention.

Figure 8 is a circuit diagram of a $V_{cc}/2$ reference circuit (part of receiver circuitry) implemented according to an embodiment of the invention.

Figure 9 illustrates waveforms provided by an interface circuit (e.g., part of a driver) implemented according to an embodiment of the invention.

20 **Figure 10** is a cross-sectional view of a semiconductor device, implemented according to an embodiment of the invention.

DETAILED DESCRIPTION

Embodiments of the invention are generally directed to systems, methods, and apparatuses for a signaling scheme that implements a weighted NRZ + RZ signal. The
25 weighted NRZ + RZ signal may be driven, for example, on inter-die and/or intra-die interconnects. The signaling scheme may be effective in decreasing the latency of signal

propagation on the line. In some embodiments, the signal latency can be made to approach the flight time of the line.

FIG. 1 is a high-level block diagram illustrating selected aspects of a device 100 implemented according to an embodiment of the invention. Device 100 may include die 102 that communicates with die 104 through interfaces 106. In some embodiments, interfaces 106 use a signaling scheme that is a weighted sum of the corresponding NRZ and RZ waveforms on the interconnect (e.g. on vias 108). As is further discussed below, with reference to FIGs. 2-10, the signaling scheme employed by interfaces 106 may support configurable edges and/or configurable swing voltages for signals transmitted on the interconnect (e.g., on vias 108). Such a signaling scheme is particularly useful when it is important to match the delays on wires that are dissimilarly routed.

Interfaces 106 may communicate with each other using an interconnect that may include one or more die-to-die vias 108. Vias 108 may be electrically conductive to allow electrical signals to pass between dies 102 and 104. Vias 108 may be constructed with material such as aluminum, copper, silver, gold, combinations thereof, or other electrically conductive material.

Dies 102 and 104 may include circuitry corresponding to various components of a computing system. For example, die 102 may include a memory device and die 104 may include one or more processing cores and/or shared or private caches. In some embodiments, dies 102 and 104 may overlap partially. In other embodiments, dies 102 and 104 may overlap fully or not at all. Accordingly, dies 102 and 104 may have a three-dimensional (3D) stacking configuration. Such a configuration may provide for utilization of disparate process technologies. For example, dies 102 and 104 may be bonded after alignment of the vias 108. Also, a 3D configuration may provide for a higher density when packaging semiconductor devices. A 3D configuration may also enable more efficient system-on-chip or system-on-stack (SOS) solutions for computing devices or systems. Furthermore, even though FIG. 1 only illustrates two dies, additional dies may be used to integrate other components into the same device.

FIG. 2 is a block diagram illustrating selected aspects of an interface circuit, implemented according to an embodiment of the invention. Circuit 200 illustrates selected portions of a driver 202 and a receiver 204 suitable for inter-chip and/or intra-chip

communication according to an embodiment of the invention. For ease of description, only a single instance of a driver and/or a receiver are shown. It is to be appreciated, however, that an interface (e.g., interface 106, shown in FIG. 1) may include nearly any number of drivers and/or receivers. In addition, each driver and/or receiver may include
5 more elements, fewer elements, and/or different elements than those shown in FIG. 2.

In the illustrated embodiment, driver 202 includes edge detect circuitry 206 (e.g., short pulse generator with selectable pulse width) and driver circuitry 208. Edge detect circuitry 206 receives, as an input a data signal and provides short pulses when it detects a positive / negative going data transition. Component 214 receives an inverted data signal
10 and its output is used to modulate swing and edge rate of a leading edge signal, whereas component 212 receives a data signal in true polarity and its output is used to modulate the swing and edge rate of trailing edge signal. In an alternative embodiment, detect circuitry 206 may include more elements, fewer elements, and/or different elements.

In some embodiments, driver circuitry 208 includes a plurality of drivers having
15 outputs that are coupled together (e.g., in parallel). The plurality of drivers may be used to selectively adjust the amount of driver current provided by driver 202. For example, during a first portion of a transmission cycle, driver circuitry 208 may provide a first level of driver current. Similarly, during a second portion of the transmission cycle, driver circuitry 208 may provide a second level of driver current. The first level of driver current
20 may be greater than the second level to ensure that receiver 204 is tripped. The ability to selectively control the amount of driver current enables driver 202 to employ the weighted sum of the NRZ and RZ waveforms on the line.

In some embodiments, the selective control of driver current enables driver 202 to modulate the edge rate of a transmitted signal. For example, the edge of a transmitted
25 signal can be increased by increasing the driver current (e.g., by activating more drivers). Similarly, the edge rate of a transmitted signal can be decreased by decreasing the driver current. In some embodiments, the edge rate may be relatively large (e.g., approaching full strength) during a first (e.g., initial) portion of a transmission cycle and then may be reduced during a second portion of the transmission cycle.

In some embodiments, the selective control of driver current enables driver 202 to modulate the voltage swing of a transmitted signal. For example, the voltage swing of a
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transmitted signal can be increased by increasing the driver current (e.g., by activating more drivers). Similarly, the voltage swing of a transmitted signal can be decreased by decreasing the driver current. In some embodiments, the voltage swing may be relatively large (e.g., approaching the rail voltage) during a first (e.g., initial) portion of a transmission cycle and then may be reduced during a second portion of the transmission cycle.

In some embodiments, all of the drivers and receivers are tuned to the same settings (in terms of voltage and/or edge rates) via scan. This enables the driver to oscillate very closely to the trip point of the receiving device (e.g., V_t of the transistor) at $V_{cc}/2$ (~0.5 V or so). For example, in some embodiments, the driver only has to increase the voltage on the transmission line by 0.2V to switch the device ($0.7V - 0.5V = 0.2V$ versus 0.7V for full rail-to-rail switching). Increasing the line voltage by 0.2V is significantly faster than increasing it by 0.7V and thus reduces the effect of line length. It also reduces the strength of the required driver. In alternative embodiments, each driver/receiver pair may be independently tuned.

FIGs. 3A and 3B illustrate the use of a weighted sum signal according to an embodiment of the invention. Waveforms 302 and 304 respectfully illustrate idealized NRZ and RZ waveforms for a bit sequence that includes 01101. Waveform 306 illustrates the line $W(t) = a.W_{NRZ}(t) + b.W_{RZ}(t)$ as constructed from waveforms 302 and 304. In some embodiments, $W(t)$ is centered on the trip-point of an inverter (e.g., an inverter in receiver 204). The $W(t)$ waveform exhibits some properties that are different than those provided by either the NRZ or the RZ waveforms. For example, unlike the RZ waveform, the $W(t)$ waveform can be recovered using an inverter. Also, since $W(t)$ starts close to the trip-point of an inverter a substantial portion of the RC delay of the line is removed. Since the actual delay of the line is the sum of the flight time and the RC component, the delay can be made to approach the flight time of the line.

FIG. 3B illustrates actual waveforms corresponding to idealized waveforms 302 and 306. In particular, waveform 308 corresponds to NRZ waveform 302 and waveform 310 corresponds to $W(t)$ waveform 306. The waveforms shown in FIG. 3B are referred to as “actual” waveforms because they represent the way waveforms generated from CMOS circuits are likely to appear.

FIG. 4 is a circuit diagram of an idealized embodiment of a driver according to an embodiment of the invention. Circuit 400 generates $W(t)$ by sequencing four switches (402) between V_{cc} , V_{ss} , $V_{split}/2$. The four switches (402) may be sequenced around the midpoint of interconnect 404.

FIG. 5 is a circuit diagram of an alternative embodiment of a driver implemented according to an embodiment of the invention. Unlike circuit 400, circuit 500 does not have a power supply to generate V_{split} . Instead, the intermediate swings are generated by the thevenin equivalent source of $(V_{cc}/2) * R_2 / (R_1 + R_2)$.

FIG. 6 is a circuit diagram of an embodiment of driver circuitry using tri-state drivers, according to an embodiment of the invention. Circuit 600 uses weak tri-state drivers 602 to replace the resistor, R_2 , which is used in circuit 500 (shown in FIG. 5). The number of active tri-state drivers may be modulated to generate $W(t)$. In some embodiments, the modulation of the number of active tri-state drivers enables circuit 600 to modify the edge rate of $W(t)$ and/or to modify the voltage swing of $W(t)$. The modulation of the number of active tri-state drivers also enables circuit 600 to use a signaling scheme based on the weighted NZ and NRZ representations of the signal to be transmitted on the interconnect.

FIG. 7 is a circuit diagram of a tri-state driver implemented according to an embodiment of the invention. Driver 700 may be one of a plurality of drivers used in the driver circuitry (e.g., driver circuitry 208, shown in FIG. 2). For example, driver 700 may be any of the tri-state drivers shown in circuit 600 of FIG. 6. In some embodiments, the smallest (or weakest) tri-state driver (e.g., 602-1) may be one instance of Driver 700. Successively larger (or stronger) tri-state drivers (e.g., 602-2 and 602-3) may include multiple instances (e.g., 2, 4, ..., N) of driver 700 coupled in parallel.

Driver 700 receives as an input a data signal and one more or more modified edge signals. For example, in the illustrated embodiment, driver 700 receives data signal 702, and edge detect signals 704 and 706. In alternative embodiments, driver 700 may receive a different number of modified edge signals (e.g., 1, 3, 4, ..., etc.). The output of driver 708 (e.g., the signal duration of the output) is based, at least in part, on modified edge signals 704 and 706. In addition, the output of driver 708 may be based on one or more control bits that determine whether a particular instance of driver 700 is active.

FIG. 8 is a circuit diagram of a $V_{cc}/2$ reference circuit implemented according to an embodiment of the invention. In some embodiments, circuit 800 is used to provide a reference voltage (e.g., V_T) to a receiver (e.g., receiver 204, shown in FIG. 2). In such an embodiment, the amplitude difference between a logic 0 and a logic 1 can be reduced because the threshold voltage of the receiver is tied to $V_{cc}/2$. In alternative embodiments of the invention, a different circuit may be used to provide a reference voltage to the receiver.

FIG. 9 illustrates waveforms provided by an interface circuit implemented according to an embodiment of the invention. Reference number 902 illustrates that, in some embodiments, the edge rate of a signal transmitted from an interface is modifiable. In some embodiments, the edge rate is modified based on the number of drivers (e.g., drivers 208, shown in FIG. 2) that are currently active. In alternative embodiments, a different mechanism may be used to modify the edge rate of a transmitted signal.

Referring to reference number 904, in some embodiments, the voltage swing of a signal transmitted from an interface is modifiable. In some embodiments, the voltage swing is modified by dynamically changing the number of drivers that are currently active. In alternative embodiments, a different mechanism may be used to modify the edge rate of a transmitted signal.

Fig. 10 illustrates a cross-sectional view of a semiconductor device 1000 in accordance with an embodiment of the invention. Device 1000 may include a package 1002, die 1028, die 1030, and die-to-die vias 1026. One or more bumps 1004-1 through 1004-N (collectively referred to herein as “bumps 1004”) may allow electrical signals including power, ground, clock, and/or input/output (I/O) signals to pass between the package 1002 and the die 1028. As shown in Fig. 2, the die 1028 may include one or more through-die vias 1006 to pass signals between the bumps 1004 and the die 1030. The device 1000 may further include a heat sink 1008 to allow for dissipation of generated heat by the die 1030 and/or device 1000.

As illustrated in Fig. 2, dies 1028 and 1030 may include various layers. For example, die 1028 may include a bulk silicon (SI) layer 1010, an active Si layer 1012, and a metal stack 1014. Die 1030 may include a metal stack 1020, an active Si layer 1022, and a bulk Si layer 1024. As shown in Fig. 2, the vias 1026 may communicate with the dies

1028 and 1030 through the metal stacks 1014 and 1020, respectively. In an embodiment, die 1028 may be thinner than die 1030. For example, die 1028 may include a memory device (such as a random access memory device) and die 1030 may include one or more processor cores and/or shared or private caches. As with device 100 of Fig. 1, device 1000
5 may include additional dies, e.g., to integrate other components into the same device or system. In such an embodiment, die-to-die and/or through-die vias may be used to communicate signals between the various dies (e.g., such as discussed with respect to the vias 1026 and 1006).

Elements of embodiments of the present invention may also be provided as a
10 machine-readable medium for storing the machine-executable instructions. The machine-readable medium may include, but is not limited to, flash memory, optical disks, compact disks-read only memory (CD-ROM), digital versatile/video disks (DVD) ROM, random access memory (RAM), erasable programmable read-only memory (EPROM), electrically erasable programmable read-only memory (EEPROM), magnetic or optical cards,
15 propagation media or other type of machine-readable media suitable for storing electronic instructions. For example, embodiments of the invention may be downloaded as a computer program which may be transferred from a remote computer (e.g., a server) to a requesting computer (e.g., a client) by way of data signals embodied in a carrier wave or other propagation medium via a communication link (e.g., a modem or network
20 connection).

It should be appreciated that reference throughout this specification to “one embodiment” or “an embodiment” means that a particular feature, structure or characteristic described in connection with the embodiment is included in at least one embodiment of the present invention. Therefore, it is emphasized and should be
25 appreciated that two or more references to “an embodiment” or “one embodiment” or “an alternative embodiment” in various portions of this specification are not necessarily all referring to the same embodiment. Furthermore, the particular features, structures or characteristics may be combined as suitable in one or more embodiments of the invention.

Similarly, it should be appreciated that in the foregoing description of
30 embodiments of the invention, various features are sometimes grouped together in a single embodiment, figure, or description thereof for the purpose of streamlining the disclosure

aiding in the understanding of one or more of the various inventive aspects. This method of disclosure, however, is not to be interpreted as reflecting an intention that the claimed subject matter requires more features than are expressly recited in each claim. Rather, as the following claims reflect, inventive aspects lie in less than all features of a single
5 foregoing disclosed embodiment. Thus, the claims following the detailed description are hereby expressly incorporated into this detailed description.

CLAIMS

What is claimed is:

1. A circuit comprising:
edge detect circuitry to provide a short pulse at a rising and a falling edge of a data
5 signal; and
driver circuitry to receive the data signal and the short pulse and to provide a
weighted sum signal, wherein the weighted sum signal is a weighted sum of the return-to-
zero (RZ) and the non-RZ (NRZ) components of the data signal.
2. The circuit of claim 1, wherein the driver circuitry comprises a plurality of drivers
10 and further wherein an edge rate of the weighed sum signal is selectively determined
based, at least in part, on a number of the plurality of drivers that are turned on.
3. The circuit of claim 2, wherein the driver circuitry includes edge rate configuration
circuitry to configure, at least in part, an edge rate of the weighted sum signal.
4. The circuit of claim 1, wherein the driver circuitry comprises a plurality of drivers
15 and further wherein a voltage swing of the weighed sum signal is selectively determined
based, at least in part, on a number of the plurality of drivers that are turned on.
5. The circuit of claim 4, wherein the driver circuitry includes voltage swing
configuration circuitry to configure, at least in part, a voltage swing of the weighted sum
signal.
- 20 6. The circuit of claim 4, wherein at least some of the plurality of drivers are tri-state
drivers.
7. The circuit of claim 1, wherein during a first portion of a signal transmission cycle,
the driver circuitry provides maximum driver current and during a second portion of the
signal transmission cycle, the driver circuitry provides less than the maximum driver
25 current.
8. The circuit of claim 7, wherein the driver circuitry includes a plurality of drivers
and further wherein at least some of the drivers are tri-state drivers.
9. The circuit of claim 8, wherein a number N of the plurality of drivers are on during

the first portion of the signal transmission cycle and a number M of the plurality of drivers are on during the second portion of the signal transmission cycle and wherein N is greater than M.

10. An interface circuit comprising:

5 edge detect circuitry to provide a short pulse at a rising and a falling edge of a data signal

driver circuitry to receive the data signal and the short pulse as inputs and to provide a weighted sum signal as an input, the driver circuitry including a plurality of drivers, wherein an edge rate of the weighted sum signal is selectively determined based, 10 at least in part, on a number of the plurality of drivers that are turned on.

11. The interface circuit of claim 10, wherein the weighted sum signal comprises a weighted return-to-zero (RZ) + non-RZ (NRZ) signal.

12. The interface circuit of claim 10, wherein the driver circuitry includes voltage swing configuration circuitry to configure, at least in part, the voltage swing of the 15 weighted sum signal.

13. The interface circuit of claim 10, wherein a voltage swing of the weighted sum signal is selectively determined based, at least in part, on a number of the plurality of drivers that are turned on.

14. The interface circuit of claim 10, wherein at least some of the plurality of drivers 20 are tri-state drivers.

15. An interface circuit comprising:

edge detect circuitry to provide a short pulse at a rising and a falling edge of a data signal

driver circuitry to receive the data signal and the short pulse as inputs and to 25 provide a weighted sum signal as an input, the driver circuitry including a plurality of drivers, wherein a voltage swing of the weighted sum signal is selectively determined based, at least in part, on a number of the plurality of drivers that are turned on.

16. The interface circuit of claim 15, wherein the weighted sum signal comprises a weighted return-to-zero (RZ) + non-RZ (NRZ) signal.

17. The interface circuit of claim 15, wherein the driver circuitry includes voltage swing configuration circuitry to configure, at least in part, the voltage swing of the weighted sum signal.
18. The interface circuit of claim 15, wherein an edge rate of the weighted sum signal is selectively determined based, at least in part, on a number of the plurality of drivers that are turned on.
19. The interface circuit of claim 15, wherein at least some of the plurality of drivers are tri-state drivers.
20. A system comprising:
a first die having an interface circuit, the interface circuit including edge detect circuitry to provide a short pulse at a rising and a falling edge of a data signal, and driver circuitry to receive the data signal and the short pulse and to provide a weighted sum signal, wherein the weighted sum signal is a weighted sum of the return-to-zero (RZ) and the non-RZ (NRZ) components of the data signal; and
a second die stacked on the first die, wherein the second die includes an interface circuit having a receiver to receive the weighted sum signal from the first die.
21. The system of claim 20, further comprising:
an interconnect coupled between the interface circuit of the first die and the interface circuit of the second die.
22. The system of claim 20, wherein a reference voltage of the receiver is substantially equal to $V_{cc}/2$.
23. The system of claim 20, wherein the driver circuitry comprises a plurality of drivers and further wherein an edge rate of the weighted sum signal is selectively determined based, at least in part, on a number of the plurality of drivers that are turned on.
24. The system of claim 23, wherein the driver circuitry includes edge rate configuration circuitry to configure, at least in part, an edge rate of the weighted sum signal.

25. The system of claim 20, wherein the driver circuitry comprises a plurality of drivers and further wherein a voltage swing of the weighted sum signal is selectively determined based, at least in part, on a number of the plurality of drivers that are turned on.

5 26. The system of claim 23, wherein the driver circuitry includes voltage swing configuration circuitry to configure, at least in part, a voltage swing of the weighted sum signal.

27. The system of claim 20, wherein during a first portion of a signal transmission cycle, the driver circuitry provides maximum driver current and during a second portion of
10 the signal transmission cycle, the driver circuitry provides less than the maximum driver current.

28. The system of claim 27, wherein a number N of the plurality of drivers are on during the first portion of the signal transmission cycle and a number M of the plurality of drivers are on during the second portion of the signal transmission cycle and wherein N is
15 greater than M.