a first gate electrode having a laminated structure of a metal film and a polysilicon film, both of which are formed around the gate insulating film;

a gate insulating film formed around the second pillar-shaped silicon layer;

a second gate electrode having a laminated structure of a metal film and a polysilicon film, both of which are formed around the gate insulating film;

a gate line connected to the first and second gate electrodes, wherein a center line of the gate line is displaced by a predetermined distance from a imaginary line joining a center point of the first pillar-shaped silicon layer to a center point of the second pillar-shaped silicon layer; and wherein the thickness of each of the polysilicon films being smaller than half of a distance between the first pillar-shaped silicon layer and the second pillar-shaped silicon layer so that a portion of the gate line between the first and second pillar-shaped silicon layers also mutually connects the first and second gate electrodes;

an upper surface of the gate line being located at a lower position than upper surfaces of the first and second gate electrodes;

a first n-type diffusion layer formed in an upper portion of the first pillar-shaped silicon layer;

a second n-type diffusion layer formed in a lower portion of the first pillar-shaped silicon layer and in an upper portion of the planar silicon layer;

a first p-type diffusion layer formed in an upper portion of the second pillar-shaped silicon layer; and

a second p-type diffusion layer formed in a lower portion of the second pillar-shaped silicon layer and in an upper portion of the planar silicon layer.

8. The semiconductor device according to claim ~~6~~7, wherein the gate line has a laminated structure of the metal film and a silicide.

9. The semiconductor device according to claim ~~6~~7, wherein the thickness of the insulating film sidewall formed on a side wall of the first n-type diffusion layer is larger than the sum of the thicknesses of the metal film and polysilicon film.