SELECTIVE CONNECTION IN IC PACKAGING

The field of the invention is that of packaging integrated circuits, in particular the connection technology referred to as "flip-chip" or C4.

In the process of fabricating substrates for connecting sets of integrated circuits, (ICs) manufacturers sometimes have occasion to make selected contacts with the solder bump connections on the bottom of an integrated circuit. For example, there may be a set of similar products that have different connections to a standard chip, so that the kth bump on the chip is used with some packages and not used with others.

In the past, as shown in Fig. 3 in cross section, a chip 10 having a ball grid array of solder bump (or ball) contacts 30 (referred to as "flip chip" technology or as C4 technology) would all be soldered to metal contact pads 110 in a corresponding contact array on the top surface 135 of the substrate. In that case, the chip would have to be designed and manufactured with only those contacts that were used. U.S. Patent 6,229,219 illustrates different chips with irregular sets of contacts on the bottom. All of the contacts on each chip are bonded to corresponding contacts on the package. The package accommodates two different chips by having empty locations on the chip - i.e. a chip has an empty location at the kth slot on that chip so there is no bond formed between the contact at the kth location and the empty slot on the chip.

Alternatively, a chip would be bonded to a contact on the package, but contacts that were not used would be "floating", i.e. not connected to further layers of the package. This meant that there was potential for such contacts pads 110 to short out to other contacts. Additionally, the metal on the substrate represented capacitance that might affect the operation of the chip.

Removing the contact on the bottom of the chip would cost money for different masks in forming the chip contacts. Removing the contact after the chip is formed would require extra handling, with the possibility of damaging the chip. Removing the contact pad 110 at that location was a possibility, but there was a chance that the solder bump 30 would flow to short out an adjacent contact, or a via that had been fabricated below the contact pad 110, even with the presence of solder mask 130, a conventional dielectric layer that is deposited and patterned photolithographically. The solder mask in this prior art view is shown as separating the solder

bumps 30 and the corresponding metal contact pads 110 that the solder bumps make contact with, as is conventional.

The present invention provides a substrate as claimed in claim 1. Preferred features are recited in the dependent claims.

Preferably, the invention isolates unused solder bumps on the bottom of an IC by patterning the metal interconnect on the top surface of the substrate, together with the solder mask, to isolate the unused solder bumps.

A preferred feature of the invention is changing the shape of a metal interconnect passing under an unused chip contact to form a depression in the dielectric solder mask to lower the height of the solder mask at the selected location.

Another preferred feature of the invention is patterning the solder mask to place a layer of dielectric between a contact on a chip and a corresponding contact on the package.

Figure 1 shows a top view of a structure according to the invention.

Figure 2 shows a cross section through the view of Figure 1.

Figure 3 shows a prior art cross section corresponding to Figure 2.

Referring again to Fig. 3, there is shown a cross section of a portion of an IC packaging substrate, in which chip 10 is connected to the package through a set of C4 solder bumps or balls 30 that bond to an array of metal contact pads 110. The contact pads are connected to interconnects that extend down through top surface 135 of the substrate and connect the chip 10 to other chips and/or to the outside world. Solder mask 130 is a dielectric layer that is put down after the conductors on the top surface has been patterned and before the chips are bonded. It isolates the solder bumps 30 by surrounding the contact pads 110.

Solder mask 130 is put down as a photo-sensitive liquid or film after the metal layer of contact pads 110 has been patterned, and then patterned by exposure to light of the appropriate characteristic and then developed after patterning. As can be seen in Fig. 3, the standard way of patterning a solder mask is as a separation and isolation feature between

the solder bumps, forming a wall around each contact pad 110. In the cross section of Fig. 3, none of the solder balls are shorted together by metal 110. If any were, i.e. if the metal 110 extended between the contacts, layer 30 would be slightly higher where it passes over a layer of metal 110.

A feature of the prior art technique is that modification of the IC pinout (or connections to the solder bumps) is expensive, so that cost considerations dictate that the solder bump-contact 110 connection remain. That, in turn, means that the solder ball attached to chip 10 is soldered to the contact pad 110 on the surface and therefore that there may be problems with capacitance added to the chips by the effect of connections on the substrate. Those skilled in the art are aware that a contact pad 110 is typically connected to a via extending downward through the substrate, so that there is a significant amount of area in electrical contact with the solder ball 30.

According to the invention, the arrangement of the IC is unchanged, but accommodation to different connections on the substrate is made by isolating the unused solder bumps on the chip by a patterned dielectric that does not interfere with chip operation.

Referring now to Figure 1, there is shown a plan view of an area of a package substrate according to the invention, in which a 3x7 array of contact pads 110 conforms to the standard I/O of a particular IC. Not all of the contacts are used, however. In this example, two contacts in the middle row are not used.

A heavy line 120 passing from left to right along the middle row of the array represents a conductive interconnect that is required according to the system being implemented (connecting contacts 1, 3, 4, 6 and 7). The line passes through seven contiguous contact locations in this example. Two contact locations are not used in this example, however, both denoted by numeral 122 and located in an area of line 120 having the shape of a hexagon. The function of the layout shown is that the conductive interconnect member 120 is displaced from the location of the solder bumps on chip 10; i.e. it splits, defining a hexagonal opening between the two sides. The solder mask that will be put down before the chip bonding operation fills the hexagonal opening and forms a depression in the top surface of the solder mask layer 125 at that location. That depression surrounds the solder ball on the chip 10 and isolates it from surrounding connectors, so that any conductive material turning to the

molten state during the heating and solder reflow process is confined. In the bonding operation, the solder balls 30 on the bottom of chip 10 will change shape, lowering chip 10 slightly. The dielectric material 125 located between ball 30 and contact pad 110 prevents an electrical path from forming. Thus, the connections on the lower face of IC 10 are not disturbed, but the unused connections do not affect the substrate connections (e.g. by causing unwanted shorts) or the operations of the chip (by changing capacitance).

Looking at the side view in Fig. 2, the section 2-2 is taken past the interconnect 120, so it does not show in the cross section, i.e. the line is labeled 120 where it passes through pad 110 and 122 where it passes through hexagon 122. The two thin lines of hexagons 122 are in the plane of the cross section. Thus, in Fig. 2, both areas 125 show a bump on each side, where the solder mask goes over the interconnect 122.

At the top row of Fig. 1, box 124 defines an area around a contact location that will enclose a dielectric pad 125, formed from the solder mask material. This pad prevents a path from being formed between the contact 110 at that location and the chip contact above the location. This arrangement is useful for a situation in which there is a contact on the chip that is not used in this particular system and a contact in the substrate that does connect or may short to another interconnect on or in the substrate.

Thus, a broader class of chips and/or substrates may be used with the invention, since a stock substrate having a contact 110 connected to other wires in the substrate that would increase the capacitive loading on the circuit in the chip (if contact were made) can still be used. Similarly, an interconnect in the substrate that shorts chip contacts K and L in one version of a system may be blocked, so that a system that does not have that short can still use the same substrate.

Those skilled in the art will be aware that having a closed hexagon is not required and that a single-sided structure would also do to preserve the continuity of line 120. The line 120 does not have to be a straight line and it may have a right angle or other shape. A diamond shape, rectangle, parallelogram or other shape (preferably a closed curve) could be used instead of the hexagon.

Preferably, the thickness of the solder mask is thick enough to prevent electrical contact and thin enough that it does not prevent the

other solder bumps from making contact with the pads 110 that the bond to. Some tolerance is permissible, as the solder bumps will flow during the bonding process. The invention has been described in the context of the flip chip process developed by IBM, but other technologies in which a set of contacts on the bottom of an IC are bonded to an array on the top of the substrate could also be used.

CLAIMS

1. A substrate for connecting integrated circuits (10) having a substrate top surface (135) with a standard-pattern array of contacts (110) formed thereon and a patterned dielectric layer (130) disposed on said top surface (135), said patterned dielectric layer (130) being patterned to surround and isolate from one another a subset of said array of contacts in which a conductive contact interconnect member (120) is disposed on said top surface and electrically connecting at least some of said array of contacts, said contact interconnect member (120) being displaced from a selected location of the contact locations in said array, and said patterned dielectric layer covers said selected location, wherein an integrated circuit contact at said selected location of said top surface is insulated from a contact, of said array of contacts, located at said selected location.

2. A substrate according to claim 1, in which said contact interconnect member (120) is displaced from said selected location in a closed curve (122) surrounding said selected location, wherein said dielectric layer has a depression within said closed curve at said selected location.

3. A substrate according to claim 1, in which said conductive interconnect member (120) extends past at least one non-connected contact to which it is not connected.

4. A substrate according to claim 3, in which said conductive interconnect member forms a closed curve surrounding said at least one non-connected contact.

5. A substrate according to claim 4, in which said conductive interconnect member forms a hexagon surrounding said at least one non-connected contact.