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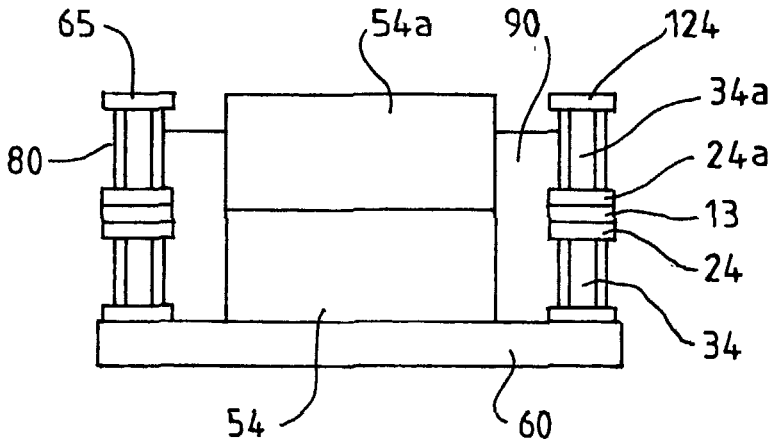
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(54) Title: AN INTERMEDIATE MANUFACTURE FOR A DUAL GATE LOGIC DEVICE



(57) Abstract: The present invention features double-or dual-gate logic devices that contain gate conductors that are consistently self-aligned and that have channels that are of constant width. The inventive process also provides a method of selectively etching germanium-containing gate conductor materials without significantly etching the adjacent silicon channel material. In this manner, the gate conductor can be encased in a dielectric shell without changing the length of the silicon channel. A single-crystal silicon wafer is utilized as the channel material. Pillars or stacks of self aligned dual gate MOSFETs are generated by etching, via the juxtaposition of overlapping germanium-containing gate conductor regions. Vertically etching through regions of both gate conducting material and dielectric insulating material provides an essentially perfect, self-aligned dual gate stack. A process is described wherein the gate conductor material can be selectively etched without etching the channel material.

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