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(21) International Application Number: ✓ PCT/US98/00843 (22) International Filing Date: ✓ 19 January 1998 (19.01.98) (30) Priority Data: 08/787,627 ✓ 23 January 1997 (23.01.97) ✓ US (71) Applicant: LUMINOUS INTENT, INC. [US/US]; 345 McCormick Avenue, Costa Mesa, CA 92626 (US). SCE PCT/18/306 (72) Inventors: METZLER, Richard, A.; 28232 Driza, Mission Viejo, CA 92692 (US). RODOV, Vladimir; 818 South Juanita Avenue, Redondo Beach, CA 90277 (US). ✓ (74) Agents: BLAKELY, Roger, W. et al.; Blakely, Sokoloff, Taylor & Zafman, 7th floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025-1026 (US).		(81) Designated States: AL, AM, AT, AT (Utility model), AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, CZ (Utility model), DE, DE (Utility model), DK, DK (Utility model), EE, EE (Utility model), ES, FI, FI (Utility model), GB, GE, GH, GM, GW, HU, ID, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SK (Utility model), SL, TJ, TM, TR, TT, UA, UG, UZ, VN, YU, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG). Published With international search report. Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments. 9903305.2 19053 6099
(54) Title: SEMICONDUCTOR DIODES HAVING LOW FORWARD CONDUCTION VOLTAGE DROP AND LOW REVERSE CURRENT LEAKAGE		
(57) Abstract Semiconductor diodes having a low forward voltage conduction drop, a low reverse leakage current and a high voltage capability suitable for use in integrated circuits as well as for discrete devices. The semiconductor diodes are fabricated as field effect devices having a common gate and drain connection by a process which provides very short channels, shallow drain regions and longitudinally graded junctions. Continuation of the gate/drain contact layer over specially located tapered edge field oxide (34) maximizes the breakdown voltages of the devices. The preferred fabrication technique utilizes four masking steps, all without any critical mask alignment requirements. Various embodiments are disclosed. ✓ 		