C L A I M S

1. A storage system comprising:

a first stocker that is capable of storing a plurality of memory devices, each of the plurality of memory devices including a plurality of non-volatile memory chips;

a mounter configured to mount at least one of the plurality of memory devices in a case;

a second stocker that is capable of storing a case-mounted memory device, the case-mounted memory device including the case and the at least one of the plurality of memory devices mounted in the case;

a host apparatus including at least one slot to which the case-mounted memory device is connectable, the host apparatus being configured to read or write data from or to the at least one of the plurality of memory devices included in the case-mounted memory device connected to the slot;

a first transport device configured to transport the plurality of memory devices between the first stocker and the mounter; and

a second transport device configured to transport the case-mounted memory device among the mounter, the second stocker, and the host apparatus, wherein

the host apparatus is further configured to:

determine a first memory device to be accessed among the plurality of memory devices;

when a first case-mounted memory device, which is the case-mounted memory device that includes the first memory device, is connected to the slot of the host apparatus, execute reading or writing of data from or to the first memory device;

when the first case-mounted memory device is not connected to the slot of the host apparatus and is stored in the second stocker, cause the second transport device to transport the first case-mounted memory device to the slot of the host apparatus, and to connect the first case-mounted memory device to the slot; and

when the first case-mounted memory device is not connected to the slot of the host apparatus and is not stored in the second stocker, cause the first transport device to transport the first memory device from the first stocker to the mounter, cause the mounter to mount the transported first memory device in the case for assembling the first case-mounted memory device, and cause the second transport device to transport the first case-mounted memory device to the slot of the host apparatus, and to connect the first case-mounted memory device to the slot.

2. The storage system of claim 1, wherein the host apparatus is configured to:

when the first case-mounted memory device that is connected to the slot is not recognized as a storage device,

cause the second transport device to remove the first case-mounted memory device from the slot and to reconnect the first case-mounted memory device to the slot.

3. The storage system of claim 1, wherein the host apparatus is configured to:

manage a priority of each of the plurality of memory devices, and

control a location where each of the plurality of memory devices is present, based on the priority of each of the plurality of memory devices, such that the case-mounted memory device including a memory device having a priority of a first level is connected to the slot of the host apparatus, the case-mounted memory device including a memory device having a priority of a second level lower than the first level is stored in the second stocker, and a memory device having a priority of a third level lower than the second level is stored in the first stocker.

4. The storage system of claim 3, wherein the host apparatus is configured to:

when the priority of a second memory device among the plurality of memory devices stored in the first stocker is raised from the third level to the second level,

cause the first transport device to transport the second memory device from the first stocker to the mounter,

cause the mounter to mount the transported second memory device in the case for assembling a second case-mounted memory device, and

cause the second transport device to transport the second case-mounted memory device from the mounter to the second stocker.

5. The storage system of claim 1, wherein

the case includes a plug terminal, and

the host apparatus includes:

a host case including the slot; and

a receptacle terminal provided in the host case, which is connected to the plug terminal of the

case when the case-mounted memory device is inserted to the slot.

6. The storage system of claim 1, wherein

the plurality of memory devices is a plurality of semiconductor wafers, respectively,

the first stocker is capable of storing the plurality of semiconductor wafers,

the case is a cassette case that is capable of accommodating at least one of the plurality of semiconductor wafers,

the mounter is configured to accommodate the at least one of the plurality of semiconductor wafers in the cassette case,

the second stocker is capable of storing a wafer cassette, the wafer cassette including the cassette case and the at least one of the plurality of semiconductor wafers accommodated in the cassette case,

the first transport device is configured to transport the plurality of semiconductor wafers between the first stocker and the mounter,

the second transport device is configured to transport the wafer cassette among the mounter, the second stocker, and the host apparatus,

the host apparatus includes the at least one slot to which the wafer cassette is connectable, and configured to read or write data from or to the at least one of the plurality of semiconductor wafers included in the wafer cassette connected to the slot, and

the host apparatus is configured to:

determine a first semiconductor wafer to be accessed among the plurality of semiconductor wafers;

when a first wafer cassette, which is the wafer cassette that includes the first semiconductor wafer, is connected to the slot of the host apparatus, execute reading or writing of data from or to the first semiconductor wafer;

when the first wafer cassette is not connected to the slot of the host apparatus and is stored in the second stocker, cause the second transport device to transport the first wafer cassette to the slot of the host apparatus, and to connect the first wafer cassette to the slot; and

when the first wafer cassette is not connected to the slot of the host apparatus and is not stored in the second stocker, cause the first transport device to transport the first semiconductor wafer from the first stocker to the mounter, cause the mounter to accommodate the transported first semiconductor wafer in the cassette case for assembling the first wafer cassette, and cause the second transport device to transport the first wafer cassette to the slot of the host apparatus, and to connect the first wafer cassette to the slot.

7. The storage system of claim 6, wherein the host apparatus is configured to:

when the first wafer cassette that is connected to the slot is not recognized as a storage device,

cause the second transport device to remove the first wafer cassette from the slot and to reconnect the first wafer cassette to the slot.

8. The storage system of claim 6, wherein

the host apparatus is configured to:

manage a priority of each of the plurality of semiconductor wafers, and

control a location where each of the plurality of semiconductor wafers is present, based on the priority of each of the plurality of semiconductor wafers, such that the wafer cassette including a semiconductor wafer having a priority of a first level is connected to the slot of the host apparatus, the wafer cassette including a semiconductor wafer having a priority of a second level lower than the first level is stored in the second stocker, and a semiconductor wafer having a priority of a third level lower than the second level is stored in the first stocker.

9. The storage system of claim 8, wherein the host apparatus is configured to:

when the priority of a second semiconductor wafer among the plurality of semiconductor wafers stored in the first stocker is raised from the third level to the second level,

cause the first transport device to transport the second semiconductor wafer from the first stocker to the mounter,

cause the mounter to accommodate the transported second semiconductor wafer in the cassette case for assembling a second wafer cassette, and

cause the second transport device to transport the second wafer cassette from the mounter to the second stocker.

10. The storage system of claim 6, wherein

a plurality of electrodes is formed on each of the plurality of semiconductor wafers,

the cassette case includes:

a lower case on which the at least one of the plurality of semiconductor wafers is capable of being placed;

an upper case;

a probe card including a plurality of probe pins contactable to the plurality of electrodes of the at least one of the plurality of semiconductor wafers placed on the lower case; and

a controller configured to execute reading or writing of data from or to at least one of the plurality of nonvolatile memory chips through the probe card based on a read request or a write request received from the host apparatus, and

the mounter is configured to bring the plurality of electrodes and the plurality of probe pins into contact with each other by joining the upper case and the lower case on which the at least one of the plurality of semiconductor wafers is placed, to each other.

11. The storage system of claim 10, wherein

the lower case includes three or more centering arms, the three or more centering arms being arranged at equal intervals from each other along a circumference having a predetermined radius from a center of a wafer mounting region in the lower case, the three or more centering arms being movable toward the center of the wafer mounting region, and

the mounter aligns a center of the at least one of the plurality of semiconductor wafers placed on the lower case with the center of the wafer mounting region by moving the three or more centering members toward the center of the wafer mounting region.

12. The storage system of claim 10, wherein

one of the upper case and the lower case includes a groove, and

the other of the upper case and the lower case includes a protruding portion that is to be fitted into the groove.

13. The storage system of claim 10, wherein

the upper case includes a plurality of protruding portions that abut a region on a surface of the at least one of the plurality of semiconductor wafers placed on the lower case when the upper case and the lower case are joined to each other, the region being a region other than the plurality of electrodes on the surface of the at least one of the plurality of semiconductor wafers.

14. The storage system of claim 10, wherein

the upper case includes a cushion material that abuts a region on a surface of the at least one of the plurality of semiconductor wafers placed on the lower case and contracts when the upper case and the lower case are joined to each other, the region being a region other than the plurality of electrodes on the surface of the at least one of the plurality of semiconductor wafers,

each of the plurality of probe pins is connected to the probe card via a conductive elastic member, and

when the upper case and the lower case are joined together, each of the plurality of probe pins is contact with a corresponding electrode, and the conductive elastic member contracts.

15. The storage system of claim 10, wherein

in each of the plurality of semiconductor wafers stored in the first stocker, edge processing to uniformize diameters of the plurality of semiconductor wafers to a first length has been subjected.

16. The storage system of claim 6, wherein

the first stocker includes a first side plate having a first opening,

the mounter includes a second side plate opposing the first side plate of the first stocker, the second side plate having a second opening disposed in a position opposing the first opening, and

the first transport device is configured to transport the plurality of semiconductor wafers between the first stocker and the mounter through the first opening and the second opening.

17. The storage system of claim 16, wherein

the first transport device includes a first robot arm disposed in the first stocker and a second robot arm disposed in the mounter, and

each of the plurality of semiconductor wafers is configured to be passed between the first robot arm and the second robot arm through the first opening and the second opening.

18. The storage system of claim 16, wherein

the mounter includes a third side plate located on an opposite to the second side plate, and the third side plate having a third opening,

the second stocker includes a fourth side plate opposing the third side plate of the mounter and a fifth

side plate located on an opposite side to the fourth side plate, the fourth side plate having a fourth opening located at a position opposing the third opening, and the fifth side plate having a fifth opening,

the host apparatus is included in a server rack, and the server rack including a sixth side plate opposing the fifth side plate of the second stocker, and the sixth side plate having a sixth opening located at a position opposing the fifth opening, and

the second transport device is configured to:

transport the wafer cassette between the mounter and the second stocker, through the third opening and the fourth opening; and

transport the wafer cassette between the second stocker and the server rack including the host apparatus, through the fifth opening and the sixth opening.

19. The storage system of claim 6, wherein

the cassette case includes a plug terminal, and

the host apparatus includes:

a host case including the slot; and

a receptacle terminal provided in the host case, which is connected to the plug terminal of the cassette case when the wafer cassette is inserted to the slot.

20. The storage system of claim 6, wherein

each of the plurality of semiconductor wafers includes a redistribution layer,

a plurality of electrodes included in the redistribution layer are electrically connected to a plurality of electrodes of the nonvolatile memory chip,

respectively, by internal wiring in the redistribution layer,

a size of each of the plurality of electrodes included in the redistribution layer is larger than a size of each of the plurality of electrodes of the nonvolatile memory chip, and

an interval between each other of the plurality of electrodes included in the redistribution layer is wider than an interval between each other of the plurality of electrodes of the nonvolatile memory chip.