# DESCRIPTION

TITLE OF THE INVENTION:

GOLD-COATED BONDING WIRE, METHOD OF MANUFACTURING THEREOF, SEMICONDUCTOR WIRE BONDING STRUCTURE, AND SEMICONDUCTOR DEVICE

## FIELD

**[0001]** The present invention relates to a gold-coated bonding wire, a method of manufacturing thereof, a semiconductor wire bonding structure, and a semiconductor device.

## BACKGROUND

**[0002]** The majority of the market for semiconductor devices is dominated by integrated circuits such as ICs and LSIs that incorporate semiconductor elements such as capacitors and diodes in a single package. A “semiconductor chip” made of a silicon single crystal or the like is incorporated in the integrated circuit. The semiconductor chip contains a large number of electronic circuit elements that perform complex functions, and is a delicate electronic component that is extremely vulnerable to vibration and shock. Further, a plurality of electrodes (called chip electrodes or pads) are provided on the surface of the semiconductor chip, and by bonding wires, electrode parts of a circuit substrate such as a lead frame or circuit board that mainly supports and fixes the semiconductor chip and establishes connections with external wirings and the chip electrodes are bonded and wired.

**[0003]** As for the bonding wire, for example, one end of the bonding wire is bonded to the chip electrode by a method called ball bonding (first bonding), and the other end of the bonding wire is bonded to an external electrode of the circuit substrate such as a lead frame by a method called wedge bonding (or stitch bonding) (second bonding) generally. In the ball bonding, one end of the bonding wire is melted by electrical discharge or the like, and

solidified into a spherical shape by surface tension or the like, to form a ball. The solidified ball is called a free air ball (Free Air Ball: FAB), and is connected to the chip electrode by an ultrasonic wave-combined thermocompression bonding method or the like. In the wedge bonding, ultrasonic waves and load are applied to the wire by a bonding tool (capillary) to bond the wire to the electrode.

**[0004]** As the bonding wire, there are used metal wires such as a gold wire, a silver wire, and a copper wire having a diameter of about 15 to 35 μm, coated wires made by coating these metal wires with other metals, and so on. The semiconductor device is configured by resin-encapsulating the semiconductor chip and the circuit substrate connected by the wire bonding.

**[0005]** By the way, computers, smartphones, digital cameras, portable music players, and other devices have built-in storage devices (memories), and the memories are classified into two types: mechanically readable and writable ones, such as hard disks; and semiconductor memories, such as flash memories. The semiconductor memory is a kind of semiconductor device, and includes an electronic component that stores data, which is called a cell, incorporated in the semiconductor chip. The semiconductor memory used to be rarely used for external storage because of its high cost per capacity, but in recent years, the demand for the semiconductor memory has been increasing because its cost is reduced and the mechanical hard disks have a weak point of being broken by vibrations.

**[0006]** In addition, there are strong needs for storing large-capacity data of music and moving images and for making portable devices such as portable music players smaller and thinner, so that there is an increasing demand for a larger capacity and smaller semiconductor memory. For example, a NAND flash memory has been adopted for storing images of digital cameras, and a USB memory (Universal Serial Bus) has been adopted for smartphones, portable audio players, and the like. The memory capacity was 1 Gbyte or less around A. D. 2000, but around 2010, it met the need for 100 Gbytes or more and in recent years, even larger capacity has been required.

**[0007]** On the other hand, with the miniaturization of portable devices, the demand for

miniaturization of semiconductor memory is also increasing, and naturally, making semiconductor memory chips thinner is also required. Around A. D. 2000, a chip having a thickness of about 150 μm was sufficient, but since then, the thickness of the chip has rapidly decreased, and around 2010, a chip having a thickness of about 30 μm has been adopted. In recent years, the development of chip having a thickness of only 20 μm (0.020 mm) has also been in progress. Needless to say, with the thinning of chip, electronic components, which are originally very delicate and destroyed if not handled carefully, are made even more fragile and must be handled more carefully.

**[0008]** In order to meet the conflicting demands for larger capacity and miniaturization, semiconductor memory manufacturers each have been working to develop thinner memory chips and multistage stacked packaging. There is a limit to the storage capacity of one memory chip with specifications of about 4 to 8 Gbytes per chip, and thus, at least 16 chips are required to meet a 128-Gbyte storage capacity requirement, for example. The memory product itself becomes large when a plurality of semiconductor devices are incorporated, so that stacking thin chips in one semiconductor device becomes a means to meet the needs for both large capacity and miniaturization. Examples of the stacking method include a method of stacking chips in a unidirectional stepped shape as illustrated in FIG. 11 and FIG. 12 to be described later, a method of stacking chips so as to form a V shape laid down horizontally as illustrated in FIG. 13, and so on.

**[0009]** In the field of the above-described semiconductor memory, there is a mission to bond and wire the electrodes on the surface of these stacked delicate and fragile chips and the electrode of the lead frame or circuit board using bonding wires. Here, there is explained a bonding method that has been performed so far. For example, in the case of a semiconductor device with a circuit board and three chips thereon stacked in four stages as illustrated in FIG. 9, first, a projecting electrode called a bump is formed on an electrode of each of the chips, and then a bonding wire is ball-bonded onto an electrode of the circuit board, and then a looping operation is performed and the bonding wire is wedge-bonded onto the surface of the bump formed on the chip electrode. Such a bonding method is

called a BSOB (BALL STITCH ON BALL) method or reverse bonding. This is intended to obtain such an effect as a cushioning material that prevents chip destruction by forming the bump on the delicate and fragile chip electrode. This BSOB is performed repeatedly for 3 times each to connect the chip electrodes and the circuit board. A normal order is to perform ball bonding directly on the chip electrode without forming a bump on the chip electrode, perform a looping operation, and then wedge-bond the bonding wire to the electrode of the circuit board. Such a bonding method is called a positive bonding method. Generally, the chip electrode and the circuit board are connected by the positive bonding method, but with the recent thinning of a semiconductor package, it is necessary to control the loop height low, so that as the bonding method on the stacked chips, the reverse bonding method has been adopted. The ball bonding has a significant negative impact on the thinning of the semiconductor memory because after the FAB is formed, the wire goes straight up near a neck portion between a ball portion and a wire portion due to wire characteristics, and is not easily bent at a steep angle, and thus, when performing ball bonding on the chip electrode at the upper stage by the positive bonding method, a space up to a higher position is required. Therefore, this is one of the main reasons for performing the reverse bonding from the electrode of the circuit board at the lower position to the chip electrode at the upper stage. Incidentally, the conditions for the bonding wire suitable for the reverse bonding method include having softness that does not destroy the delicate chip electrode and having high corrosion resistance and oxidation resistance of the bump surface and the wire surface for performing wedge bonding on the bump. Therefore, a gold (Au) bonding wire and a gold (Au) bump containing soft and non-oxidizing gold (Au) as a main component are used.

**[0010]** However, the above-described bonding method requires man-hours to go back and forth between the chip electrodes and the circuit board because the distance between the chip electrode and the circuit board is longer and the chip electrode and the circuit board are connected by a single wire, resulting in lower productivity. In addition, the longer loop length causes problems such as controlling the straightness of the wire after

looping. Thus, a method (cascade bonding method) has been introduced to connect chip electrodes by a wire and then connect the chip electrodes and an electrode of a circuit board as illustrated in FIG. 10. The cascade bonding method is explained below. In the case of a semiconductor device in which a circuit board and three chips are stacked in four stages, the chips are connected from the upper stage (the lowermost-stage circuit board is set to the first stage and the uppermost-stage chip is set to the fourth stage). First, a bump is formed on the third-stage chip electrode, ball bonding is performed on the fourth-stage chip electrode, a looping operation is performed, and then a bonding wire is wedge-bonded onto the bump formed on the third-stage chip electrode. Thereby, the third-stage chip electrode and the fourth-stage chip electrode are connected. Next, a bump is formed on the second-stage chip electrode, and ball bonding is performed on the wedge-bonded bump on the third-stage chip electrode. After performing a looping operation, wedge bonding is performed on the bump formed on the second-stage chip electrode. Thereby, the second-stage chip electrode, the third-stage chip electrode, and the fourth-stage chip electrode are connected. Finally, ball bonding is performed on the bump with a wedge bonding portion formed on the second-stage chip electrode, and the bonding wire is wedge-bonded to the first-stage circuit board through a looping operation. As a result, a state of a series wiring from the uppermost-stage chip electrode to the lowermost-stage electrode of the circuit board is made. In the case of this method as well, as in the reverse bonding method, a gold (Au) bonding wire and a gold (Au) bump are used because the characteristics required for the bonding wire are required to have softness and oxidation resistance.

**[0011]** These methods have met the demands for larger capacity and miniaturization of the semiconductor device, but this time, with these methods, a four-step cycle of (1) bump formation, (2) ball bonding, (3) wedge bonding, and (4) wire tearing off must be performed for the number of chips, and thus, in response to the recent trend toward ultra-multistage stacking of chips, such as 16 stages or 32 stages due to a further increase in the capacity, there has been caused a problem that the number of steps is too large, such as 64 steps or 128 steps, the productivity is lowered, and the manufacturing cost is very high.

Therefore, as a bonding method improved mainly by a bonding device manufacturer, there has been proposed a multistage continuous bonding method called capillary wedge bonding (CWB: Capillary Wedge Bonding). The CWB is not conventional ball bonding, but is a method in which wedge bonding is performed on the uppermost-stage chip electrode, followed by looping and performing wedge bonding on the next-stage chip electrode, and the same single wire is continuously connected to the next-stage chip electrode without tearing off the wire and the same wire is connected to the electrode of the circuit board finally. With this method, the aforementioned bump formation, wire tearing off after wedge bonding, and ball bonding after FAB formation can be omitted, thus enabling a significant reduction of the man-hours required. Specifically, only one step of wedge bonding is performed for each chip, and thus, the conventional man-hours are reduced to one-fourth of the man-hours and bonding can be performed continuously without forming bumps or FABs, resulting in that the bonding time can be significantly shortened. Moreover, since neither bumps nor FABs are formed, the amount of bonding wire used can be significantly reduced. This makes it possible to significantly increase the productivity and reduce the manufacturing cost (FIG. 6 to be described later is an example of conventional ball bonding, and FIG. 11 and FIG. 12 are examples of the CWB).

**[0012]** As described above, using the CWB method in a bonding device can significantly improve the productivity of continuous bonding of multistage stacked chips. This is namely an improvement in the hard side, and for the bonding wire, which is the soft side, a gold wire that does not damage the chip electrode is still supposed to be used. As described above, bumps and FABs no longer need to be formed, but the use amount of bonding wire increases significantly when multistage stacked chips are required, thus creating a new issue that the productivity has improved, but the use of expensive gold increases the material cost, resulting in higher total costs.

**[0013]** Our issue is to develop a bonding wire that has the characteristics equivalent to those of gold and is applicable to the CWB method with no material cost, in place of the

bonding wire containing gold as a main component. As a result of summarizing the conditions of the wire required for continuous bonding of multistage stacked chip electrodes by the CWB method, they are (1) good wedge bondability (having continuous bondability and bonding strength), (2) no damage to chip electrodes, (3) thin wire having a diameter of 35 μm or less, (4) inexpensive material cost, (5) low specific resistance, which is not limited to the CWB, and so on.

**[0014]** For example, Japanese Laid-open Patent Publication No. 2007-012776 (Patent Document 1) describes, as a bonding wire capable of improving the formability and bondability of a ball as well as increasing the bonding strength of wedge bonding, a bonding wire that includes: a core material containing copper as a main component; and an outer skin layer that is provided on the core material and contains a conductive metal different from the core material in one or both of its component and composition and copper, the outer skin layer having a thickness of 0.001 to 0.02 μm (1 to 20 nm). Further, Japanese Laid-open Patent Publication No. 2007-1297 (Patent Document 2) describes, as a bonding wire capable of improving the formability and bondability of a ball as well as increasing the bonding strength of wedge bonding, a bonding wire including: a core material containing one type or more of silver, gold, palladium, platinum, and aluminum as a main component element; and an outer skin layer containing a conductive metal different from the main component element as a main component, the outer skin layer having a thickness of 0.001 to 0.09 μm (1 to 90 nm). These bonding wires only improve the wedge bondability, or the like by controlling the thickness of the outer skin layer, the thickness of a concentration gradient region between the core material and the outer skin layer or another region, the concentration distribution, or the like, and no attention is paid to the characteristics of the bonding wire itself including the outer skin layer and no control is also performed on the bonding wire. Further, the target partner for wedge bonding mentioned here is the electrode of a lead frame or circuit board, or the bump on a chip electrode, which is fundamentally different from the case of direct wedge bonding to a delicate and fragile thin chip electrode.

**[0015]** Further, International Publication Pamphlet No. WO 2013/129253 (Patent Document 3) describes a power semiconductor device in which a metal electrode (die electrode) of a power semiconductor die and a metal electrode (connection electrode) of a substrate or the like are both wedge-connected with a metal wire, in which the metal wire is an Ag or Ag alloy wire having a diameter of greater than 50 μm and 2 mm or less, or a wire including a coating layer having one type or more of Pd, Au, Zn, Pt, Ni, and Sn, or an alloy thereof, or an oxide or nitride of these metals, the coating layer having a thickness of 3 nm or more, on the surface of an Ag or Ag alloy wire. In this power semiconductor device, the metal wire is wedge-bonded to both the die electrode and the connection electrode, but the metal wire is a thick wire having a diameter of greater than 50 μm and 2 mm or less, and fine metal wires having diameters of about 15 to 35 μm are not considered. Further, in this power semiconductor device, the wedge bondability is merely improved by the selection of the constituent metal and the thickness of the electrode coating layer coating the surface of the die electrode, or the like. Further, the electrode of the power semiconductor, which handles relatively large amounts of power, is fundamentally different from the delicate and fragile thin chip electrode of a memory and other devices.

CITATION LIST

PATENT LITERATURE

**[0016]** Patent Literature 1: Japanese Laid-open Patent Publication No. 2007-012776

Patent Literature 2: Japanese Laid-open Patent Publication No. 2007-123597

Patent Literature 3: International Publication Pamphlet No. WO 2013/129253

SUMMARY OF INVENTION

TECHNICAL PROBLEM

**[0017]** As described above, the issue for the present inventors is to develop, in place of the bonding wire containing gold as a main component, a bonding wire that has the characteristics equivalent to those of gold and is applicable to the method (CWB) of directly wedge-bonding multistage stacked chip electrodes with no material cost, while considering the needs for thinner chips and multistage stacking of semiconductor devices

such as a memory. As described repeatedly, the condition issues necessary for the wire are: (1) good wedge bondability (having continuous bondability and bonding strength), (2) no damage to chip electrodes, (3) thin wire having a diameter of 35 μm or less, (4) inexpensive material cost, (5) low specific resistance, which is not limited to the CWB, and so on.

**[0018]** Further, when chips are stacked in multiple stages in order to make the semiconductor device thinner, the chips are arranged so as to form a V shape laid down horizontally, as illustrated in FIG. 13, and thereby, a space is made under a chip electrode part, resulting in that a portion having no base (support) for the chips is formed. It was found out that in the absence of a base, the ultrasonic wave application by the capillary becomes ineffective and the bonding energy given to the chip is reduced, resulting in weakened bonding strength. Since the chips are stacked in multiple stages, it is necessary to individually set the bonding energy suitable for each of the stages. The bonding energy is the range of conditions required to obtain stable bonding, and the wedge bonding conditions are mainly a load, ultrasonic wave application, and a heating temperature. A wide condition range of the bonding energy is required when the situations around the bonding points vary individually.

**[0019]** The present inventors repeated trial and error with existing bonding wires not containing gold as a main component, and found out that the range of the bonding energy that can be handled with the existing bonding wires is narrow, and thus, in continuous wedge bonding, in the case where the bonding energy is low, namely the load is low where the wire crushing amount is small mainly, the bonding strength is weak and in the middle of the next looping, wire peeling (a lift) occurs at a bonding interface, and in the case where the bonding energy is high where (the wire crushing amount is large and the load is high), on the other hand, chip damage is caused and the wire is deformed so thin that the wire breaks at a point of a thin bonding portion in the middle of the next looping.

**[0020]** The present invention is to provide a bonding wire that is capable of continuously and well wedge-bonding thin and multistage staked chip electrodes of a

semiconductor memory or the like, does not damage the chip electrodes, has a wide range of bonding energy conditions, has a low specific resistance, and has a low material cost. Further, the issue is solved by providing a manufacturing method of the bonding wire and a semiconductor wire bonding structure and a semiconductor device using the bonding wire.

**[0021]** In order to solve the above-described wedge bonding problems, the present inventors found out that controlling a compressive stress of the wire is effective as a result of the conclusion reached through diligent research and trials and errors with the bonding wire. The compressive stress is the value of strength (force) per unit area when the wire is deformed by receiving force in a compressing direction, and they found out in the present invention that the issue can be solved as long as the compressive stress when the wire is compressed (deformed) by 60% with respect to the wire diameter is in a range of 290 MPa or more and 590 MPa or less.

**[0022]** Details of the method of measuring the compressive stress of the present invention will be described in paragraphs [0050] to [0053] to be described later, but the compressive stress is calculated from the following equation.

**[0023]** Wire compressive stress (MPa) = Force applied at 60% deformation with respect to a wire diameter (N) / (Circumference ratio × Wire diameter (mm) / 2) × Indenter diameter (mm)

Incidentally, as the compressive stress, a value automatically calculated by a compression testing machine may be used. The indenter diameter is the diameter of the indenter attached to the compression testing machine. As the circumference ratio, 3.14 is used.

**[0024]** As a basic idea of the present invention, the present inventors have focused on a wire structure in which Ag or Cu wires are used mainly and surfaces of these wires are coated with soft Au under the condition that the above-described compressive stress falls within the range, the specific resistance is low, and the cost is low.

**[0025]** The gold-coated bonding wire of the present invention is a gold-coated bonding wire including: a core material containing silver or copper as a main component; and a

coating layer that is provided on a surface of the core material and contains gold as a main component, in which a compressive stress when the gold-coated bonding wire is deformed by 60% with respect to a wire diameter is 290 MPa or more and 590 MPa or less.

**[0026]** The manufacturing method of the gold-coated bonding wire of the present invention is a method of manufacturing a gold-coated bonding wire, the gold-coated bonding wire including: a core material containing silver or copper as a main component; and a coating layer that is provided on a surface of the core material and contains gold as a main component, the manufacturing method including: setting a compressive stress when the gold-coated bonding wire is deformed by 60% with respect to a wire diameter to 290 MPa or more and 590 MPa or less.

**[0027]** The semiconductor wire bonding structure of the present invention is a semiconductor wire bonding structure including: a gold-coated bonding wire including: a core material containing silver or copper as a main component; and a coating layer containing gold as a main component; an electrode of a semiconductor chip; and a wedge bonding portion where the wire and the electrode are bonded, in which a film thickness of the coating layer is 5 nm or more and 200 nm or less, and the gold-coated bonding wire has a compressive stress of 290 MPa or more and 590 MPa or less when deformed by 60% with respect to a wire diameter.

**[0028]** The semiconductor device of the present invention is a semiconductor device including: one or a plurality of semiconductor chips, the semiconductor chip including at least one first electrode; a circuit substrate that is selected from a lead frame and a circuit board including at least one second electrode; and a gold-coated bonding wire that electrically connects at least one selected from between the first electrode of the semiconductor chip and the second electrode of the circuit substrate and between the first electrodes of a plurality of the semiconductor chips and is wedge-bonded to at least one of the first electrode and the second electrode or one of a plurality of the first electrodes, in which the gold-coated bonding wire includes: a core material containing silver or copper as a main component; and a coating layer that is provided on a surface of the core material

and contains gold as a main component, and a compressive stress of the gold-coated bonding wire is 290 MPa or more and 590 MPa or less.

EFFECT OF THE INVENTION

**[0029]** According to the gold-coated bonding wire and the manufacturing method thereof of the present invention, by setting the compressive stress to 290 MPa or more and 590 MPa or less, a stable wedge bonding strength can be obtained without damaging semiconductor chip electrodes and the like, even in the case of continuous wedge bonding where the bonding energy condition varies depending on individual bonding points such multistage stacked chip electrodes. Further, according to the semiconductor device of the present invention, the use of such a gold-coated bonding wire makes it possible to provide an inexpensive, thin, and large storage capacity semiconductor memory, and the like with a reduced total cost.

**[0030]** In addition to the above effects, the present invention is naturally effective in bonding stability, bonding reliability, and the like in ball bonding to ordinary semiconductor chip electrodes and wedge bonding to substrate circuits, lead frames, and the like.

BRIEF DESCRIPTION OF THE DRAWINGS

**[0031]** [FIG. 1] FIG. 1 is a vertical cross-sectional view illustrating a gold-coated bonding wire in an embodiment.

[FIG. 2] FIG. 2 is a cross-sectional view illustrating the gold-coated bonding wire in the embodiment.

[FIG. 3] FIG. 3 is a vertical cross-sectional view illustrating a modified example of the gold-coated bonding wire in the embodiment.

[FIG. 4] FIG. 4 is a cross-sectional view illustrating the modified example of the gold-coated bonding wire in the embodiment.

[FIG. 5] FIG. 5 is a view illustrating an indentation shape in a compressive stress test of the bonding wire in the embodiment.

[FIG. 6] FIG. 6 is a cross-sectional view illustrating a stage of a semiconductor

device in an embodiment before resin encapsulation.

[FIG. 7] FIG. 7 is a cross-sectional view illustrating a stage of the resin-encapsulated semiconductor device in the embodiment.

[FIG. 8] FIG. 8 is a cross-sectional view illustrating a wedge bonding portion of the gold-coated bonding wire bonded to an electrode of a semiconductor chip in the semiconductor device in the embodiment.

[FIG. 9] FIG. 9 is a view illustrating one example of a wire connection structure of conventional multistage stacked semiconductor chips.

[FIG. 10] FIG. 10 is a view illustrating another example of the wire connection structure of the conventional multistage stacked semiconductor chips.

[FIG. 11] FIG. 11 is a cross-sectional view illustrating a first modified example of the semiconductor device in the embodiment.

[FIG. 12] FIG. 12 is a cross-sectional view illustrating a second modified example of the semiconductor device in the embodiment.

[FIG. 13] FIG. 13 is a cross-sectional view illustrating one example of a semiconductor device including a multistage stacked structure of semiconductor chips.

DETAILED DESCRIPTION

**[0032]** Hereinafter, there will be explained a gold-coated bonding wire in an embodiment of the present invention and a method of manufacturing thereof, a semiconductor wire bonding structure, and a semiconductor device with reference to the drawings. In each embodiment, substantially the same constituent portions will be denoted by the same reference numerals and symbols and explanation thereof is sometimes partially omitted. The drawings are schematic, and a relation between a thickness and a planar dimension, a thickness ratio of the respective parts, a ratio between a vertical size and a transverse size, and so on are sometimes different from actual ones. Further, as the compressive stress (MPa) in this description, a value based on the conversion formula of 1 $kgf/mm^2$ = 9.8 MPa is used.

**[0033]** (Gold-coated bonding wire and Manufacturing method thereof)

A gold-coated bonding wire 1 in an embodiment includes a core material 2 containing silver (Ag) or copper (Cu) as a main component and a coating layer 3 that is provided on the surface of the core material 2 and contains gold (Au) as a main component as illustrated in FIG. 1 and FIG. 2. As illustrated in FIG. 3 and FIG. 4, the gold-coated bonding wire 1 in the embodiment may further include an intermediate metal layer 4 provided between the core material 2 and the coating layer 3. The intermediate metal layer 4 contains one metal selected from palladium (Pd), platinum (Pt), and nickel (Ni) as a main component.

**[0034]** The gold-coated bonding wire 1 in the embodiment, when deformed by 60% with respect to its wire diameter, has a compressive stress of 290 MPa or more and 590 MPa or less. The compressive stress of the gold-coated bonding wire 1 affects the amount of deformation of the wire, the bondability to electrodes, or the like when the gold-coated bonding wire 1 is wedge-bonded to an electrode of a semiconductor chip and an electrode of a circuit substrate such as a circuit board or a lead frame. In response to such a point, by using the gold-coated bonding wire 1 having a compressive stress of 290 MPa or more and 590 MPa or less, stable wedge bondability and wedge bonding strength can be obtained without damaging the semiconductor chip or the like during wedge bonding. This makes it possible to obtain a sufficient wedge bonding strength without causing chip damage when continuously connecting electrodes of multistage stacked semiconductor chips with a single bonding wire by the CWB with the connection energy that varies in condition depending on each bonding point in particular.

**[0035]** The critical significance of defining the range of compressive stress is explained. When the compressive stress of the gold-coated bonding wire 1 is less than 290 MPa, the gold-coated bonding wire 1 is excessively deformed by the energy at the time of wedge bonding, specifically, by the applied ultrasonic waves and load, so that the width of the crushed wire of a wire bonding portion with respect to the electrode becomes too large. When a portion of the crushed wire protrudes to the outside of the electrode, it comes into contact with an adjacent wire bonding portion to easily cause short circuit

failure to occur. In addition, the wire bonding portion is too crushed and the bonded wire becomes thin, and when a loop is formed by a bonding tool (capillary), the wire at the bonding portion is prone to breakage or the like. In particular, when continuously connecting the electrodes of the semiconductor chips with a single bonding wire by the CWB, the width of the crushed wire and the wire thickness at the wire bonding portion are likely to be unstable. On the contrary, when wedge bonding is performed with low bonding energy in order to avoid such problems, the wire at the bonding portion is not sufficiently deformed, the wedge bonding strength becomes weak, and wire peeling is likely to occur at the bonding interface during the next loop formation. Incidentally, a pull test is a means of evaluating such a bonding strength, and the wire peeling is called a lift, which is a barometer to evaluate the possibility of peeling to occur at the bonding interface between the wire and the electrode. The compressive stress of the gold-coated bonding wire 1 is preferably 340 MPa or more.

**[0036]** On the other hand, when the compressive stress of the gold-coated bonding wire 1 exceeds 590 MPa, even if wedge bonding is performed with high bonding energy, the wire is not easily deformed, the bonding area of the wire bonding portion decreases, the bonding strength becomes weak, and wire peeling is likely to occur at the bonding interface during the next loop formation. A lift occurs in the aforementioned pull test also in this case. Therefore, the compressive stress of the gold-coated bonding wire 1 is preferably 540 MPa or less, and more preferably 490 MPa or less. That is, by using the gold-coated bonding wire 1 having a compressive stress of 290 MPa or more and 590 MPa or less, stable wedge bonding is enabled under a wide range of wedge bonding conditions.

**[0037]** As for the compressive stress of the gold-coated bonding wire 1, a compressive stress of 290 MPa or more and 590 MPa or less can be obtained by appropriately controlling the composition of a metal material (silver-based material or copper-based material) forming the core material 2, the composition of the core material 2 and a heat treatment, the thicknesses of the coating layer 3 and the intermediate metal layer 4, the diameter of the bonding wire 1, conditions of heat treatments applied to the bonding wire

1, or the like, as will be described in detail later. However, the compressive stress of the gold-coated bonding wire 1 is not limited to the material, the manufacturing process, the manufacturing conditions, or the like of the gold-coated bonding wire 1, and exhibits its characteristics as long as it is within the above range.

**[0038]** The above-described gold-coated bonding wire 1 preferably has a diameter of 13 μm or more and 35 μm or less (a diameter D illustrated in FIG. 1). When the diameter of the wire 1 is less than 13 μm, the strength, conductivity, or the like may decrease and the reliability or the like of wire bonding may decrease when the wire bonding is performed using the bonding wire 1 during manufacture of the semiconductor device. When the diameter of the wire 1 exceeds 35 μm, the bonding bondability to the electrode, particularly, the wedge bonding bondability, may decrease. For example, an opening area between narrow-pitched electrodes of a semiconductor device becomes small. When the bonding wire 1 having a diameter of greater than 35 μm is wedge-bonded into the opening area between such narrow-pitched electrodes, destruction of a passivation film or a short circuit between adjacent bonding portions may occur. Incidentally, the passivation film is an insulating film on the uppermost layer of the chip, and has a function of protecting the inside from external moisture or metal ions derived from an encapsulating resin or the like. Therefore, when the chip is viewed from its vertical cross section, the passivation film is positioned higher than a bonding surface of the chip. When the diameter of the wire exceeds 35 μm, contact with the side surface of the wire near the bonding portion or contact with the wire crushed at the bonding portion during bonding will cause destruction of the passivation film.

**[0039]** The core material 2 mainly forms the bonding wire 1 in the embodiment and plays the function of the bonding wire 1. As the main component of such a core material 2, silver or copper is used. Here, containing silver or copper as a main component means that the core material 2 contains at least 50 mass% or more of silver or copper. In the case where a material containing silver as a main component is used as the core material 2, the core material 2 may be formed of pure silver, but is preferably formed of a silver alloy

made by adding an additive element to silver. Further, in the case where a material containing copper as a main component is used as the core material 2, the core material 2 may be formed of pure copper, but is preferably formed of a copper alloy made by adding an additive element to copper. Pure metals have the disadvantage of causing self annealing to be too soft, thus making the bonding wire difficult to be handled in the manufacturing process. Alloying them has the advantage that the alloys become moderately harder than the pure metals to make the bonding wire easier to be handled in the manufacturing process. In addition, using the core material 2 formed of a silver alloy or copper alloy also has the advantage that the gold-coated bonding wire 1 having a compressive stress of 290 MPa or more and 590 MPa or less can be obtained easily.

**[0040]** In principle, controlling the compressive stress of the entire wire is the most important condition for achieving the issue, but the core material 2 containing silver or copper as a main component preferably has a Vickers hardness (Hv) of 40 or more and 80 or less. The Vickers hardness mentioned here is the Vickers hardness of the core material 2 in the cross section of the gold-coated bonding wire 1. When the Vickers hardness of the core material 2 is 40 or more and 80 or less, it becomes easy to obtain the gold-coated bonding wire 1 having a compressive stress of 290 MPa or more and 590 MPa or less. That is, when the Vickers hardness of the core material 2 is less than 40, the compressive stress of the gold-coated bonding wire 1 becomes too low, thereby making it difficult to obtain a compressive stress of 290 MPa or more. When the Vickers hardness of the core material 2 exceeds 80, the compressive stress of the gold-coated bonding wire 1 becomes too high, thereby making it difficult to obtain a compressive stress of 590 MPa or less. The Vickers hardness of the core material 2 is more preferably 45 or more, and more preferably 70 or less. Of course, not only does this make it easier to obtain the target compressive stress, but also by further setting the hardness to the Vickers hardness in this range, the synergistic effect of the compressive stress and the hardness further improves the wedge bondability. Incidentally, the compressive stress and the Vickers hardness do not necessarily have a simple proportional relationship.

**[0041]** When the core material 2 is formed of a silver alloy, the content of silver in the silver alloy is preferably 97 mass% or more. The silver alloy forming the core material 2 preferably contains at least one element selected from the group consisting of copper (Cu), calcium (Ca), phosphorus (P), gold (Au), palladium (Pd), platinum (Pt), nickel (Ni), rhodium (Rh), indium (In), and iron (Fe). The element to be added to the silver alloy that forms the core material 2 improves the reliability (corrosion resistance) of the gold-coated bonding wire 1 and increases the Vickers hardness of the core material 2, thereby exhibiting an effect of preventing self annealing. When the self annealing is caused, the wire becomes too soft, which makes the wire difficult to be handled in the manufacturing process and further makes the wire more easily scratched. However, when the content of the additive element is too large, the specific resistance of the core material 2 increases, and the electrical conductivity of the core material 2 and furthermore the gold-coated bonding wire 1 decreases. The content of the additive element preferably falls within a range of 1 mass ppm or more and 3 mass% or less with respect to the total amount of the wire 1.

**[0042]** When the content of the additive element in the silver alloy that forms the core material 2 is less than 1 mass ppm with respect to the total amount of the wire 1, there is a possibility that the reliability of the gold-coated bonding wire 1, the effect of inhibiting self annealing of the core material 2, and the like cannot be sufficiently obtained. When the content of the additive element exceeds 3 mass% with respect to the total amount of the wire 1, the specific resistance of the gold-coated bonding wire 1 increases. The content of the additive element is preferably set so that the specific resistance of the gold-coated bonding wire 1 falls within a range of 2.3 μΩ•cm or less.

**[0043]** When the core material 2 is formed of a copper alloy, the content of copper in the copper alloy is preferably 98 mass% or more. The copper alloy forming the core material 2 preferably contains at least one element selected from the group consisting of phosphorus (P), gold (Au), palladium (Pd), platinum (Pt), nickel (Ni), silver (Ag), rhodium (Rh), indium (In), gallium (Ga), and iron (Fe). As described above, the element to be

added to the copper alloy that forms the core material 2 improves the reliability (corrosion resistance) of the gold-coated bonding wire 1 and increases the Vickers hardness of the core material 2, thereby exhibiting an effect of preventing self annealing. When the self annealing is caused, the wire becomes too soft, which makes the wire difficult to be handled in the manufacturing process and further makes the wire more easily scratched even by a slight impact. However, when the content of the additive element is too large, the specific resistance of the core material 2 increases, and the function as the core material 2 and furthermore as the gold-coated bonding wire 1 decreases. The content of the additive element preferably falls within a range of 1 mass ppm or more and 2 mass% or less with respect to the total amount of the wire 1.

**[0044]** When the content of the additive element in the copper alloy that forms the core material 2 is less than 1 mass ppm with respect to the total amount of the wire 1, there is a possibility that the reliability of the gold-coated bonding wire 1, the effect of inhibiting self annealing of the core material 2, and the like cannot be sufficiently obtained. When the content of the additive element exceeds 2 mass% with respect to the total amount of the wire 1, the specific resistance of the gold-coated bonding wire 1 increases. The content of the additive element is preferably set so that the specific resistance of the gold-coated bonding wire 1 falls within a range of 2.3 μΩ•cm or less.

**[0045]** In the gold-coated bonding wire 1 using the core material 2 formed of silver and the silver alloy described above, the compressive stress is preferably 290 MPa or more and 440 MPa or less. Using such a gold-coated bonding wire 1 makes it possible to improve the wedge bondability while satisfying the wire characteristics of the gold-coated bonding wire 1 using the silver-based core material 2. Further, in the gold-coated bonding wire 1 using the core material 2 formed of copper and the copper alloy described above, the compressive stress is preferably 440 MPa or more and 590 MPa or less. Using such a gold-coated bonding wire 1 makes it possible to improve the wedge bondability while satisfying the wire characteristics of the gold-coated bonding wire 1 using the copper-based core material 2.

**[0046]** The gold-coated bonding wire 1 in the embodiment includes the coating layer 3 provided on the surface of the above-described core material 2 containing silver or copper as a main component. The coating layer 3 contains gold as a main component. Here, containing gold as a main component means that the coating layer 3 contains 50 mass% or more of gold. The coating layer 3 containing gold as a main component improves the corrosion resistance of the wire, and is compatible with aluminum (Al) and an aluminum alloy (Al alloy) that form the electrode of the semiconductor chip, gold (Au) and a gold alloy (Au alloy) that form the electrode of the circuit board, silver (Ag) plating and silver alloy (Ag alloy) plating formed on the surface of an inner lead of a lead frame, and so on and diffuses easily, and thus a good bonding strength, particularly, a good wedge bonding strength is exhibited. Therefore, when the bonding wire 1 including the coating layer 3 containing gold as a main component on the surface is wedge-bonded, particularly, continuously bonded by the CWB, the bonding wire 1 can be wedge-bonded with good bonding strength and bonding reliability.

**[0047]** The coating layer 3 may be formed of pure gold (gold content of 99.9% or more) or may be formed of a gold alloy made by adding an additive element to gold. The gold alloy forming the coating layer 3 preferably contains at least one element selected from the group consisting of antimony (Sb), palladium (Pd), platinum (Pt), nickel (Ni), cobalt (Co), and bismuth (Bi). The element to be added to the gold alloy that forms the coating layer 3 is effective in improving the bonding reliability of the gold coating layer 3 with aluminum (Al) that forms the semiconductor chip electrode, or other factors. Further, the film thickness of the gold coating layer 3 is preferably 5 nm or more and 200 nm or less. By setting the film thickness of the gold coating layer 3 to 5 nm or more, the wedge bondability to the aluminum electrode, the gold electrode, the silver-plated electrode, and the like by the gold coating layer 3 can be sufficiently improved. When the film thickness of the gold coating layer 3 exceeds 200 nm, the manufacturing cost of the gold-coated bonding wire 1 increases, which is not preferable. As described above, the product of the present invention may also be used for ball bonding applications, and thus,

when the film thickness of the gold coating layer exceeds 200 nm, ball formability such as eccentricity of a FAB may deteriorate. Further, the film thickness of the gold coating layer 3 is preferably greater than 20 nm, more preferably 50 nm or more, and more preferably 150 nm or less.

**[0048]** As described above, the gold-coated bonding wire 1 in the embodiment may include the intermediate metal layer 4 provided between the core material 2 and the coating layer 3, as illustrated in FIG. 3 and FIG. 4. The intermediate metal layer 4 contains one metal selected from palladium (Pd), platinum (Pt), and nickel (Ni) as a main component. By providing such an intermediate metal layer 4 between the core material 2 and the coating layer 3, not only is reliability (corrosion resistance) improved, but it is also possible to inhibit the forming material of the core material 2 from seeping beyond the coating layer 3 onto the surface of the bonding wire 1 at high temperatures. For example, when copper is exposed on the outermost surface of the core material 2, there is a greater risk of oxidation, or when silver is exposed on the outermost surface of the core material 2, there is a greater risk of sulfurization. These all result in the factor that reduces the bonding reliability of the gold-coated bonding wire 1 to the electrode. In response to this point, by providing the intermediate metal layer 4 between the core material 2 and the coating layer 3, copper or silver seepage to the surface of the wire in a high-temperature atmosphere can be inhibited, to improve the bonding reliability.

**[0049]** The intermediate metal layer 4 may be formed of pure palladium, pure platinum, or pure nickel, or formed of an alloy containing two or more of these metals. Further, the intermediate metal layer 4 may contain one metal selected from palladium, platinum, and nickel as a main component, and may be formed of a palladium alloy, platinum alloy, or nickel alloy made by adding an additive element to each of the metals.

**[0050]** The intermediate metal layer 4 preferably has a thickness of 60 nm or less. When the thickness of the intermediate metal layer 4 exceeds 60 nm, the original characteristics such as ball formability of a FAB of the gold-coated bonding wire 1 may be impaired. Incidentally, the thickness of the intermediate metal layer 4 is preferably 1 nm

or more in order to sufficiently obtain the effect of inhibiting the above-described copper or silver from being exposed on the surface of the wire. Incidentally, the gold-coated bonding wire 1 in the embodiment is not limited to the one formed only of the core material 2 and the coating layer 3 described above, or the core material 2, the coating layer 3, and the intermediate metal layer 4. The gold-coated bonding wire 1 in the embodiment may have a configuration other than these, which is, for example, a three-layer coating structure, a four-layer coating structure, or the like, according to need.

**[0051]** The compressive stress of the gold-coated bonding wire 1 is measured as follows. That is, a wire sample is prepared by cutting the gold-coated bonding wire 1 into a length of several centimeters with no tension applied thereto. The wire sample is placed horizontally on a flat sample stage of a compression testing machine (for example, Micro Compression Tester Model No. MCT-W-500 manufactured by SHIMADZU CORPORATION), while considering that the wire sample should not stretch or sag. Then, as settings for the machine, a circular sample shape is selected, an indenter size is set to ϕ200 μm, a deformation amount in the cross-sectional direction of the wire is set to 60% of the wire diameter, and the maximum load according to the wire diameter is set. For example, when the wire diameter is ϕ 20 μm, the maximum load is set to 3.5 N as a guide.

**[0052]** Then, the stage is moved so that the wire comes to the center of the indenter, the surface of the wire is compressed by the indenter, and the compressive stress of the wire is found. The compressive stress value is calculated automatically by the machine, and the value can be used without any problem. In the calculation equation, the value obtained by dividing the force applied when the wire diameter is compressed by 60% by the cross-sectional area of the crushed wire is used. Here, there is explained how to find the cross-sectional area. When the wire surface is crushed by the indenter evenly and as thinly as possible in an ideal state, the shape (cross section) of the crushed wire becomes a quadrangle, and the thickness approaches as close to 0 (zero) as possible. The horizontal length of the cross section is the diameter of the indenter, and the vertical length is a value as close as possible to half the circumference length of the wire. Therefore, the cross-

sectional area of the wire is found by the horizontal length × the vertical length, and thus, the diameter of the indenter × (the circumference ratio × the diameter/2) is established.

**[0053]** In a specific example, 60%-compression of a wire diameter of 20 μm means that the force (N) applied at the point where the wire is crushed to a height of 8 μm is divided by the cross-sectional area ($mm^2$) defined above. That is, the value obtained by dividing the force by (indenter size 200 μm = 0.2 mm) × (half the length of the circumference of the wire) = (wire diameter 0.02 mm × 3.14 / 2) is the compressive stress. Strictly speaking, at the point where the wire is deformed by 60%, the wire is not completely crushed into a thin layer, so that the vertical length of the cross-sectional area is not half the length of the circumference, but the measurement method with this value is adopted in the present invention because there is a slight difference between the measured value calculated with this cross-sectional area and the measured value strictly calculated with the cross-sectional area at 60% deformation and such a difference as to exceed the range of critical significance is not made. The compressive stress is expressed in a simple equation as follows.

**[0054]** Wire compressive stress (MPa) = Force applied at 60% deformation with respect to a wire diameter (N) / (Circumference ratio × Wire diameter (mm) / 2) × Indenter diameter (mm)

**[0055]** Also, as a precaution, after the compression of the wire, the wire after the test is collected and the shape of the indentation is observed using a scanning electron microscope. As illustrated in FIG. 5 (an attached SEM image), an indentation state is confirmed that the length of the indentation is ± 20% of the diameter of the indenter and the width of the crushed wire is symmetrical about the longitudinal axis of the wire. When these conditions are not satisfied, the measurement is performed again because the measured value may not be accurate. The measured value is set to the average value of three measured values, and the unit is set to MPa. Incidentally, when the output unit of the compression testing machine is $kgf/mm^2$, the value converted based on the conversion formula of 1 $kgf/mm^2$ = 9.8 MPa is applied. Further, the reason why the deformation

amount of compression is set to 60% of the wire diameter is because the average wire crushing ratio in wedge bonding is about 60%.

**[0056]** The Vickers hardness in the cross section of the core material 2 is measured as follows. That is, a plurality of wire samples are prepared by cutting the gold-coated bonding wire into a length of several centimeters. The wire sample is attached straight and evenly on a metal (Ag-plated frame) plate, while considering that the wire sample should not stretch or sag. After that, the wire sample is put into a cylindrical mold together with the metal plate so that the metal plate becomes the bottom of the cylinder, an embedding resin is poured into the mold, and then a curing agent is added to cure the resin. Then, the cured cylindrical resin containing the wire sample is roughly polished with a polisher so that the cross-sectional surface of the wire is exposed. Thereafter, the cut surface is finished by final polishing, and then the residual strain of the polished surface is removed by ion milling to obtain a smooth surface. Incidentally, an ion milling device is fine adjusted so that the cut surface of the wire is vertical to the longitudinal direction of the wire. The wire sample is fixed to a sample stage of a hardness testing machine (one example: HM-220 manufactured by Mitutoyo Corporation) so that the cross section of the wire sample (namely, the polished surface of the sample) is parallel to the sample stage, and the Vickers hardness is measured near the center of the cross section of the wire under the following conditions: a test force of 0.001 kgf, a load time of 4.0 seconds, a holding time of 10.0 seconds, an unloading time of 4.0 seconds, and an approaching speed of 60.0 um/sec. The above-described hardness measurement is performed on five wires, and the average value of the measurements is found.

**[0057]** In the gold-coated bonding wire 1, the content of the additive element in the entire wire 1 in the case where the core material 2 is formed of a silver alloy or copper alloy, the content of gold forming the coating layer 3 in the entire wire 1, the content of the additive element in the entire wire 1 in the case where the coating layer 3 is formed of a gold alloy, the content of palladium, platinum, or nickel forming the intermediate metal layer 4 in the entire wire 1, and the content of the additive element in the entire wire 1 in

the case where the intermediate metal layer 4 is formed of an alloy are measured as follows. That is, first, in order to calculate the content of gold, the bonding wire 1 is put into dilute nitric acid to dissolve the core material 2, and then a dissolution solution is collected. Hydrochloric acid is added to this dissolution solution, and ultrapure water is used to make a constant volume solution. Using this constant volume solution, inductively coupled plasma atomic emission spectroscopy (ICP-AES: Inductively Coupled Plasma Atomic Emission Spectroscopy) or inductively coupled plasma-mass spectrometry (ICP-MS: Inductively Coupled Plasma-Mass Spectrometry) is performed to measure the content of the additive element of the core material 2.

**[0058]** The thicknesses of the coating layer 3 and the intermediate metal layer 4 are measured as follows. That is, an elemental composition is analyzed from the surface of the gold-coated bonding wire 1 in the depth direction by a scanning auger electron spectroscopy (Auger Electron Spectroscopy: AES) analyzer (for example, product name: JAMP-9500F manufactured by JEOL Ltd.). The setting conditions of the AES analyzer are set as follows: an acceleration voltage of a primary electron beam of 10 kV, a current of 50 nA, a beam diameter of 5 μm, an acceleration voltage of argon ion sputtering of 1 kV, and a sputter rate of 2.5 nm/min (in terms of $SiO_2$). The analysis is performed from the surface of the gold-coated bonding wire 1 to a position where the detected concentration of the main component of the core material is 50 atom% or more in the depth direction, and the average concentration of gold with respect to the total of gold and silver or copper is found. When the intermediate metal layer 4 is provided, the average concentration of gold and the average concentration of an element M with respect to the total of the main forming element M of the intermediate metal layer 4 and gold and silver or copper are each found.

**[0059]** The coating layer 3 is defined as the region from the surface of the wire 1 to the point where the ratio of gold to the total of silver or copper and gold described above is 50.0 atom%, and the thickness of that region is found as the thickness of the coating layer 3. The point where the ratio of gold is 50.0 atom% is set to the boundary between the

core material 2 and the coating layer 3. The intermediate metal layer 4 is defined as the region from the point where the ratio of gold is 50.0 atomic% with respect to the total of silver or copper and gold and the element M described above to the point where the ratio of the element M is 50.0 atom%, and the thickness of that region is found as the thickness of the intermediate metal layer 4.

**[0060]** Next, there is explained a method of manufacturing the gold-coated bonding wire 1 in the embodiment. Incidentally, the method of manufacturing the gold-coated bonding wire in the embodiment is not particularly limited to the method of manufacturing described below. The gold-coated bonding wire 1 in the embodiment is obtained, for example, by forming a layer containing gold as a main component on the surface of a wire rod containing silver or copper as a main component, which serves as the core material 2, to form a wire raw material and drawing the wire raw material to a wire diameter required for the gold-coated bonding wire 1 and performing a heat treatment or the like thereon according to need. Further, in the case of the gold-coated bonding wire 1 including the intermediate metal layer 4, the gold-coated bonding wire 1 is obtained, for example, by sequentially forming a layer to be the intermediate metal layer 4 and a layer containing gold as a main component on the surface of the silver or copper wire rod that serves as the core material 2, to thereby form a wire raw material and drawing the wire raw material to a wire diameter required for the gold-coated bonding wire 1 and performing a heat treatment or the like thereon according to need.

**[0061]** When silver or copper is used as the core material 2, silver or copper of a predetermined purity is melted, and when a silver alloy or copper alloy is used, silver of a predetermined purity is melted together with an additive element, or copper of a predetermined purity is melted together with an additive element to obtain a silver core material or a copper core material. A heating furnace such as an arc heating furnace, a high-frequency heating furnace, a resistance heating furnace, or a continuous casting furnace is used for melting. The molten silver or molten copper in the heating furnace is preferably kept in a vacuum or an atmosphere of an inert gas such as argon or nitrogen in

order to prevent entry of oxygen and hydrogen from the atmosphere. The melted core material is solidified by continuous casting from the heating furnace so as to have a predetermined wire diameter, or the melted core material is cast into a mold to make an ingot, and the ingot is rolled. A heat treatment is applied according to need, and the core material is drawn to a predetermined wire diameter to obtain a silver wire rod or a copper wire rod (including a silver alloy wire rod and a copper alloy wire rod).

**[0062]** As a method of forming the layer to be the gold layer or the intermediate metal layer 4 on the surface of the silver wire rod or the copper wire rod, for example, a plating method (wet method) or a vapor deposition method (dry method) is used. The plating method may be either an electrolytic plating method or an electroless plating method. In the electrolytic plating such as strike plating or flash plating, the plating speed is high, and when it is applied to gold plating, good adhesion of the gold layer to the silver wire rod or the copper wire rod can be obtained. In order to contain an additive element in the gold layer or a palladium layer, a platinum layer, or a nickel layer as the intermediate metal layer 4 by the plating method, for example, in the above-described electrolytic plating, a plating solution containing a plating additive containing an additive element is used for a gold plating solution or a plating solution of the forming element of the intermediate metal layer 4. At this time, the amount of additive element in the coating layer 3 or the intermediate metal layer 4 can be adjusted by adjusting the type and amount of the plating additive.

**[0063]** As the vapor deposition method, physical vapor deposition (PVD) such as a sputtering method, an ion plating method, or a vacuum vapor deposition, or chemical vapor deposition (CVD) such as thermal CVD, plasma CVD, or a metal organic chemical vapor deposition method (MOCVD) can be used. According to these methods, cleaning the gold coating layer or the intermediate metal layer after formation is not required, and thus there is no concern about surface contamination or the like during cleaning. As a method of containing an additive element in the gold layer or a palladium layer, a platinum layer, or a nickel layer as the intermediate metal layer 4 by the vapor deposition method, there is

a method of forming a gold layer or an intermediate metal layer by magnetron sputtering or the like while using a gold target containing the additive element or a forming material target of the intermediate metal layer 4. Even in the case of applying other methods other than the above, it is only necessary to use a raw material containing a desired additive element in the gold material or the forming material of the intermediate metal layer 4.

**[0064]** Further, as another method, there is also a clad manufacturing method or the like, in which one like a tubular pipe is formed of a coating material in advance and a core material is inserted thereinto.

**[0065]** A working ratio of the wire drawing is determined according to the final diameter of the gold-coated bonding wire 1 to be manufactured, application, or the like. In general, the working ratio of wire drawing is preferably 90% or more as a working ratio until the process of working the silver wire rod or the copper wire rod to the final wire diameter. This working ratio can be calculated as a reduction ratio of a wire cross-sectional area. The wire drawing is preferably performed so as to reduce the wire diameter in stages by using a plurality of diamond dies. In this case, a reduction ratio of area (working ratio) per diamond die is preferably 5% or more and 15% or less.

**[0066]** After the silver wire rod or the copper wire rod coated with the gold layer and the forming material layer of the intermediate metal layer 4 is drawn to the final wire diameter, a final heat treatment is preferably performed. The final heat treatment is performed in consideration of a strain relief heat treatment for relieving strain of a metal structure remaining inside the wire 1 or required wire characteristics at the final wire diameter. Regarding the strain relief heat treatment, the temperature and the time are preferably determined in consideration of the required wire characteristics, which are the compressive stress of the wire 1 in particular. Besides, a heat treatment according to purposes may be performed in any stage of the wire manufacturing. Examples of such a heat treatment include a strain relief heat treatment during the drawing process of the wire, a diffusion heat treatment intended for improving adhesion after forming the gold layer or the forming material layer of the intermediate metal layer 4, and so on. By performing

the diffusion heat treatment, the adhesion between the core material 2 and the coating layer 3, or the like can be improved. As the heat treatment, a running heat treatment, in which a wire is passed through a heating atmosphere heated to a predetermined temperature to be heat treated, is preferred because the heat treatment conditions are adjusted easily. In the case of the running heat treatment, the heat treatment time can be calculated by the speed at which the wire passes and the distance of the wire passing in a heating device. An electric furnace or the like is used as the heating device. When inhibiting surface oxidation of the wire, it is also effective to heat the wire with a flow of an inert gas such as $N_2$ or Ar. If needed, a reducing mixed gas of $N_2$ and $H_2$ is used.

**[0067]** In the above-described manufacturing process of the gold-coated bonding wire 1, a compressive stress of 290 MPa or more and 590 MPa or less can be obtained by appropriately controlling manufacturing conditions such as heat treatment conditions, according to the composition of the metal material (silver-based material or copper-based material) forming the core material 2, the forming material or the thickness of the coating layer 3 and the intermediate metal layer 4 formed according to need, the diameter of the bonding wire 1, or the like. For example, the core material 2 is preferably formed of a silver alloy or copper alloy, and the compressive stress tends to increase as the amount of additive element in the silver alloy or the copper alloy increases. Further, the compressive stress tends to decrease as the thickness of the coating layer 3 is thicker. Further, the compressive stress tends to increase in the core material 2 using the copper alloy rather than in the core material 2 using the silver alloy.

**[0068]** It is preferable to select the heat treatment condition based on the tendency of the compressive stress based on the forming material of the gold-coated bonding wire 1 described above or other factors. The heat treatment is preferably performed at both the intermediate stage and the final stage. Regarding the final heat treatment, the compressive stress tends to decrease as the temperature is higher. Regarding the intermediate heat treatment as well, the compressive stress tends to decrease as the temperature is higher. Based on these points, when a material exhibiting a tendency to

have a high compressive stress is used as the forming material, the intermediate heat treatment temperature is preferably set to 400°C or more and 600°C or less, and the heat treatment time is preferably set to 0.2 seconds or more and 20 seconds or less. When a material exhibiting a tendency to have a low compressive stress is used as the forming material, the intermediate heat treatment temperature is preferably set to 200°C or more and less than 400°C, and the heat treatment time is preferably set to 0.2 seconds or more and 20 seconds or less. Furthermore, when a material exhibiting a tendency to have a high compressive stress is used as the forming material, the final heat treatment temperature is preferably set to 350°C or more and 650°C or less, and the heat treatment time is preferably set to 0.01 seconds or more and 5 seconds or less. When a material exhibiting a tendency to have a low compressive stress is used as the forming material, the final heat treatment temperature is preferably set to 150°C or more and 350°C or less, and the heat treatment time is preferably set to 0.01 seconds or more and 5 seconds or less.

**[0069]** Incidentally, even if the heat treatment conditions are the same, the compressive stress may be affected by the structure of a heat treatment device or the type and amount of additive element in the core material. In this respect, in the manufacturing process of the gold-coated copper bonding wire in this embodiment, it is possible to control the compressive stress of the wire by adjusting the elongation percentage in the heat treatment in the final heat treatment. In the case of the wire including, as a forming material, a core material containing copper as a main component, the elongation percentage is preferably adjusted to 5.0% or more and 20.0% or less, and it is more preferably 8.0% or more and 20.0% or less. In the case of the wire including, as a forming material, a core material containing silver as a main component, the elongation percentage is preferably adjusted to 1.5% or more and 15.0% or less, and it is more preferably 2.0% or more and 11.0% or less.

**[0070]** The elongation percentage is set to the value obtained by a tensile test of the bonding wire. The elongation percentage can be measured in accordance with JIS-Z2241 or JIS-Z2201. For example, when a bonding wire having a 10-cm length is pulled at a

speed of 20 mm/min and with a rated load cell of 2 N by a tensile test device (for example, AUTO COM manufactured by T·S·E Co., Ltd), the elongation percentage is calculated as the percentage of the elongated length when the wire breaks. As the elongation percentage, it is desired to find the average value of five wires in consideration of the variation in measurement results.

**[0071]** The following is a supplementary explanation of the above. Ideally, the final heat treatment conditions should be adjusted while measuring the compressive stress so that a final product falls within the target range of compressive stress, but from the viewpoint of simplifying the manufacturing work, here, the elongation percentage of the wire, which can be measured easily, is used as a rough indication for the compressive stress. As a matter of course, controlling the elongation percentage does not necessarily mean that the final product will fall within the target range of compressive stress.

**[0072]** (Semiconductor device)

Next, there is explained a semiconductor device using the gold-coated bonding wire 1 in the embodiment with reference to FIG. 6 to FIG. 8, FIG. 11, and FIG. 12. Incidentally, FIG. 6 is a cross-sectional view illustrating a stage of the semiconductor device in the embodiment before resin encapsulation, FIG. 7 is a cross-sectional view illustrating the resin-encapsulated semiconductor device in the embodiment, and FIG. 8 is a cross-sectional view illustrating a wedge bonding portion of the gold-coated bonding wire 1 bonded to an electrode of a semiconductor chip in the semiconductor device in the embodiment. FIG. 11 and FIG. 12 are cross-sectional views each illustrating a modified example of the semiconductor device in the embodiment.

**[0073]** A semiconductor device 10 in the embodiment (a semiconductor device 10X before resin encapsulation) includes, as illustrated in FIG. 6 and FIG. 7, a circuit board 12 including electrodes (substrate electrodes) 11, a plurality of semiconductor chips 14 (14A, 14B, and 14C) each including at least one electrode (chip electrode) 13, which are arranged on the circuit board 12, and bonding wires 15 (the gold-coated bonding wires 1) that connect the electrode 11 of the circuit board 12 and the electrode 13 of the semiconductor

chip 14 and connect the electrodes 13 of a plurality of the semiconductor chips 14. For the circuit board 12, for example, there is used a printed wiring board, a ceramic circuit board, or the like, in which a wiring network is provided on a surface or in the inside of an insulating base material such as a resin material or ceramic material and electrodes connected to the wiring network are provided on the surface.

**[0074]** Incidentally, FIG. 6 and FIG. 7 each illustrate the semiconductor device 10 including a plurality of the semiconductor chips 14 mounted on the circuit board 12, but the configuration of the semiconductor device 10 is not limited to this. For example, the semiconductor chip may be mounted on a lead frame, and in that case, the electrode of the semiconductor chip is connected to an inner lead functioning as an internal terminal (electrode) of the lead frame via the bonding wire 15. The number of semiconductor chips 14 to be mounted on the circuit board 12 or the lead frame may be either one or plural. The bonding wire 15 is applied to at least one of connection between the electrode 11 of the circuit board 12 and the electrode 13 of the semiconductor chip 14, connection between the lead frame and the electrode of the semiconductor chip, and connection between the electrodes 13 of a plurality of the semiconductor chips 14, and is wedge-bonded to at least one of these connections (two electrodes). As will be described later, when a plurality of the semiconductor chips 14 are stacked and mounted on the circuit board 12 or the lead frame in a stepped shape, it is also possible to continuously connect between a plurality of the semiconductor chips 14 and between the semiconductor chip 14 and the circuit board 2 by wedge bonding with the CWB using the single bonding wire 15.

**[0075]** The semiconductor chips 14A, 14C out of a plurality of the semiconductor chips 14 in the semiconductor device 10 illustrated in FIG. 6 and FIG. 7 are mounted on a chip mounting region of the circuit board 12 with a die-bonding material 16 provided therebetween. The semiconductor chip 14B is mounted on the semiconductor chip 14A with the die-bonding material 16 provided therebetween. Of the semiconductor chip 14A, one electrode 13 is connected to the electrode 11 of the circuit board 12 via the bonding wire 15, another electrode 13 is connected to one electrode 13 of the semiconductor chip

14B via the bonding wire 15, and another electrode 13 is connected to one electrode 13 of the semiconductor chip 14C via the bonding wire 15. Another electrode 13 of the semiconductor chip 14B is connected to the electrode 11 of the circuit board 12 via the bonding wire 15. Another electrode 13 of the semiconductor chip 14C is connected to the electrode 11 of the circuit board 12 via the bonding wire 15.

**[0076]** The semiconductor chip 14 includes an integrated circuit (IC) formed of a silicon (Si) semiconductor, a compound semiconductor, or the like. The chip electrode 13 is formed of an aluminum electrode having at least an aluminum (Al) layer or an aluminum alloy layer of AlSiCu, AlCu, or the like on the uppermost surface, for example. The aluminum electrode is formed by applying an electrode material such as Al or an Al alloy to a surface of a silicon (Si) substrate, for example, so as to be electrically connected to an internal wiring. The semiconductor chip 14 performs data communication with an external device and receives electric power from the external device via the substrate electrode 11 and the bonding wire 15.

**[0077]** The electrode 11 of the circuit board 12 is electrically connected to the electrode 13 of the semiconductor chip 14 mounted on the circuit board 12 via the bonding wire 15. In the semiconductor device 10 in the embodiment, the bonding wire 15 is formed of the gold-coated bonding wire 1 in the above-described embodiment. Of one of the bonding wires 15, one end thereof is ball-bonded to the chip electrode 13 (first bonding), and the other end thereof is wedge-bonded to the substrate electrode 11 (second bonding). The ball bonding and the wedge bonding may be opposite to each other, and one end of the bonding wire 15 may be ball-bonded to the substrate electrode 11 (first bonding) and the other end thereof may be wedge-bonded to the chip electrode 13 (second bonding). The same applies even to the case where the electrodes 13 of a plurality of the semiconductor chips 14 are connected by the bonding wire 15, and one end of the bonding wire 15 is ball-bonded to the chip electrode 13 (first bonding), and the other end thereof is wedge-bonded to another chip electrode 13 (second bonding). Incidentally, as the electrode 13 of the semiconductor chip 14 to be electrically bonded by the bonding wire

15, a bump bonded beforehand to the electrode of the semiconductor chip 14, (which is not illustrated), is also included.

**[0078]** In the wire connection by the bonding wire 15, for example, one end of the bonding wire 15 is melted by electrical discharge or the like to be solidified into a spherical shape by the surface tension or the like, and thereby a FAB is formed, and after this FAB is ball-bonded to the electrode 13 of the semiconductor chip 14, a bonding tool (capillary) is pulled up to form a loop, and while the bonding wire 15 being pressed against the electrode 11 of the circuit board 12, ultrasonic waves and load are applied to perform wedge bonding. As illustrated in FIG. 8, by forming a wedge bonding portion 17 on the substrate electrode 11 and then tearing off the bonding wire 15, connection at one position is completed. The same applies to the case where the electrodes 13 of the semiconductor chips 14 (the electrodes 13 having different built-in chips) are connected by the bonding wire 15. Thereafter, an encapsulating resin layer 18 is formed on the circuit substrate 12 so as to encapsulate a plurality of the semiconductor chips 14 and the bonding wires 15 with resin, and thereby the semiconductor device 10 is manufactured. Specific examples of the semiconductor device include a logic IC, an analog IC, a discrete semiconductor, a memory, an optical semiconductor, and so on.

**[0079]** In the semiconductor device 10 in the embodiment, as long as the gold-coated bonding wire 1 used as the bonding wire 15 has a compressive stress of 290 MPa or more and 590 MPa or less, the bonding wire 15 can be well wedge-bonded under a wide range of ultrasonic wave and load conditions, even if the electrode 11 of the circuit board 12 or the electrode 13 of the semiconductor chip 14, particularly, the chip electrode 13, is placed under positional conditions that are not suitable for bonding, such as a condition where there is no underlying support, for example, and thus it is possible to obtain a stable wedge bonding strength without damaging the semiconductor chip 14. Further, the wedge width can be controlled in an appropriate range, so that it is possible to inhibit a short circuit and other problems between narrow-pitched electrodes. These make it possible to provide a semiconductor device having improved connection reliability between electrodes by the

bonding wire 15.

**[0080]** Next, there is explained another semiconductor device 1 with reference to FIG. 11 and FIG. 12. A semiconductor device 1 illustrated in FIG. 11 includes four semiconductor chips 14A, 14B, 14C, and 14D stacked in multiple stages on the circuit board 12. These semiconductor chips 14A, 14B, 14C, and 14D are stacked in a stepped shape so as to make their electrodes 13 exposed. The electrodes 13 of the semiconductor chips 14A, 14B, 14C, and 14D and the electrode 11 of the circuit board 12 are continuously connected by the single bonding wire 15. That is, the four electrodes 13 and the substrate electrode 11 are connected by the CWB with the single bonding wire 15. Incidentally, the arrow indicates the bonding direction.

**[0081]** Specifically, the bonding wire 15 held by a bonding tool (capillary) is first wedge-bonded to the electrode 13 of the uppermost-stage semiconductor chip 14D. Then, the bonding wire 15 is moved onto the electrode 13 of the semiconductor chip 14C and wedge-bonded thereto while pulling up the bonding tool (capillary) to form a loop without tearing off the bonding wire 15. Similarly, the bonding wire 15 is wedge-bonded to the electrode 13 of the semiconductor chip 14B and the electrode 13 of the semiconductor chip 14A in order without tearing off the bonding wire 15. After the bonding wire 15 is wedge-bonded to the electrodes 13 of the semiconductor chips 14D, 14C, 14B, and 14A in order, the bonding wire 15 is wedge-bonded to the electrode 11 of the circuit board 12 in the same manner, and then the bonding wire 15 is torn off. In this manner, the electrodes 13 of the semiconductor chips 14A, 14B, 14C, and 14D and the electrode 11 of the circuit board 12 are continuously connected by the single bonding wire 15 without tearing off the bonding wire 15 in the middle.

**[0082]** By continuously wedge-bonding the single bonding wire 15 to the four chip electrodes 13 and the substrate electrode 11 described above and electrically connecting them, the number of times of ball formation and the number of times of wire tearing can be reduced, and therefore, it is possible to speed up the bonding speed and improve the productivity based on the speeding up. In performing the continuous wedge bonding, the

wedge bondability of the bonding wire 15 is important. With respect to such a point, since the gold-coated bonding wire 1 having a compressive stress of 290 MPa or more and 590 MPa or less is used as the bonding wire 15, the bondability to the electrodes 13 and 11 in continuous wedge bonding can be improved. Therefore, it is possible to well perform the wedge bonding on the chip electrode 13 under a wide range of bonding conditions without damaging the semiconductor chip 14. Accordingly, the productivity and reliability of the semiconductor device 10 to which the CWB is applied can be improved.

**[0083]** The wire bonding to which the CWB is applied is not limited to the structure illustrated in FIG. 11. For example, as illustrated in FIG. 12, the bonding wire 15 may be ball-bonded to the substrate electrode 11 of the lowermost-stage circuit board 12 to form a ball bonding portion 19, and the bonding wire 15 may be wedge-bonded to the electrodes 13 of the semiconductor chips 14A, 14B, 14C, and 14D in order without tearing off the bonding wire 15, and then the bonding wire 15 may be torn off. Even in such a semiconductor device 10 to which the CWB is applied, the continuous wedge bondability can be improved based on the effect of improving the wedge bondability of the bonding wire 15, and the productivity and reliability of the semiconductor device 10 to which the CWB is applied can be improved. The arrow indicates the bonding direction.

**[0084]** In the semiconductor device 10 in the embodiment, when connecting two electrodes by the bonding wire 15, the bonding wire 15 is only required to be wedge-bonded to at least one of the two electrodes, thereby making it possible to exhibit the effect of improving the wedge bondability by the gold-coated bonding wire 1 in the embodiment, the effect of improving the bonding strength and bonding reliability of the wedge bonding based on the effect, and the like. However, in order to more effectively exhibit the effect of improving the wedge bondability by the gold-coated bonding wire 1 in the embodiment, at least one of the two electrodes connected by the bonding wire 15 is suitable to be the electrode 13 of the semiconductor chip 14, and the semiconductor device 10 in the embodiment is suitable to be the semiconductor device 10 in which wedge bonding is performed on such a chip electrode 13. In particular, the semiconductor device 10 in the

embodiment is suitable for the semiconductor device in which the CWB is applied and wire bonding is performed, as illustrated in FIG. 11 and FIG. 12, and in such a case, good wedge bondability and good bonding strength and bonding reliability based the wedge bondability can be exhibited more effectively.

EXAMPLE

**[0085]** Next, there will be explained examples of the present invention. The present invention is not limited to the following examples.

**[0086]** (Manufacturing method and Attribute of examples)

Core materials illustrated in Table 1 were prepared and worked to an intermediate wire diameter of 0.2 to 0.5 mm by continuous wire drawing, and then each of the core materials was immersed in a gold electroplating bath while being fed continuously, to form a gold coating layer with the electric current with a current density of 0.15 to 2.00 A/dm$^2$.

**[0087]** In Examples 16 to 19, 21, and 31 to 36, before forming the gold coating layer, an intermediate layer illustrated in Table 1 was formed by the same electrolytic plating method. In Examples 1 to 19, intermediate wire drawing was performed to an intermediate wire diameter of ϕ 38 μm to 100 μm, and in Examples 22 to 36, intermediate wire drawing was performed to an intermediate wire diameter of ϕ 50 μm to 200 μm, and a heat treatment was performed at an intermediate heat treatment temperature illustrated in Table 1 (a set temperature of an electric furnace) at a wire feed speed of 0.20 to 1.00 m/sec. It takes about 0.5 to 3 seconds for the heat treatment in terms of time. Thereafter, each of the core materials was drawn to a final wire diameter illustrated in Table 1, and a final heat treatment was performed by adjusting the heat treatment temperature and the wire feed speed to achieve an elongation percentage illustrated in Table 1. In this way, gold-coated bonding wires in Examples 1 to 34 were fabricated.

**[0088]** For these completed gold-coated bonding wires, the compressive stress and the Vickers hardness of the cross section of the core material were measured by the methods described above, and the results are illustrated in Table 1. The gold-coated bonding wires obtained as above were subjected to characteristic evaluations to be described later.

**[0089]** (Manufacturing method and Attribute of comparative examples)

Comparative examples will be explained. A bonding wire having a compressive stress falling outside of the present invention range is described in Comparative examples 1 to 6 and 11 to 18, and a bonding wire on which a coating layer other than gold is formed is described in Comparative examples 10, 19, and 20. Further, a bonding wire on which no coating layer is formed is described in Comparative examples 7 to 9. Bonding wires in Comparative examples 1 to 20 were fabricated by the same manufacturing method as in the examples basically, except for the above changes. The compressive stress and the Vickers hardness of the cross section of these bonding wires were measured by the methods described above as in the examples, and the results are illustrated in Table 1. The bonding wires obtained as above were subjected to characteristic evaluations to be described later.

**[0090]** (Wedge bondability evaluation of the examples and the comparative examples)

There will be explained wedge bondability evaluation of samples fabricated as above. There are two types of wedge bonding partners: the electrode on the circuit board and the chip electrode. Details will be described below, but three evaluation items are as follows: whether or not problems occur during continuous bonding (continuous bondability); whether or not bonding is properly bonded (bonding strength); and whether or not a chip is damaged, and these three evaluations were made. The evaluation results are illustrated in Table 1 and Table 2. However, regarding the chip damage evaluation, only the delicate and fragile chip electrodes were used.

**[0091]** (Bonding energy in the wedge bondability evaluation)

As described above, when the bonding wire is wedge-bonded to the electrodes of multistage stacked chips, in particular, a wide range of variously different bonding conditions are required because the bonding wire must be firmly bonded without causing chip cracking depending on the bonding position, location, or the like. As an index to measure the adaptability of wire, the bonding energy is suitable as an evaluation method, and it is confirmed whether the wires can pass the above-described three evaluation items

without any problem even if the bonding energy condition is widely set.

**[0092]** Roughly speaking, the bonding energy depends on the crushing ratio of the wire. For example, in order to crush the wire significantly, the conditions such as a load pressure on the wire, a load time, and ultrasonic waves must be comprehensively increased. Here, the bonding energy is classified into three levels according to the crushing ratio with respect to the wire diameter ((crushed wire thickness/wire diameter before crushing) × 100) (%). That is, the crushing ratio of the wire, which is 47% or more and 53% or less, is defined as low bonding energy, the crushing ratio of the wire, which is 57% or more and 63% or less, is defined as medium bonding energy, and the crushing ratio of the wire, which is 67% or more and 73% or less, is defined as high bonding energy. These bonding energy conditions were adjusted by a bonder apparatus (IConn PLUS manufactured by Kulicke & Soffa Industries, Inc.).

**[0093]** As described above, there are two types of wedge bonding, namely, the wedge bonding to the electrode of the circuit board and the wedge bonding to the chip electrode, and the wedge bonding to the electrode of the circuit board is well supported and is not brought into a situation where the bonding environment varies as in the wedge bonding to the chip electrode, and therefore, the wedge bondability was evaluated only under the condition of high bonding energy here. On the other hand, the chip electrode is likely to be subjected to a variety of bonding environments, and thus, the wedge bondability was evaluated under the conditions of low-level, medium-level, and high-level bonding energies.

**[0094]** Furthermore, in order to simulate a severe bonding environment close to the mounting level of continuous wedge bonding of more severe and delicate multistage stacked chip electrodes, as the chips used in Table 1, chips having a lower adhesion of an Al electrode than a general-purpose chip were adopted. The cross-sectional structure of this chip has an insulating film ($SiO_2$ film) on a Si substrate, and an Al film is formed on the $SiO_2$ film. On the other hand, the cross-sectional structure of the general-purpose chip has a structure in which an insulating film (TEOS: tetraethoxysilane) is provided on a Si

substrate and a TiN layer is provided between the insulating film and an Al electrode to improve the adhesion of the Al electrode. By adopting this chip, the situation and conditions such that chip damage or chip electrode (pad) damage (a phenomenon in which the Al electrode is peeled off from the chip during a looping operation after wedge bonding) is likely to occur are made. Incidentally, the thickness of the electrode was set to 0.8 μm, and the material of the electrode was set to Al-0.5%Cu or Al-1%Si-0.5%Cu.

**[0095]** (Continuous bondability of the wedge bonding on the substrate electrode)

The wedge bondability on the substrate electrode was evaluated by continuous wire bonding to the chip electrode and the substrate electrode (lead frame). As for the wedge bonding conditions, wedge bonding was performed on an Ag-plated lead frame at 72 positions in total, which were 36 cycles × 2 sets, under the high bonding condition described above. Here, one cycle refers to the process from ball bonding on the chip electrode to wedge bonding on the frame and wire tearing, and this cycle was performed 36 times in succession for two sets. The case where the device did not stop due to a problem such as non-bonding of the wedge bonding portion or wire breakage out of 72 times of bonding in total was marked as "A" because the continuous bondability was good. The case where the device stopped less than twice due to a problem of the wedge bonding portion was marked as "B" because improvement is possible in a mass production process. The case where the device stopped two or more times was regarded as failure and marked as "C."

**[0096]** (Pull test on the substrate electrode = Bonding strength evaluation)

In a sample in which the wedge bonding was performed by the aforementioned wire bonding under the aforementioned condition, 20 wires were randomly selected, and using a bond tester (one example: Bondtester Model 4000 manufactured by DAGE), a pull test was performed on each of the wires by hooking the portion near the wedge bonding of the sample to check the presence or absence of a lift (that is one of breakage modes). The setting conditions of the bond tester were set to a load cell of WP100, a measurement range of 50%, and a test speed of 250 μm/min. In the breakage mode of the pull test, the case

where there was no occurrence of lift that causes the wire at the bonding portion to peel off from the board was regarded as good and marked as “A.” The case where less than three lifts occurred was marked as “B” because improvement is possible in a mass production process. The case where three or more lifts occurred was regarded as failure and marked as “C.” Further, the case where at least one wire having a pull strength of less than 2 gf occurred was also regarded as failure and marked as “C.”

**[0097]** (Continuous bondability of wedge bondability on the chip electrode)

For this evaluation, a device with the aforementioned chips mounted on an Ag-plated lead frame was used. By using the CWB method, continuous wedge bonding was performed on the aforementioned chips with 360 wires (10 wires/cycle × 36 cycles). The aforementioned wedge bonding conditions (three levels of low bonding energy, medium bonding energy, and high bonding energy) are provided in one cycle, and each one cycle has three wires/wedge bonding conditions × wedge bonding of three levels (the first bonding is performed by ball bonding, and thus, 9 wedge bonding points are made for one cycle). Therefore, as the wires bonded at each level per chip, 108 wires were used (the number of wedge bondings: 108 bonds = 3 wires × 36 cycles). The capillary shape for wedge bonding was set as follows: H diameter: 1.2 to 1.3 times the wire diameter, CD diameter: 1.5 to 1.8 times the wire diameter, T: 3.5 to 3.8 times the wire diameter, FA: 0°, and OR diameter: 4 to 12 μm, and Matte specifications for surface finishing were used. The case where the device did not stop due to a problem such as non-bonding of the wedge bonding portion, peeling off of the Al film, or wire breakage was marked as “A” because the continuous bondability of the wedge bonding at each bonding energy was good. The case where the device stopped less than five times due to a problem of the wedge bonding portion at each bonding energy was marked as “B” because improvement is possible in a mass production process. The case where the aforementioned device stopped five times or more was marked as “C” because the wedge bondability at this bonding energy was bad.

**[0098]** (Pull test on the chip electrode = Bonding strength evaluation)

In a sample fabricated by performing wedge bonding on the aforementioned chip,

out of 108 wires, 20 wires were randomly selected, and by a bond tester (one example: Bondtester Model 4000 manufactured by DAGE), a pull test in which the sample was hooked and pulled was performed on each of the wires for each bonding energy condition to check the breakage mode. The setting conditions of the bond tester were set to a load cell of WP100, a measurement range of 50%, and a test speed of 250 μm/min. In the breakage mode of the pull test, the case where there was no occurrence of lift that causes the wire at the bonding portion to peel off from the chip electrode was marked as "A" because the wedge bonding strength at this bonding energy was good. The case where less than three lifts occurred was marked as "B" because improvement is possible in a mass production process. The case where three or more lifts occurred was marked as "C" because the wedge bonding strength at this bonding energy was bad.

**[0099]** (Chip damage evaluation)

For this evaluation, a device with the aforementioned chips mounted on an Ag-plated lead frame was used, and by using the CWB method, continuous bonding was performed on the aforementioned chips with 64 wires (16 wires/cycle × 4 sets). The aforementioned wedge bonding conditions (three levels of low bonding energy, medium bonding energy, and high bonding energy) are provided in one cycle, and five wires each were assigned to three bonding energy levels per cycle (similarly to the above, the first bonding was performed by ball bonding, and thus, 15 wedge bonding points in total were made). As the wires bonded at each level per chip, 20 wires were used (the number of wedge bondings: 20 bonds = 5 wires × 4 cycles). As the capillary for wedge bonding, the same one as in paragraph [0095] was used.

**[0100]** After bonding, in order to dissolve the chip electrode and expose the chip base, the sample in which the wedge bonding was performed was immersed in an aqueous sodium hydroxide solution for about 30 minutes to confirm that the wire was peeled off from the chip, and then the sample was washed with pure water, washed with alcohol, and dried in that order, and then the exposed chip base (Si or $SiO_2$) was observed at 10 randomly selected bonding portions made at each bonding energy level by an optical

microscope. The case where there was no pad (chip electrode) cracking was marked as "A" because the wedge bondability at the bonding energy was good. The case where at least single pad cracking occurred was marked as "C" because the wedge bondability at the bonding energy was bad.

**[0101]** Regarding the wedge bondability in Table 1 and Table 2, the case where there was at least one failure "C" in the above-described evaluation items of continuous bondability, bonding strength, and chip damage was evaluated as a rejection in the overall evaluation because it is estimated that the sample was not able to support continuous wedge bonding in a multistage stacked structure. Further, the case where there was no evaluation of "C" was evaluated as a pass in the overall evaluation.

**[0102]** [Table 1]

| | Sample number | Bonding wire attribute | | | | | | | | | | | Wedge bondability evaluation | | | | | | | | | | | Overall evaluation |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Manufacturing process | | Wire diameter (μm) | Skin layer | Intermediate layer | | Core material | | | | Compressive stress (MPa) | Wedge bondability on substrate electrode | | Wedge bondability on chip electrode | | | | | | | | | |
| | | Intermediate heat treatment | Final characteristic target value | | | | | | | | | | | | Continuous bondability | | | Bonding strength (pull test) | | | Chip damage | | | |
| | | Temperature (°C) | Elongation percentage (%) | | Au film thickness (nm) | Main component | Film thickness (nm) | Main component | Main component concentration (mass%) | Additive element | Cross section hardness (Hv) | | Continuous bondability | Bonding strength | Low bonding energy | Medium bonding energy | High bonding energy | Low bonding energy | Medium bonding energy | High bonding energy | Low bonding energy | Medium bonding energy | High bonding energy | |
| Example | 1 | 350 | 7.7 | 20 | 112 | - | - | Ag | 99.9 | Pd | 40 | 290 | A | A | A | A | A | A | A | A | A | A | A | Pass |
| | 2 | 500 | 5.8 | 20 | 80 | - | - | Ag | 99.0 | Pd | 60 | 353 | A | A | A | A | A | A | A | A | A | A | A | Pass |
| | 3 | 450 | 2.1 | 20 | 116 | - | - | Ag | 97.0 | Pd | 80 | 588 | A | A | A | A | A | A | A | A | A | A | A | Pass |
| | 4 | 550 | 2.6 | 15 | 15 | - | - | Ag | 99.0 | Pd | 67 | 343 | A | A | A | A | A | A | A | A | A | A | A | Pass |
| | 5 | 550 | 4.3 | 20 | 72 | - | - | Ag | 98.0 | Pd | 49 | 372 | A | A | A | A | A | A | A | A | A | A | A | Pass |
| | 6 | 600 | 7.1 | 15 | 5 | - | - | Ag | 99.0 | Pt | 45 | 323 | A | A | B | B | B | B | B | B | A | A | A | Pass |
| | 7 | 550 | 4.4 | 20 | 11 | - | - | Ag | 99.0 | Pd | 85 | 500 | A | A | B | B | B | B | B | B | A | A | A | Pass |
| | 8 | 500 | 6.0 | 30 | 200 | - | - | Ag | 99.5 | Pd | 55 | 323 | A | A | A | A | A | A | A | A | A | A | A | Pass |
| | 9 | 600 | 7.3 | 20 | 64 | - | - | Ag | 99.0 | Pt | 43 | 304 | A | A | A | A | A | A | A | A | A | A | A | Pass |
| | 10 | 500 | 3.2 | 20 | 152 | - | - | Ag | 98.5 | Pt | 73 | 431 | A | A | A | A | A | A | A | A | A | A | A | Pass |
| | 11 | 400 | 2.2 | 20 | 97 | - | - | Ag | 99.0 | Ni | 79 | 568 | A | A | A | A | A | A | A | A | A | A | A | Pass |
| | 12 | 250 | 5.4 | 20 | 56 | - | - | Ag | 99.99 | - | 53 | 314 | A | A | A | A | A | A | A | A | A | A | A | Pass |
| | 13 | 300 | 3.5 | 20 | 160 | - | - | Ag | 99.95 | Cu | 62 | 363 | A | A | A | A | A | A | A | A | A | A | A | Pass |
| | 14 | 500 | 4.0 | 20 | 138 | - | - | Ag | 99.8 | In | 53 | 314 | A | A | A | A | A | A | A | A | A | A | A | Pass |
| | 15 | 450 | 3.8 | 20 | 108 | - | - | Ag | 99.6 | In | 58 | 343 | A | A | A | A | A | A | A | A | A | A | A | Pass |
| | 16 | 500 | 5.7 | 20 | 121 | Pd | 7 | Ag | 99.99 | Cu | 57 | 333 | A | A | A | A | A | A | A | A | A | A | A | Pass |
| | 17 | 600 | 5.1 | 20 | 83 | Pd | 22 | Ag | 99.0 | Pd | 68 | 402 | A | A | A | A | A | A | A | A | A | A | A | Pass |
| | 18 | 550 | 3.1 | 20 | 60 | Ni | 4 | Ag | 99.99 | Ca | 78 | 540 | A | A | A | A | A | A | A | A | A | A | A | Pass |
| | 19 | 500 | 4.6 | 20 | 78 | Ni | 15 | Ag | 99.5 | Au | 77 | 451 | A | A | A | A | A | A | A | A | A | A | A | Pass |
| | 20 | - | 10.8 | 20 | 115 | - | - | Ag | 99.0 | Pd | 54 | 382 | A | A | A | A | A | A | A | A | A | A | A | Pass |
| | 21 | - | 15.8 | 20 | 95 | Pd | 9 | Cu | 99.99 | - | 71 | 539 | A | A | A | A | A | A | A | A | A | A | A | Pass |
| | 22 | 600 | 18.7 | 20 | 101 | - | - | Cu | 99.999 | P | 45 | 343 | A | A | A | A | A | A | A | A | A | A | A | Pass |
| | 23 | 500 | 13.0 | 20 | 115 | - | - | Cu | 99.9 | Ni | 68 | 519 | A | A | A | A | A | A | A | A | A | A | A | Pass |
| | 24 | 600 | 8.9 | 20 | 98 | - | - | Cu | 98.0 | Ni | 77 | 590 | A | A | A | A | A | A | A | A | A | A | A | Pass |
| | 25 | 550 | 10.5 | 15 | 15 | - | - | Cu | 99.99 | - | 66 | 500 | A | A | A | A | A | A | A | A | A | A | A | Pass |
| | 26 | 550 | 15.4 | 20 | 85 | - | - | Cu | 99.99 | P | 63 | 480 | A | A | A | A | A | A | A | A | A | A | A | Pass |
| | 27 | 450 | 19.8 | 30 | 200 | - | - | Cu | 99.95 | P | 71 | 539 | A | A | A | A | A | A | A | A | A | A | A | Pass |
| | 28 | 500 | 12.7 | 20 | 61 | - | - | Cu | 99.0 | Pt | 64 | 490 | A | A | A | A | A | A | A | A | A | A | A | Pass |
| | 29 | 500 | 11.1 | 20 | 124 | - | - | Cu | 99.5 | Ni | 69 | 529 | A | A | A | A | A | A | A | A | A | A | A | Pass |
| | 30 | 450 | 9.9 | 20 | 36 | - | - | Cu | 99.0 | Pt | 80 | 549 | A | A | A | A | A | A | A | A | A | A | A | Pass |
| | 31 | 600 | 16.6 | 20 | 161 | Pt | 1 | Cu | 99.99 | - | 49 | 372 | A | A | A | A | A | A | A | A | A | A | A | Pass |
| | 32 | 580 | 17.2 | 20 | 189 | Pt | 33 | Cu | 99.995 | Ag | 60 | 461 | A | A | A | A | A | A | A | A | A | A | A | Pass |
| | 33 | 550 | 14.2 | 20 | 77 | Pd | 18 | Cu | 99.995 | Ag | 67 | 510 | A | A | A | A | A | A | A | A | A | A | A | Pass |
| | 34 | 580 | 10.8 | 20 | 156 | Pd | 53 | Cu | 99.99 | P | 75 | 568 | A | A | A | A | A | A | A | A | A | A | A | Pass |
| | 35 | 550 | 12.0 | 20 | 144 | Ni | 29 | Cu | 99.99 | - | 63 | 480 | A | A | A | A | A | A | A | A | A | A | A | Pass |
| | 36 | 500 | 8.4 | 20 | 176 | Ni | 60 | Cu | 99.999 | Fe | 73 | 559 | A | A | A | A | A | A | A | A | A | A | A | Pass |

**[0103]** [Table 2]

| | Sample number | Bonding wire attribute | | | | | | | | | | | Wedge bondability evaluation | | | | | | | | | | | Overall evaluation |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Manufacturing process | | Wire diameter (μm) | Skin layer | Intermediate layer | | Core material | | | Compressive stress (MPa) | | Wedge bondability on substrate electrode | | Wedge bondability on chip electrode | | | | | | | | | |
| | | Intermediate heat treatment | Final characteristic target value | | Au film thickness (nm) | Main component | Film thickness (nm) | Main component | Main component concentration (mass%) | Additive element | Cross section hardness (Hv) | | Continuous bondability | Bonding strength | Continuous bondability | | | Bonding strength (pull test) | | | Chip damage | | | |
| | | Temperature (°C) | Elongation percentage (%) | | | | | | | | | | | | Low bonding energy | Medium bonding energy | High bonding energy | Low bonding energy | Medium bonding energy | High bonding energy | Low bonding energy | Medium bonding energy | High bonding energy | |
| Comparative example | 1 | 650 | 20.9 | 20 | 11 | - | - | Ag | 99.0 | Pt | 36 | 255 | B | C | B | B | B | C | C | C | A | A | A | Reject |
| | 2 | 610 | 21.5 | 20 | 75 | - | - | Ag | 99.99 | - | 33 | 235 | B | C | B | B | B | C | C | C | A | A | A | Reject |
| | 3 | 625 | 23.2 | 30 | 206 | - | - | Ag | 99.9 | Pd | 39 | 274 | B | C | B | B | B | C | C | C | A | A | A | Reject |
| | 4 | - | 1.2 | 15 | 10 | - | - | Ag | 99.0 | Pd | 89 | 637 | B | B | B | B | B | B | B | C | C | C | C | Reject |
| | 5 | - | 1.3 | 20 | 104 | - | - | Ag | 98.0 | Pd | 85 | 617 | B | B | B | B | B | B | B | C | C | C | C | Reject |
| | 6 | - | 1.1 | 30 | 255 | - | - | Ag | 97.0 | Ni | 97 | 686 | B | B | B | B | B | B | B | C | C | C | C | Reject |
| | 7 | 550 | 3.3 | 20 | - | - | - | Ag | 99.0 | Pd | 67 | 392 | C | B | C | C | C | C | B | B | A | A | A | Reject |
| | 8 | 600 | 5.1 | 20 | - | - | - | Ag | 95.0 | Pd | 74 | 549 | C | B | C | C | C | C | B | B | A | A | A | Reject |
| | 9 | 600 | 4.5 | 20 | - | - | - | Ag | 90.0 | Au · Pd | 79 | 578 | C | B | C | C | C | C | B | B | A | A | A | Reject |
| | 10 | 450 | 2.6 | 20 | - | Pd | 84 | Ag | 98.5 | Pd | 62 | 441 | C | B | C | C | C | C | B | B | A | A | A | Reject |
| | 11 | 650 | 24.1 | 20 | 4 | - | - | Cu | 99.5 | Pt | 40 | 284 | B | C | B | B | B | C | C | C | A | A | A | Reject |
| | 12 | 650 | 22.8 | 20 | 97 | - | - | Cu | 99.999 | - | 37 | 265 | A | C | B | A | A | C | C | C | A | A | A | Reject |
| | 13 | 650 | 30.3 | 30 | 211 | - | - | Cu | 99.99 | P | 39 | 274 | A | C | B | A | A | C | C | C | A | A | A | Reject |
| | 14 | - | 4.7 | 15 | 8 | Pd | 52 | Cu | 99.99 | - | 85 | 608 | B | A | C | C | B | B | B | B | C | C | C | Reject |
| | 15 | - | 5.9 | 20 | 131 | - | - | Cu | 98.0 | Ni | 91 | 647 | A | A | B | B | B | B | B | B | C | C | C | Reject |
| | 16 | - | 7.2 | 30 | 224 | - | - | Cu | 99.99 | P | 99 | 706 | A | A | B | B | B | B | B | B | C | C | C | Reject |
| | 17 | - | 3.8 | 20 | 90 | Pd | 13 | Cu | 99.9 | Ni | 94 | 666 | A | A | B | B | B | B | B | B | C | C | C | Reject |
| | 18 | - | 5.0 | 20 | 64 | Ni | 22 | Cu | 99.5 | Pd | 96 | 686 | A | A | B | B | B | B | B | B | C | C | C | Reject |
| | 19 | 500 | 11.3 | 20 | - | Pd | 75 | Cu | 99.99 | - | 73 | 519 | C | B | C | C | C | C | C | C | A | A | A | Reject |
| | 20 | 500 | 8.7 | 20 | - | Ni | 55 | Cu | 99.99 | - | 76 | 540 | C | B | C | C | C | C | C | C | A | A | A | Reject |

**[0104]** Table 2 reveals that the gold-coated bonding wires each having a compressive stress of less than 290 MPa or greater than 590 MPa have poor wedge bondability on the substrate electrode and the chip electrode both in the case of using a silver core material (Comparative examples 1 to 6) and the case of using a copper core material (Comparative examples 11 to 18). Further, it reveals that the bonding wires including no gold coating layer formed thereon and the bonding wires including a coating layer other than gold coated also have poor wedge bondability on the substrate electrode and the chip electrode. In particular, all the bonding wires in the comparative examples have at least one or more failure "C" in the evaluation of continuous bondability, pull test, or chip damage, so that it is conceived that these wires will fail to overcome the technical problems for the bonding wires in the CWB including continuous multistage wedge bonding.

**[0105]** In contrast to this, as illustrated in Table 1, it reveals that the gold-coated bonding wires in Examples 1 to 36 having a compressive stress of 290 MPa or more and 590 MPa or less all have excellent wedge bondability on the substrate electrode and the chip electrode. In particular, in the evaluation of wedge bondability on the chip electrode, the evaluations of continuous bondability, pull test, and chip damage are all good even under the wedge bonding conditions with a mixture of low, medium, and high bonding energy levels, and the present inventors conclude that sufficient results were obtained to overcome the technical problems with the soft side (bonding wire) in the CWB.

**[0106]** According to the present invention, it is believed that it is possible to make a significant contribution to the development of the semiconductor industry, electronics industry, and so on by providing the bonding wire with reduced material and production costs in response to the conflicting market needs for large storage capacity and miniaturization, as typified by semiconductor memory in particular.

EXPLANATION OF REFERENCE NUMERALS

**[0107]** 1...gold-coated bonding wire, 2...core material, 3...coating layer, 4...intermediate metal layer, 10...semiconductor device, 11...substrate electrode, 12...circuit board, 13...chip electrode, 14, 14A, 14B, 14C, 14D...semiconductor chip, 15...bonding

wire, 16...die bonding material, 17...wedge bonding portion, 18...encapsulating resin layer, 19...ball bonding portion.

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CLAIMS

1. A gold-coated bonding wire, comprising:

a core material containing silver or copper as a main component; and

a coating layer provided on a surface of the core material, the coating layer containing gold as a main component, wherein

the gold-coated bonding wire has a film thickness of the coating layer of 5 nm or more and 200 nm or less, and

the gold-coated bonding wire has a compressive stress of 290 MPa or more and 590 MPa or less when deformed by 60% with respect to a wire diameter.

2. The gold-coated bonding wire according to claim 1, wherein

the core material has a Vickers hardness (Hv) of 40 or more and 80 or less in a cross section thereof.

3. The gold-coated bonding wire according to claim 1 or claim 2, wherein

the core material is made of a silver alloy containing 97 mass% or more of silver and contains at least one metal selected from the group consisting of copper, calcium, phosphorus, gold, palladium, platinum, nickel, rhodium, indium, and iron in the range of 1 mass ppm or more and 3 mass% or less with respect to the total amount of the wire.

4. The gold-coated bonding wire according to claim 1 or claim 2, wherein

the core material is made of a copper alloy containing 98 mass% or more of copper and contains at least one metal selected from the group consisting of phosphorus, gold, palladium, platinum, nickel, silver, rhodium, indium, gallium, and iron in the range of 1 mass ppm or more and 2 mass% or less with respect to the total amount of the wire.

5. The gold-coated bonding wire according to any one of claims 1 to 4,

wherein

the gold-coated bonding wire has a diameter of 13 μm or more and 35 μm or less.

6. The gold-coated bonding wire according to any one of claims 1 to 5, further comprising:

an intermediate metal layer provided between the core material and the coating layer, the intermediate metal layer containing one metal selected from the group consisting of palladium, platinum, and nickel as a main component.

7. The gold-coated bonding wire according to claim 6, wherein

the intermediate metal layer has a thickness of 60 nm or less.

8. The gold-coated bonding wire according to any one of claims 1 to 7, being for semiconductor memory.

9. A method of manufacturing a gold-coated bonding wire, the gold-coated bonding wire including:

a core material containing silver or copper as a main component; and

a coating layer provided on a surface of the core material, the coating layer containing gold as a main component, the method comprising:

setting a film thickness of the gold-coated bonding wire to 5 nm or more and 200 nm or less; and

setting a compressive stress to 290 MPa or more and 590 MPa or less.

10. A semiconductor wire bonding structure, comprising:

a gold-coated bonding wire including:

a core material containing silver or copper as a main component; and

a coating layer containing gold as a main component;

an electrode of a semiconductor chip; and

a wedge bonding portion where the wire and the electrode are bonded, wherein

the coating layer has a film thickness of 5 nm or more and 200 nm or less, and

the gold-coated bonding wire has a compressive stress of 290 MPa or more and 590 MPa or less when deformed by 60% with respect to a wire diameter.

11. The semiconductor wire bonding structure according to claim 10, further comprising:

two or more of the semiconductor chips; and

two or more of the wedge bonding portions where the electrodes of the two semiconductor chips and the wire are connected in sequence.

12. The semiconductor wire bonding structure according to claim 9 or claim 10, being for semiconductor memory.

13. A semiconductor device, comprising:

one or a plurality of semiconductor chips, the semiconductor chip including at least one first electrode;

a circuit substrate that is selected from a lead frame and a circuit board including at least one second electrode;

a gold-coated bonding wire configured to electrically connect at least one selected from between the first electrode of the semiconductor chip and the second electrode of the circuit substrate and between the first electrodes of a plurality of the semiconductor chips; and

a wedge bonding portion where the first electrode or the second electrode and the gold-coated bonding wire are bonded, wherein

the gold-coated bonding wire includes:

a core material containing silver or copper as a main component; and

a coating layer provided on a surface of the core material, the coating layer having a film thickness of 5 nm or more and 200 nm or less, the coating layer containing gold as a main component, and

the gold-coated bonding wire has a compressive stress of 290 MPa or more and 590 MPa or less when the gold-coated bonding wire is deformed by 60% with respect to a wire diameter.

14. The semiconductor device according to claim 13, further comprising:

a plurality of the semiconductor chips each including at least the single first electrode, wherein

the plurality of the semiconductor chips are stacked to make each of the first electrodes exposed, the semiconductor device further comprising:

two or more of the wedge bonding portions where the first electrodes of a plurality of the semiconductor chips are connected by the gold-coated bonding wire in sequence.

15. The semiconductor device according to claim 13 or claim 14, being for semiconductor memory.