

ABSTRACT

DECODED MATCH CIRCUIT FOR PERFORMANCE COUNTER

A match circuit (300) connected to a bus (104) carrying data is described. In one embodiment, the match circuit (300) includes logic (301j) for activating a decoded_match signal, the logic (301j) comprising logic (301k) for decoding a sum field comprising a selected portion of the data into a decoded_sum signal, wherein an active bit of the decoded_sum field corresponds to a value of the sum field; and logic (301l) for comparing the decoded_sum signal with a mask signal and outputting a binary bit comprising a decoded_match signal indicative of whether the decoded_sum signal and the mask signal match.

(FIG. 3)