SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREFOR

CROSS REFERENCE TO RELATED APPLICATION

This patent application claims the benefit of U.S. Patent Provisional Application 61/352,961, filed June 9, 2010 and Japanese Patent Application 2010-132488, filed June 9, 2010, the entire disclosures of which are incorporated herein.

FIELD

[0001] This application relates to a semiconductor device and a fabrication method therefor.

BACKGROUND

[0002] High integration of a semiconductor integrated circuit and an integrated circuit especially using an MOS transistor has been enhanced.
Miniaturization has been developed to a nano region of a Metal-Oxide-Semiconductor (MOS) transistor used in an integrated circuit with high integration of the semiconductor integrated circuit. When the miniaturization of the MOS transistor progressed, control of leakage current is difficult. Furthermore, there was a problem that it cannot make an occupation area of a circuit easily small in order to secure of needed amount of current value. In order to solve such a problem, it is proposed as Surrounding Gate Transistor (SGT) having a structure where a source, a gate, and a drain are disposed in a vertical direction for a substrate, and the gate surrounds a columnar semiconductor layer (for example, refer to Japanese Unexamined Patent Application H2-71556).

SUMMARY

[0003] In an MOS transistor, it is known that a compound layer formed of a compound of metal and silicon is provided on a highly doped silicon layer acting as a gate electrode, a source, and a drain. Lower-resistivity for the highly doped silicon layer can be achieved by forming a thick metal-silicon compound layer on the highly doped silicon layer. Also in SGT, the lower-resistivity for the highly doped silicon

layer acting as a gate electrode, a source, and a drain can achieved by forming the thick metal-silicon compound layer on the highly doped silicon layer acting as a gate electrode, a source, and a drain.

[0004] However, if the thick metal-silicon compound layer is formed on the highly doped silicon layer of the upper part of a columnar silicon layer, the metal-silicon compound layer may be formed in a spike shape. If the metal-silicon compound layer is formed in a spike shape, the spike-shaped metal-silicon compound layer reaches not only the highly doped silicon layer formed in the upper part of the columnar silicon layer but a channel region under this highly doped silicon layer. Accordingly, it becomes difficult for the SGT to operate as a transistor.

[0005] The above-mentioned phenomenon is avoidable by thickening the highly doped silicon layer formed in the upper part of the columnar silicon layer. That is, what is necessary is just to thickly form the highly doped silicon layer more than the metal-silicon compound layer formed in a spike shape. However, since the electrical resistance of the highly doped silicon layer is proportional to the length, the electrical resistance of the highly doped silicon layer will increase if the highly doped silicon layer formed in the columnar silicon layer upper part is thickened. Therefore, it becomes difficult to achieve the low-resistivity for the highly doped silicon layer.

[0006] Moreover, there is a phenomenon that the thickness of the formed metal-silicon compound layer becomes thick as the diameter of the columnar silicon layer becomes small in the case that the metal-silicon compound layer is formed on the highly doped silicon layer of the upper part of the columnar silicon layer. If the diameter of the columnar silicon layer becomes small and the thickness of the metal-silicon compound layer formed on the columnar silicon layer becomes thick, the metal-silicon compound layer will come to be formed in the joint part between the highly doped silicon layer and channel region which are formed in the upper part of the columnar silicon layer. This causes leakage current.

[0007] The above-mentioned phenomenon is avoidable by thickening the highly doped silicon layer formed on the upper part of the columnar silicon layer. That is,

what is necessary is just to form the highly doped silicon layer more thickly than the metal-silicon compound layer formed which becomes thick as the diameter of the columnar silicon layer becomes small. However, since the electrical resistance of the highly doped silicon layer is proportional to the length as above-mentioned, if the highly doped silicon layer formed in the upper part of the columnar silicon layer is thickened, the electrical resistance of the highly doped silicon layer increases and then it is difficult to achieve the low-resistivity.

[0008] Usually, in a MOS transistor, the metal-silicon compound layer formed on the highly doped silicon layer acting as a gate electrode, a source, and a drain is formed in the same processing step. Also in an SGT, the metal-silicon compound layer formed on the highly doped silicon layer acting as a gate electrode, a source, and a drain is formed in the same processing step as well as the MOS transistor. Therefore, in the SGT, when forming a thick metal-silicon compound layer in either of the highly doped silicon layers acting as a gate electrode, source, and drain, a metal-silicon compound layer will be formed in all the highly doped silicon layers acting as a gate electrode, source, and drain. As above-mentioned, when the metal-silicon compound layer is formed on the columnar semiconductor layer, the metal-silicon compound layer is formed in a spike shape. Therefore, the highly doped silicon layer formed in the upper part of the columnar silicon layer must be formed thickly so as to avoid that this spike shape metal-silicon compound layer reaches channel regions. As a result, the electrical resistance of this highly doped silicon layer will increase.

[0009] In the gate electrode of SGT, the same material as the material which forms the gate electrode often performs gate wiring. Therefore, the low-resistivity for the gate electrode and gate wiring is achieved by forming the metal-silicon compound layer thickly at the gate electrode and gate wiring. Accordingly, the high-speed operation of SGT becomes enabling. Also, in the SGT, it often wires using a planar silicon layer disposed under the columnar silicon layer. Therefore, the low-resistivity for this planar silicon layer is achieved by forming the metal-silicon compound layer thickly into the same layer as the planar silicon layer, thereby enabling the high-speed

operation of SGT. On the other hand, since the highly doped silicon layer of the upper part of the columnar silicon layer of SGT connects to electric contact directly, it is difficult to wire with this highly doped silicon layer of the upper part of the columnar silicon layer. Therefore, the metal-silicon compound layer is formed between the electric contact and the highly doped silicon layer. Since current flows into the thickness direction of this metal-silicon compound layer, the low-resistivity for the highly doped silicon layer of the upper part of the columnar silicon layer is achieved corresponding to the thickness of the metal-silicon compound layer. As mentioned above, in order to thickly form the metal-silicon compound layer at the upper part of the columnar silicon layer, there is no other way but to thickly form the highly doped silicon layer formed in the upper part of the columnar silicon layer. However, since the electrical resistance of the highly doped silicon layer is proportional to the length, the electrical resistance of the highly doped silicon layer will increase if the highly doped silicon layer is thickly formed. As a result, it is difficult to achieve the low-resistivity for the highly doped silicon layer lower. Also, parasitic capacitance occurred between multilayer interconnections with the miniaturization of SGT as well as the MOS transistor, thereby there was also a problem that the operating speed of transistor is dropped.

[0010] This application is made in view of the above-mentioned situation, and the object is to provide a semiconductor device having satisfactory characteristics and having achieved miniaturization and, a fabrication method for such semiconductor device.

[0011] In order to achieve the above object, a semiconductor device according to a first aspect of the present invention comprises:

a first planar semiconductor layer;

a first columnar semiconductor layer formed on the first planar semiconductor layer;

a first highly doped semiconductor layer formed in a lower region of the first columnar semiconductor layer and the first planar semiconductor layer;

a second highly doped semiconductor layer formed in an upper region of the first columnar semiconductor layer and having a conductivity type same as a conductivity type of the first highly doped semiconductor layer;

a first gate insulating film formed so as to surround the first columnar semiconductor layer on a sidewall of the first columnar semiconductor layer between the first highly doped semiconductor layer and the second highly doped semiconductor layer;

a first gate electrode formed so as to surround the first gate insulating film on the first gate insulating film;

a first insulating film formed between the first gate electrode and the first planar semiconductor layer;

a first insulating film sidewall formed so as to contact a top surface of the first gate electrode and an upper sidewall of the first columnar semiconductor layer, and to surround the upper region of the first columnar semiconductor layer;

a second metal-semiconductor compound layer formed in the same layer as the first planar semiconductor layer so as to contact the first highly doped semiconductor layer; and

a first electric contact formed on the second highly doped semiconductor layer, wherein

the first electric contact and the second highly doped semiconductor layer are connected directly and

the first gate electrode includes a first metal-semiconductor compound layer.

[0012] Preferably, further comprising a fifth metal-semiconductor compound layer formed between the first electric contact and the second highly doped semiconductor layer, wherein

the metal of the fifth metal-semiconductor compound is a different type of metal than the metal of the first metal-semiconductor compound layer and the metal of the second metal-semiconductor compound layer.

[0013] Preferably, the first gate electrode further comprises a first metal film

formed between the first gate insulating film and the first metal-semiconductor compound layer.

[0014] In order to achieve the above object, a semiconductor device according to a second aspect of the present invention comprises a first transistor and a second transistor,

the first transistor comprising:

a first planar semiconductor layer;

a first columnar semiconductor layer formed on the first planar semiconductor layer;

a first highly doped semiconductor layer of a second-conductivity type formed in the lower region of the first columnar semiconductor layer and the first planar semiconductor layer;

a second highly doped semiconductor layer of the second-conductivity type formed in the upper region of the 1st columnar semiconductor layer;

a first gate insulating film formed so as to surround the first columnar semiconductor layer on a sidewall of the first columnar semiconductor layer between the first highly doped semiconductor layer and the second highly doped semiconductor layer;

a first gate electrode formed so as to surround the first gate insulating film on the first gate insulating film;

a first insulating film formed between the first gate electrode and the first planar semiconductor layer;

a first insulating film sidewall formed so as to contact to a top surface of the first gate electrode and an upper sidewall of the first columnar semiconductor layer and to surround the upper region of the first columnar semiconductor layer;

a second metal-semiconductor compound layer formed in the same layer as the first planar semiconductor layer so as to contact to the first highly doped semiconductor layer; and

a first electric contact formed on the second highly doped semiconductor layer,

and

the second transistor comprising:

a second planar semiconductor layer;

a second columnar semiconductor layer formed on the second planar semiconductor layer;

a third highly doped semiconductor layer of a first conductivity type formed in a lower region of the second columnar semiconductor layer and the second planar semiconductor layer;

a fourth highly doped semiconductor layer of the first conductivity type formed in an upper region of the second columnar semiconductor layer;

a second gate insulating film formed so as to surround the second columnar semiconductor layer on a sidewall of the second columnar semiconductor layer between the third highly doped semiconductor layer and the fourth highly doped semiconductor layer;

a second gate electrode formed so as to surround the second gate insulating film on the second gate insulating film;

a second insulating film formed between the second gate electrode and the second planar semiconductor layer;

a second insulating film sidewall formed so as to contact to a top surface of the second gate electrode and an upper sidewall of the second columnar semiconductor layer, and to surround the upper region of the second columnar semiconductor layer;

a fourth metal-semiconductor compound layer formed in the same layer as the second planar semiconductor layer so as to contact the third highly doped semiconductor layer; and

a second electric contact formed on the fourth highly doped semiconductor layer, wherein

the first electric contact and the second highly doped semiconductor layer are connected directly,

the second electric contact and the fourth highly doped semiconductor layer

are connected directly,

the first gate electrode includes a first metal-semiconductor compound layer, and

the second gate electrode includes a third metal-semiconductor compound layer.

[0015] Preferably, further comprising

a fifth metal-semiconductor compound layer formed between the first electric contact and the second highly doped semiconductor layer;

a sixth metal-semiconductor compound layer formed between the second electric contact and the fourth highly doped semiconductor layer, wherein

the metal of the fifth metal-semiconductor compound is a different type of metal than the metal of the first metal-semiconductor compound and the metal of the second metal-semiconductor compound, and

the metal of the sixth metal-semiconductor compound is a different type of metal than the metal of the third metal-semiconductor compound and the metal of the fourth metal-semiconductor compound.

[0016] Preferably, further comprising

a first metal film formed between the first gate insulating film and the first metal-semiconductor compound layer; and

a second metal film formed between the second gate insulating film and the third metal-semiconductor compound layer.

[0017] Preferably, the first gate insulating film and the first metal film are formed from materials for configuring the first transistor to be an enhancement type, and

the second gate insulating film and the second metal film are formed from materials for configuring the second transistor to be an enhancement type.

[0018] In order to achieve the above object, a fabrication method for a semiconductor device according to a third aspect of the present invention being a method for fabricating the semiconductor device mentioned above, the fabrication method of aforesaid semiconductor device comprises the step of:

preparing a structure including: the first planar semiconductor layer; the first columnar semiconductor layer formed on the first planar semiconductor layer, a hard mask being formed in a top surface of the first columnar semiconductor layer; the first highly doped semiconductor layer formed in a lower region of the first planar semiconductor layer and the first columnar semiconductor layer; and a third insulating film formed on the hard mask and the first planar semiconductor layer;

forming a fourth insulating film, a third metal film, and a first semiconductor layer in this sequence on the structure;

etching the first semiconductor film to remain the first semiconductor film in a shape of a sidewall on a sidewall of the first columnar semiconductor layer;

etching the third metal film to remain the sidewall of the first columnar semiconductor layer in a shape of the sidewall;

etching the fourth insulating film to remain the sidewall of the first columnar semiconductor layer in a shape of the sidewall;

forming a second semiconductor layer on results of the step of etching the fourth insulating film;

forming a third semiconductor layer so that results of the step of forming the second semiconductor layer are embedded,

planarizing the second semiconductor layer, the third semiconductor layer and the first semiconductor layer and etching back so that an upper region of the third metal film is exposed;

etching the third metal film made remaining in the shape of the sidewall and the fourth insulating film made remaining in the shape of the sidewall so as to expose an upper sidewall of the first columnar semiconductor layer, and then forming the first metal film and the first gate insulating film;

forming a second highly doped semiconductor layer having a conductivity type same as the first highly doped semiconductor layer in the upper region of the first columnar semiconductor layer;

forming an oxide film and a nitride film sequentially on results of the step of

forming the second highly doped semiconductor layer;

etching the oxide film and the nitride film so that the oxide film and the nitride film remain in a shape of the sidewall on the upper sidewall of the first columnar semiconductor layer and the sidewall of the hard mask, and then forming the first insulating film sidewall;

etching the first semiconductor layer, the second semiconductor layer and the third semiconductor layer to remain at least a part of the first semiconductor layer and the second semiconductor layer so as to surround the first metal film on the first metal film sidewall;

etching to remove the third insulating film exposed in the step of etching the semiconductor layer and exposing the first planar semiconductor layer;

by depositing and then annealing a metal on results of the step of exposing the first planar semiconductor layer, making react the deposited metal with a semiconductor included in the first planar semiconductor layer, and making react the deposited metal with a semiconductor included in the first semiconductor layer and the second semiconductor layer made to remain on the first metal film; and

by removing an unreacted metal in the step of making react the metal and the semiconductor, forming the second metal-semiconductor compound layer in the first planar semiconductor layer, and forming the first metal-semiconductor compound layer in the first gate electrode.

[0019] Preferably, further comprising the step of directly forming the first electric contact on the second highly doped semiconductor layer formed in the upper part of the first columnar semiconductor layer.

[0020] According to the present invention, the semiconductor device and the fabrication method for such semiconductor device having satisfactory characteristics and achieving the miniaturization can be provided.

BRIEF DESCRIPTION OF THE DRAWINGS

[0021]

[FIG. 1] FIG. 1A is a top view of a semiconductor device according to a first

embodiment of the present invention, and FIG. 1B is a cross-sectional diagram taken in the line **X-X'** of FIG. 1A.

[**FIG. 2**] FIG. 2A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 1A, and FIG. 2B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 1A.

[**FIG. 3**] FIG. 3A is a top view for explaining a fabrication method of the semiconductor device according to the first embodiment, and FIG. 3B is a cross-sectional diagram taken in the line **X-X'** of FIG. 3A.

[**FIG. 4**] FIG. 4A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 3A, and FIG. 4B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 3A.

[**FIG. 5**] FIG. 5A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 5B is a cross-sectional diagram taken in the line **X-X'** of FIG. 5A.

[**FIG. 6**] FIG. 6A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 5A, and FIG. 6B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 5A.

[**FIG. 7**] FIG. 7A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 7B is a cross-sectional diagram taken in the line **X-X'** of FIG. 7A.

[**FIG. 8**] FIG. 8A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 7A, and FIG. 8B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 7A.

[**FIG. 9**] FIG. 9A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 9B is a cross-sectional diagram taken in the line **X-X'** of FIG. 9A.

[**FIG. 10**] FIG. 10A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 9A, and FIG. 10B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 9A.

[**FIG. 11**] FIG. 11A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 11B is a cross-sectional diagram taken in the line **X-X'** of FIG. 11A.

[**FIG. 12**] FIG. 12A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 11A, and FIG. 12B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 11A.

[**FIG. 13**] FIG. 13A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 13B is a cross-sectional diagram taken in the line **X-X'** of FIG. 13A.

[**FIG. 14**] FIG. 14A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 13A, and FIG. 14B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 13A.

[**FIG. 15**] FIG. 15A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 15B is a cross-sectional diagram taken in the line **X-X'** of FIG. 15A.

[**FIG. 16**] FIG. 16A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 15A, and FIG. 16B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 15A.

[**FIG. 17**] FIG. 17A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 17B is a cross-sectional diagram taken in the line **X-X'** of FIG. 17A.

[**FIG. 18**] FIG. 18A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 17A, and FIG. 18B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 17A.

[**FIG. 19**] FIG. 19A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 19B is a cross-sectional diagram taken in the line **X-X'** of FIG. 19A.

[**FIG. 20**] FIG. 20A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 19A, and FIG. 20B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 19A.

[**FIG. 21**] FIG. 21A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 21B is a cross-sectional diagram taken in the line **X-X'** of FIG. 21A.

[**FIG. 22**] FIG. 22A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 21A, and FIG. 22B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 21A.

[**FIG. 23**] FIG. 23A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 23B is a cross-sectional diagram taken in the line **X-X'** of FIG. 23A.

[**FIG. 24**] FIG. 24A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG.

23A, and FIG. 24B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 23A.

[**FIG. 25**] FIG. 25A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 25B is a cross-sectional diagram taken in the line **X-X'** of FIG. 25A.

[**FIG. 26**] FIG. 26A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 25A, and FIG. 26B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 25A.

[**FIG. 27**] FIG. 27A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 27B is a cross-sectional diagram taken in the line **X-X'** of FIG. 27A.

[**FIG. 28**] FIG. 28A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 27A, and FIG. 28B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 27A.

[**FIG. 29**] FIG. 29A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 29B is a cross-sectional diagram taken in the line **X-X'** of FIG. 29A.

[**FIG. 30**] FIG. 30A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 29A, and FIG. 30B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 29A.

[**FIG. 31**] FIG. 31A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 31B is a cross-sectional diagram taken in the line **X-X'** of FIG. 31A.

[**FIG. 32**] FIG. 32A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 31A, and FIG. 32B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 31A.

[**FIG. 33**] FIG. 33A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 33B is a cross-sectional diagram taken in the line **X-X'** of FIG. 33A.

[**FIG. 34**] FIG. 34A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 33A, and FIG. 34B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 33A.

[**FIG. 35**] FIG. 35A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 35B is a cross-sectional diagram taken in the line **X-X'** of FIG. 35A.

[**FIG. 36**] FIG. 36A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 35A, and FIG. 36B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 35A.

[**FIG. 37**] FIG. 37A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 37B is a cross-sectional diagram taken in the line **X-X'** of FIG. 37A.

[**FIG. 38**] FIG. 38A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 37A, and FIG. 38B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 37A.

[**FIG. 39**] FIG. 39A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 39B is a cross-sectional diagram taken in the line **X-X'** of FIG. 39A.

[**FIG. 40**] FIG. 40A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 39A, and FIG. 40B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 39A.

[**FIG. 41**] FIG. 41A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 41B is a cross-sectional diagram taken in the line **X-X'** of FIG. 41A.

[**FIG. 42**] FIG. 42A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 41A, and FIG. 42B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 41A.

[**FIG. 43**] FIG. 43A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 43B is a cross-sectional diagram taken in the line **X-X'** of FIG. 43A.

[**FIG. 44**] FIG. 44A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 43A, and FIG. 44B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 43A.

[**FIG. 45**] FIG. 45A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 45B is a cross-sectional diagram taken in the line **X-X'** of FIG. 45A.

[**FIG. 46**] FIG. 46A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 45A, and FIG. 46B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 45A.

[**FIG. 47**] FIG. 47A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 47B is a

cross-sectional diagram taken in the line **X-X'** of FIG. 47A.

[**FIG. 48**] FIG. 48A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 47A, and FIG. 48B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 47A.

[**FIG. 49**] FIG. 49A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 49B is a cross-sectional diagram taken in the line **X-X'** of FIG. 49A.

[**FIG. 50**] FIG. 50A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 49A, and FIG. 50B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 49A.

[**FIG. 51**] FIG. 51A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 51B is a cross-sectional diagram taken in the line **X-X'** of FIG. 51A.

[**FIG. 52**] FIG. 52A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 51A, and FIG. 52B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 51A.

[**FIG. 53**] FIG. 53A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 53B is a cross-sectional diagram taken in the line **X-X'** of FIG. 53A.

[**FIG. 54**] FIG. 54A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 53A, and FIG. 54B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 53A.

[**FIG. 55**] FIG. 55A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 55B is a cross-sectional diagram taken in the line **X-X'** of FIG. 55A.

[**FIG. 56**] FIG. 56A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 55A, and FIG. 56B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 55A.

[**FIG. 57**] FIG. 57A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 57B is a cross-sectional diagram taken in the line **X-X'** of FIG. 57A.

[**FIG. 58**] FIG. 58A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 57A, and FIG. 58B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 57A.

[**FIG. 59**] FIG. 59A is a top view for explaining the fabrication method of the

semiconductor device according to the first embodiment, and FIG. 59B is a cross-sectional diagram taken in the line **X-X'** of FIG. 59A.

[**FIG. 60**] FIG. 60A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 59A, and FIG. 60B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 59A.

[**FIG. 61**] FIG. 61A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 61B is a cross-sectional diagram taken in the line **X-X'** of FIG. 61A.

[**FIG. 62**] FIG. 62A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 61A, and FIG. 62B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 61A.

[**FIG. 63**] FIG. 63A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 63B is a cross-sectional diagram taken in the line **X-X'** of FIG. 63A.

[**FIG. 64**] FIG. 64A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 63A, and FIG. 64B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 63A.

[**FIG. 65**] FIG. 65A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 65B is a cross-sectional diagram taken in the line **X-X'** of FIG. 65A.

[**FIG. 66**] FIG. 66A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 65A, and FIG. 66B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 65A.

[**FIG. 67**] FIG. 67A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 67B is a cross-sectional diagram taken in the line **X-X'** of FIG. 67A.

[**FIG. 68**] FIG. 68A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 67A, and FIG. 68B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 67A.

[**FIG. 69**] FIG. 69A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 69B is a cross-sectional diagram taken in the line **X-X'** of FIG. 69A.

[**FIG. 70**] FIG. 70A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 69A, and FIG. 70B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 69A.

[**FIG. 71**] FIG. 71A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 71B is a cross-sectional diagram taken in the line **X-X'** of FIG. 71A.

[**FIG. 72**] FIG. 72A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 71A, and FIG. 72B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 71A.

[**FIG. 73**] FIG. 73A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 73B is a cross-sectional diagram taken in the line **X-X'** of FIG. 73A.

[**FIG. 74**] FIG. 74A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 73A, and FIG. 74B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 73A.

[**FIG. 75**] FIG. 75A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 75B is a cross-sectional diagram taken in the line **X-X'** of FIG. 75A.

[**FIG. 76**] FIG. 76A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 75A, and FIG. 76B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 75A.

[**FIG. 77**] FIG. 77A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 77B is a cross-sectional diagram taken in the line **X-X'** of FIG. 77A.

[**FIG. 78**] FIG. 78A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 77A, and FIG. 78B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 77A.

[**FIG. 79**] FIG. 79A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 79B is a cross-sectional diagram taken in the line **X-X'** of FIG. 79A.

[**FIG. 80**] FIG. 80A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 79A, and FIG. 80B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 79A.

[**FIG. 81**] FIG. 81A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 81B is a cross-sectional diagram taken in the line **X-X'** of FIG. 81A.

[**FIG. 82**] FIG. 82A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG.

81A, and FIG. 82B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 81A.

[FIG. 83] FIG. 83A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 83B is a cross-sectional diagram taken in the line **X-X'** of FIG. 83A.

[FIG. 84] FIG. 84A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 83A, and FIG. 84B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 83A.

[FIG. 85] FIG. 85A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 85B is a cross-sectional diagram taken in the line **X-X'** of FIG. 85A.

[FIG. 86] FIG. 86A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 85A, and FIG. 86B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 85A.

[FIG. 87] FIG. 87A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 87B is a cross-sectional diagram taken in the line **X-X'** of FIG. 87A.

[FIG. 88] FIG. 88A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 87A, and FIG. 88B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 87A.

[FIG. 89] FIG. 89A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 89B is a cross-sectional diagram taken in the line **X-X'** of FIG. 89A.

[FIG. 90] FIG. 90A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 89A, and FIG. 90B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 89A.

[FIG. 91] FIG. 91A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 91B is a cross-sectional diagram taken in the line **X-X'** of FIG. 91A.

[FIG. 92] FIG. 92A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 91A, and FIG. 92B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 91A.

[FIG. 93] FIG. 93A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG.93B is a cross-sectional diagram taken in the line **X-X'** of FIG. 93A.

[**FIG. 94**] FIG. 94A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 93A, and FIG. 94B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 93A.

[**FIG. 95**] FIG. 95A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 95B is a cross-sectional diagram taken in the line **X-X'** of FIG. 95A.

[**FIG. 96**] FIG. 96A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 95A, and FIG. 96B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 95A.

[**FIG. 97**] FIG. 97A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 97B is a cross-sectional diagram taken in the line **X-X'** of FIG. 97A.

[**FIG. 98**] FIG. 98A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 97A, and FIG. 98B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 97A.

[**FIG. 99**] FIG. 99A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 99B is a cross-sectional diagram taken in the line **X-X'** of FIG. 99A.

[**FIG. 100**] FIG. 100A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 99A, and FIG. 100B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 99A.

[**FIG. 101**] FIG. 101A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 101B is a cross-sectional diagram taken in the line **X-X'** of FIG. 101A.

[**FIG. 102**] FIG. 102A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 101A, and FIG. 102B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 101A.

[**FIG. 103**] FIG. 103A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 103B is a cross-sectional diagram taken in the line **X-X'** of FIG. 103A.

[**FIG. 104**] FIG. 104A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 103A, and FIG. 104B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG.

103A.

[**FIG. 105**] FIG. 105A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 105B is a cross-sectional diagram taken in the line **X-X'** of FIG. 105A.

[**FIG. 106**] FIG. 106A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 105A, and FIG. 106B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 106A.

[**FIG. 107**] FIG. 107A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 107B is a cross-sectional diagram taken in the line **X-X'** of FIG. 107A.

[**FIG. 108**] FIG. 108A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 107A, and FIG. 108B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 107A.

[**FIG. 109**] FIG. 109A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 109B is a cross-sectional diagram taken in the line **X-X'** of FIG. 109A.

[**FIG. 110**] FIG. 110A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 109A, and FIG. 110B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 109A.

[**FIG. 111**] FIG. 111A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 111B is a cross-sectional diagram taken in the line **X-X'** of FIG. 11A.

[**FIG. 112**] FIG. 112A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 111A, and FIG. 112B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 111A.

[**FIG. 113**] FIG. 113A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 113B is a cross-sectional diagram taken in the line **X-X'** of FIG. 113A.

[**FIG. 114**] FIG. 114A is a cross-sectional diagram taken in the line **Y1-Y1'** of

FIG. 113A, and FIG. 114B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 113A.

[**FIG. 115**] FIG. 115A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 115B is a cross-sectional diagram taken in the line **X-X'** of FIG. 115A.

[**FIG. 116**] FIG. 116A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 115A, and FIG. 116B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 115A.

[**FIG. 117**] FIG. 117A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 117B is a cross-sectional diagram taken in the line **X-X'** of FIG. 117A.

[**FIG. 118**] FIG. 118A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 117A, and FIG. 118B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 117A.

[**FIG. 119**] FIG. 119A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 119B is a cross-sectional diagram taken in the line **X-X'** of FIG. 119A.

[**FIG. 120**] FIG. 120A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 119A, and FIG. 120B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 119A.

[**FIG. 121**] FIG. 121A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 121B is a cross-sectional diagram taken in the line **X-X'** of FIG. 121A.

[**FIG. 122**] FIG. 122A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 121A, and FIG. 122B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 121A.

[**FIG. 123**] FIG. 123A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 123B is a cross-sectional diagram taken in the line **X-X'** of FIG. 123A.

[**FIG. 124**] FIG. 124A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 123A, and FIG. 124B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 123A.

[**FIG. 125**] FIG. 125A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 125B is a cross-sectional diagram taken in the line **X-X'** of FIG. 125A.

[**FIG. 126**] FIG. 126A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 125A, and FIG. 126B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 125A.

[**FIG. 127**] FIG. 127A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 127B is a cross-sectional diagram taken in the line **X-X'** of FIG. 127A.

[**FIG. 128**] FIG. 128A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 127A, and FIG. 128B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 127A.

[**FIG. 129**] FIG. 129A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 129B is a cross-sectional diagram taken in the line **X-X'** of FIG. 129A.

[**FIG. 130**] FIG. 130A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 129A, and FIG. 130B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 129A.

[**FIG. 131**] FIG. 131A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 131B is a cross-sectional diagram taken in the line **X-X'** of FIG. 131A.

[**FIG. 132**] FIG. 132A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 131A, and FIG. 132B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 131A.

[**FIG. 133**] FIG. 133A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 133B is a

cross-sectional diagram taken in the line **X-X'** of FIG. 133A.

[**FIG. 134**] FIG. 134A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 133A, and FIG. 134B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 133A.

[**FIG. 135**] FIG. 135A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 135B is a cross-sectional diagram taken in the line **X-X'** of FIG. 135A.

[**FIG. 136**] FIG. 136A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 135A, and FIG. 136B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 135A.

[**FIG. 137**] FIG. 137A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 137B is a cross-sectional diagram taken in the line **X-X'** of FIG. 137A.

[**FIG. 138**] FIG. 138A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 137A, and FIG. 138B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 137A.

[**FIG. 139**] FIG. 139A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 139B is a cross-sectional diagram taken in the line **X-X'** of FIG. 139A.

[**FIG. 140**] FIG. 140A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 139A, and FIG. 140B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 139A.

[**FIG. 141**] FIG. 141A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 141B is a cross-sectional diagram taken in the line **X-X'** of FIG. 141A.

[**FIG. 142**] FIG. 142A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 141A, and FIG. 142B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 141A.

[**FIG. 143**] FIG. 143A is a top view for explaining the fabrication method of the

semiconductor device according to the first embodiment, and FIG. 143B is a cross-sectional diagram taken in the line **X-X'** of FIG. 143A.

[**FIG. 144**] FIG. 144A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 143A, and FIG. 144B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 143A.

[**FIG. 145**] FIG. 145A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 145B is a cross-sectional diagram taken in the line **X-X'** of FIG. 49A.

[**FIG. 146**] FIG. 146A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 145A, and FIG. 146B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 145A.

[**FIG. 147**] FIG. 147A is a top view for explaining the fabrication method of the semiconductor device according to the first embodiment, and FIG. 147B is a cross-sectional diagram taken in the line **X-X'** of FIG. 147A.

[**FIG. 148**] FIG. 148A is a cross-sectional diagram taken in the line **Y1-Y1'** of FIG. 147A, and FIG. 148B is a cross-sectional diagram taken in the line **Y2-Y2'** of FIG. 147A.

DETAILED DESCRIPTION

[**0022**] (First Embodiment)

FIG. 1A is a top view showing an inverter including Negative Channel Metal-Oxide-Semiconductor (NMOS)-SGT and Positive Channel Metal-Oxide-Semiconductor (PMOS)-SGT according to a first embodiment of the present invention, and FIG. 1B is a cross-sectional diagram taken in the cutting line **X-X'** of FIG. 1A. FIG. 2A is a cross-sectional diagram taken in the cutting line **Y1-Y1'** of FIG. 1A. FIG. 2B is a cross-sectional diagram taken in the cutting line **Y2-Y2'** of FIG. 1A. Although FIG. 1A is a top view, hatching is attached in part in order to distinguish an area.

With reference to FIG. 1A to FIG. 2B, the inverter including the NMOS-SGT and PMOS-SGT according to the first embodiment will be explained hereinafter.

[0023] First of all, the NMOS-SGT of the first embodiment will be explained.

A first planar silicon layer **212** is formed on a silicon dioxide film **101**, and a first columnar silicon layer **208** is formed on the first planar silicon layer 212.

A first n+ type silicon layer **113** is formed in a lower region of the first columnar silicon layer **208** and a region of the first planar silicon layer **212** located under the first columnar silicon layer **208**, and a second n+ type silicon layer **144** is formed in an upper region of the first columnar silicon layer **208**. In this embodiment, the first n+ type silicon layer **113** functions as a source diffusion layer, and the second n+ type silicon layer **144** functions as a drain diffused layer. Moreover, a part between the source diffusion layer and the drain diffused layer functions as a channel region. The region of the first columnar silicon layer **208** between the first n+ type silicon layer **113** and the second n+ type silicon layer **144** which function as this channel region is a first silicon layer **114**.

[0024] A first gate insulating film **140** is formed in the side surface of the first columnar silicon layer **208** so that the channel region may be surrounded. That is, the first gate insulating film **140** is formed so that the first silicon layer **114** is surrounded. The first gate insulating film **140** is composed of an oxide film, a nitride film, or a high dielectric film, for example. Furthermore, a first metal film **138** is formed on the first gate insulating film **140**, and a first metal-silicon compound layer **159a** (hereinafter, referred to as first compound layer) is formed in the sidewall of the first metal film **138**. The first metal film **138** is a film including titanium nitride or tantalum nitride, for example. Also, the first metal-silicon compound layer **159a** is formed of the compound of metal and silicon, and this metal is Ni, Co, or the like.

The first metal film **138** and first metal-silicon compound layer **159a** compose a first gate electrode **210**.

In this embodiment, a channel is formed in the first silicon layer **114** by applying voltage to the first gate electrode **210** at the time of operation.

[0025] A first insulating film **129a** is formed between the first gate electrode **210** and the first planar silicon layer **212**. Furthermore, a first insulating film sidewall **223**

is formed in the upper sidewall of the first columnar silicon layer **208** so that the upper region of the first columnar silicon layer **208** is surrounded, and the first insulating film sidewall **223** contacts with the top surface of the first gate electrode **210**. Also, the first insulating film sidewall **223** is composed of a nitride film **150** and an oxide film **152**.

Furthermore, a second metal-silicon compound layer **160** is formed in the first planar silicon layer **212**.

The second metal-silicon compound layer **160** is formed of the compound of metal and silicon, and this metal is Ni, Co or the like.

The second metal-silicon compound layer **160** is formed to contact with the first n+ type silicon layer **113**, and functions as a wiring layer for providing power supply potential to the first n+ type silicon layer **113**.

[**0026**] An electric contact **216** is formed on the first columnar silicon layer **208**. In addition, the electric contact **216** is composed of a barrier metal layer **182** and metal layers **183** and **184**. The electric contact **216** is directly formed on the second n+ type silicon layer **144**. Accordingly, the electric contact **216** and the second n+ type silicon layer **144** are connected directly. In this embodiment, the electric contact **216** is contacted with the second n+ type silicon layer **144**.

The barrier metal layer **182** is formed of metal, such as titanium or tantalum. The second n+ type silicon layer **144** is connected to an output wiring **220** via the electric contact **216**. The output wiring **220** is composed of a barrier metal layer **198**, a metal layer **199**, and a barrier metal layer **200**.

[**0027**] A seventh metal-silicon compound layer **159c** is formed in a part of the side surface of the first metal-silicon compound layer **159a**. In addition, a material which composes the seventh metal-silicon compound layer **159c** is the same material as the first metal-silicon compound layer **159a**. The seventh metal-silicon compound layer **159c** functions as a gate wiring **218**. An electric contact **215** is formed on the seventh metal-silicon compound layer **159c**. The electric contact **215** is composed of a barrier metal layer **179** and metal layers **180** and **181**. Furthermore, the electric contact **215** is

connected to an input wiring **221** composed of a barrier metal layer **201**, a metal layer **202**, and a barrier metal layer **203**. At the time of operation, input voltage is provided to the first gate electrode **210** via the electric contact **215** so that a channel is formed in the first silicon layer **114**.

[0028] Also, an electric contact **217** is formed on the second metal-silicon compound layer **160**. The electric contact **217** is composed of a barrier metal layer **185** and metal layer **186** and **187**, and is connected to a power source wiring **222**. The power source wiring **222** is composed of a barrier metal layer **204**, a metal layer **205**, and a barrier metal layer **206**. Power supply potential is provided to both of the first n+ type silicon layer **113** and second metal-silicon compound layer **160** via the electric contact **217** at the time of operation.

The NMOS-SGT is formed according to such a configuration.

[0029] As mentioned above, in the NMOS-SGT according to this embodiment, the thick first, seventh and second metal-silicon compound layers **159a**, **159c**, and **160** are formed in the gate electrode **210**, the gate wiring **218** and planar silicon layer **212**. By such a structure of the SGT, the low-resistivity for the gate electrode **210** and planar silicon layer **212** is achieved, thereby enabling high-speed operation.

[0030] Furthermore, in the NMOS-SGT according to this embodiment, the electric contact **216** is directly disposed on the second n+ type silicon layer 144 comprising the highly doped silicon layer of the upper part of the columnar silicon layer **208**. That is, since the metal-silicon compound layer is not formed between the electric contact **216** and the second n+ type silicon layer **144**, the spike-shaped metal-silicon compound layer which may cause occurrence of leakage current is not formed. Even if the diameter of the columnar silicon layer is formed small for the purpose of high integration of the semiconductor device, the phenomenon in which the metal-silicon compound layer formed on the columnar silicon layer becomes still thicker is not occurred, either. Therefore, the above leakage current is not occurred. Also, since it is not necessary to thickly form the second n+ type silicon layer **144** comprising the highly doped silicon layer in order to suppress the occurrence of this leakage current,

increase of the electrical resistance by the second n+ type silicon layer **144** is also avoidable.

According to the configuration mentioned above, the low-resistivity and the miniaturization for the semiconductor device are achievable.

Also, the parasitic capacitance between the gate electrode **210** and the planar silicon layer **212** can be reduced with the first insulating film 129a. Accordingly, the reduction of operating speed with the miniaturization of SGT is avoidable.

[0031] Next, PMOS-SGT according to this embodiment will be explained. A second planar silicon layer **211** is formed on a silicon dioxide film **101**, and a second columnar silicon layer **207** is formed on the second planar silicon layer **211**, as well as the NMOS-SGT mentioned above.

A first p+ type silicon layer **119** is formed in a lower region of the second columnar silicon layer **207** and a region of the second planar silicon layer 211 located under the second columnar silicon layer **207**, and a second p+ type silicon layer **146** is formed in an upper region of the second columnar silicon layer 207. In this embodiment, the first p+ type silicon layer **119** functions as a source diffusion layer, and the second p+ type silicon layer **146** functions as a drain diffused layer. Also, a part between the source region and a drain region functions as a channel region. The region of the second columnar silicon layer **207** between the first p+ type silicon layer **119** and the second p+ type silicon layer **146** which function as this channel region is a second silicon layer **120**.

[0032] A second gate insulating film **139** is formed in the side surface of the second columnar silicon layer **207** so that the channel region is surrounded. That is, the second gate insulating film **139** is formed in the side surface of the second silicon layer **120** so that the second silicon layer 114 is surrounded. The second gate insulating film **139** is composed of an oxide film, a nitride film, or a high dielectric film, for example. Also, a second metal film **137** is formed in the perimeter of the second gate insulating film **139**. The second metal film **137** is a film including titanium nitride or tantalum nitride, for example. Also, a third metal-silicon compound layer

159b is formed in the perimeter of the second metal film **137**. A material which composes the third metal-silicon compound layer 159b is the same material as that of the first metal-silicon compound layer 159a and that of the seventh metal-silicon layer 159c. The second gate electrode **209** is composed of the second metal film **137** and the third metal-silicon compound layer **159b**. A seventh metal-silicon compound layer **159c** formed between the first gate electrode **210** and the second gate electrode **209** functions as a gate wiring **218**, and provides input potential to the second and first gate electrodes **209** and **210** at the time of operation.

In this embodiment, a channel is formed in a region of the second silicon layer **120** by applying voltage to the second gate electrode **209**.

[**0033**] A second insulating film **129b** is formed between the second gate electrode **209** and the second planar silicon layer **211**. Furthermore, a second insulating film sidewall **224** is formed in the upper sidewall of the second columnar silicon layer **207**, and the second insulating film sidewall **224** contacts with the top surface of the second gate electrode **209**. The second insulating film sidewall **224** is composed of an oxide film **151** and a nitride film **149**.

Also, a fourth metal-silicon compound layer **158** is formed in the second planar silicon layer **211** so as to contact with the first p+ type silicon layer **119**. The fourth metal-silicon compound layer **158** is formed of the compound of metal and silicon, and this metal is Ni, Co or the like.

[**0034**] An electric contact **214** is formed on the second columnar silicon layer **207**. In addition, the electric contact **214** is composed of a barrier metal layer **176** and metal layers **177** and **178**. Also, the electric contact **214** is directly formed on the second p+ type silicon layer **146**. Accordingly, the electric contact **214** and the second p+ type silicon layer **146** are connected directly. In this embodiment, the electric contact **214** is contacted with the second p+ type silicon layer **146**.

The barrier metal layer **176** is formed of metal, such as titanium or tantalum. The second p+ type silicon layer **146** is connected to an output wiring **220** via the electric contact **214**. The output of PMOS-SGT is outputted to the output wiring **220**.

[0035] Also, as mentioned above, an electric contact **215** formed on the seventh metal-silicon compound layer **159c** is connected to an input wiring **221**, and the potential for forming a channel in the second silicon layer **120** is applied to the second gate electrode **209** from the input wiring **221**. Furthermore, the gate electrodes **210** and **209** are connected by the gate wiring **218**.

Also, an electric contact **213** is formed on the fourth metal-silicon compound layer **158**. The electric contact **213** is composed of a barrier metal layer **173** and metal layers **174** and **175**. The electric contact **213** is connected to the power source wiring **219** in order to input power supply potential into PMOS-SGT. The power source wiring **219** is composed of a barrier metal layer **195**, a metal layer **196**, and a barrier metal layer **197**.

The PMOS-SGT is formed according to such a configuration.

[0036] Furthermore, an oxide film **126** is formed between the first planar silicon layer **212** and the second planar silicon layer **211** of adjoining PMOS-SGT, and a first insulating film **129a** and a second insulating film **129b** extends on the oxide film **126**. Also, each transistor is separated by a nitride film **161** and an interlayer insulating film **162**.

An inverter provided with the NMOS-SGT and PMOS-SGT is formed according to such a configuration.

In this embodiment, the first metal-silicon compound layer **159a**, third metal-silicon compound layer **159b**, and seventh metal-silicon compound layer **159c** are formed in the same processing step by using the same material in one piece. Also, the first insulating film **129a** and second insulating film **129b** are formed in the same processing step by using the same material in one piece.

In the inverter according to this embodiment, the first gate insulating film **140** and first metal film **138** are formed by using a material which applies the NMOS-SGT an enhancement type, and the second gate insulating film **139** and second metal film **137** are formed by using a material which applies the PMOS-SGT an enhancement type. Therefore, the short circuit conduction current which flows at the time of operation of

this inverter can be reduced.

[0037] Hereinafter, an example of a fabrication method for forming the inverter provided with the SGT of the first embodiment of this application will be explained with reference to FIG. 3A to FIG. 148B. In the drawings, the same components are denoted by the same reference numerals.

In FIG. 3A to FIG. 4B, FIG. 3 (a) shows a top view, FIG. 3B shows a cross-sectional diagram taken in the cutting line **X-X'** of FIG. 3A, FIG. 4A is a cross-sectional diagram taken in the cutting line **Y1-Y1'** of FIG. 3A, and FIG. 4B shows a cross-sectional diagram taken in the cutting line **Y2-Y2'** of FIG. 3A. Also in the following, it is similar for FIG. 5A to FIG. 148B.

[0038] As shown in FIG. 3A to FIG. 4B, a nitride film **103** is further formed on a substrate composed of a silicon dioxide film **101** and a silicon layer 102. A substrate consisting of silicon may be used. Alternatively, a substrate by which an oxide film is formed on silicon and a silicon layer is formed on the oxide film may be used. In this embodiment, an i type silicon layer is used as the silicon layer **102**. An impurity is doped into the part acting as a channel of SGT when using a p type silicon layer and a n type silicon layer as the silicon layer **102**. Alternatively, a thin n type silicon layer or a thin p type silicon layer may be used instead of the i type silicon layer.

[0039] As shown in FIG. 5A to FIG. 6B, resists **104** and **105** for forming a hard mask for formation of the columnar silicon layer is formed.

[0040] As shown in FIG. 7A to FIG. 8B, the nitride film **103** is etched to form hard masks **106** and **107**.

[0041] As shown in FIG. 9A to FIG. 10B, the silicon layer **102** is etched by applying the hard mask **106** and **107** as a mask to form columnar silicon layers **207** and **208**.

[0042] As shown in FIG. 11A to FIG. 12B, the resists **104** and **105** are removed.

[0043] As shown in FIG. 13A to FIG. 14B, a surface of the silicon layer **102** is oxidized to form a sacrificing oxide film **108**. The sacrifice oxidation removes the silicon surface where carbon and the like are driven in the silicon etching.

[0044] As shown in FIG. 15A to FIG. 16B, etching removes the sacrificing oxide film **108**.

[0045] As shown in FIG. 17A to FIG. 18B, an oxide film **109** is formed on the results of the above-mentioned processing step.

[0046] As shown in FIG. 19A to FIG. 20B, the oxide film **109** is etched to remain in a sidewall shape on sidewalls of the columnar silicon layers, and thereby sidewalls **110** and **111** are formed. When an n+ type silicon layer is formed into a lower part of the columnar silicon layers **207** and **208** by impurity implantation, the impurity is not doped into a channel by the sidewalls **101** and **111**, and therefore a variation in threshold voltage of the SGT can be suppressed.

[0047] As shown in FIG. 21A to FIG. 22B, a resist **112** for implanting the impurity into the lower part of the columnar silicon layer **208** is formed.

[0048] As the arrow shows FIG. 23B and FIG. 24A, arsenic is implanted into the silicon layer **102** of a formation scheduled region of the NMOS-SGT to form an n+ type silicon layer **113a** under the columnar silicon layer 208. Accordingly, as shown in FIG. 23A to FIG. 24B, the region of the first silicon layer **114** in the columnar silicon layer **208** and the planar region of the silicon layer **102** are separated.

[0049] As shown in FIG. 25A to FIG. 26B, the resist **112** is removed.

[0050] As shown in FIG. 27A to FIG. 28B, the sidewalls **110** and **111** are removed by etching.

[0051] Next, annealing is performed to activate the implanted impurity (arsenic). Accordingly, as shown in FIG. 29A to FIG. 30B, the implanted impurity is diffused in a part of the silicon layer **102** and columnar silicon layer **208**.

[0052] As shown in FIG. 31A to FIG. 32B, an oxide film **115** is formed on the results of the above-mentioned processing step.

[0053] As shown in FIG. 33A to FIG. 34B, the oxide film **115** is etched, to remain in the sidewall of the columnar silicon layers **207** and **208** in a sidewall shape, and thereby sidewalls **116** and **117** are formed. When forming a p+ type silicon layer under the columnar silicon layers **207** and **208** by impurity implantation, the impurity is

not doped into a channel region by the sidewalls **116** and **117**, and therefore a variation of a threshold value voltage of the SGT can be suppressed.

[**0054**] As shown in FIG. 35A to FIG. 36B, a resist **118** for implanting an impurity into the silicon layer **102** under the columnar silicon layer **207** is formed.

[**0055**] As shown in FIG. 37A to FIG. 38B, for example, boron is implanted into the silicon layer **102** of a formation scheduled region of the PMOS-SGT to form a p+ type silicon layer **119a** under the columnar silicon layer **207**. Accordingly, as shown in FIG. 37A to FIG. 38B, the region of the second silicon layer **120** in the columnar silicon layer **207** is separated from the planar silicon layer region.

[**0056**] As shown in FIG. 39A to FIG. 40B, the resist **118** is removed.

[**0057**] As shown in FIG. 41A to FIG. 42B, the sidewalls **116** and **117** is etched to remove.

[**0058**] Next, annealing is performed to activate the implanted impurity (boron). Accordingly, as shown in FIG. 43A to FIG. 44B, the implanted impurity is diffused in a part of the silicon layer **102** and columnar silicon layer **207**.

[**0059**] As shown in FIG. 45A to FIG. 46B, an oxide film **121** is formed on the results of the above-mentioned processing step. The oxide film **121** protects the first silicon layer **114** and second silicon layer **120** from the resist for the formation of the planar silicon layer to be performed in the following processing step.

[**0060**] As shown in FIG. 47A to FIG. 48B, resists **122** and **123** for the formation of the planar silicon layer is formed.

[**0061**] As shown in FIG. 49A to FIG. 50B, a part of the oxide films 121 between the columnar silicon layers **207** and **208** is etched and separated into oxide films **124** and **125**.

[**0062**] As shown in FIG. 51A to FIG. 52B, a part of the p+ type silicon layer **119a** and n+ type silicon layer **113a** is etched. Accordingly, planar silicon layers **211** and **212** having the p+ type silicon layer **119** and the first n+ type silicon layer **113** which remained, respectively, are formed.

[**0063**] As shown in FIG. 53A to FIG. 54B, the resists **122** and **123** is removed.

[0064] As shown in FIG. 55A to FIG. 56B, an oxide film **126a** is thickly formed so that these results is embedded on the results of the above-mentioned processing step.

[0065] As shown in FIG. 57A to FIG. 58B, chemical mechanical polishing (CMP) is performed by applying the hard masks **106** and **107** as a stopper to planarize the oxide film **126a**.

[0066] Next, the oxide film **126a** and oxide films **124** and **125** are etched, and as shown in FIG. 59A to FIG. 60B, an oxide film **126** which fills between the planar silicon layers **211** and **212** is formed.

[0067] As shown in FIG. 61A to FIG. 62B, an oxide film **128** is formed on the results of the above-mentioned processing step. The oxide film **128** is thickly formed on the first n+ type silicon layer **113**, p+ type silicon layer **119**, oxide film **126**, and hard masks **106** and **107**, and the oxide film **128** is thinly formed on the sidewall of the columnar silicon layers **207** and **208**.

[0068] As shown in FIG. 63A to FIG. 64B, a part of oxide films **128** are etched to remove the oxide film **128** formed on the sidewall of the columnar silicon layers **207** and **208**. The etching is preferably isotropically performed. The oxide film **128** is thickly formed on the first n+ type silicon layer **113**, p+ type silicon layer **119**, oxide film **126**, and hard masks **106** and **107**, and thinly formed on the sidewalls of the columnar silicon layers **207** and **208**, and therefore even after the oxide film on the sidewalls of the columnar silicon layers has been etched, a part of the oxide film **128** remains on the first n+ type silicon layer **113**, p+ type silicon layer **119**, and oxide film **126** to form into an insulating film **129c**. In this case, oxide films **130** and **131** also remain on the hard masks **106** and **107**.

The insulating film **129c** becomes first and second insulating films **129a** and **129b** in the following processing step, and the first and second insulating films **129a** and **129b** can reduce parasitic capacitances between the gate electrode and the planar silicon layer.

[0069] As shown in FIG. 65A to FIG. 66B, an insulating film **132** is formed on the results of the above-mentioned processing step. The insulating film **132** is a film

including any one of an oxide film, nitride film, or high dielectric film. Also, hydrogen atmosphere annealing or epitaxial growth may be performed for the columnar silicon layers **207** and **208** before the film formation of the insulating film **132**.

[**0070**] As shown in FIG. 67A to FIG. 68B, a metal film **133** is formed on the insulating film **132**. The metal film **133** is preferably a film including titanium nitride or tantalum nitride. By using the metal film **133**, depleting of the channel region can be suppressed, and low-resistivity of the gate electrode can be achieved. Moreover, depending on a material for the metal film **133**, a threshold voltage of the transistors can also be set. It is necessary to apply all the processing steps after this process into a fabricating processing step so as to suppress the metallic contamination by the metal gate electrode.

[**0071**] As shown in FIG. 69A to FIG. 70B, a polysilicon film **134** is formed on the results of the above-mentioned processing step. In order to suppress the metallic contamination, it is preferable to form the polysilicon film **134** using atmospheric pressure CVD.

[**0072**] As shown in FIG. 71A to FIG. 72B, the polysilicon film **134** is etched to form polysilicon films **135** and **136** made to remain in a sidewall shape on the sidewall of the columnar silicon layers **207** and **208** and the sidewall of the hard masks **106** and **107.**

[**0073**] As shown in FIG. 73A to FIG. 74B, the metal film **133** is etched. The metal film **133** of the sidewall of the columnar silicon layers **207** and **208** is protected by the polysilicon films **135** and **136** without being etched, and forms metal films **137a** and **138a** remaining in a sidewall shape on the sidewall of the columnar silicon layers **207** and **208** and the sidewall of the hard masks **106** and **107**.

[**0074**] Next, the insulating film **132** is etched. As shown in FIG. 75A to FIG. 76B, the insulating film **132** of the sidewall of the columnar silicon layers **207** and **208** is protected by the polysilicon films **135** and **136** without being etched, and forms gate insulating films **139a** and **140a** remaining in a sidewall shape on the sidewall of the columnar silicon layers **207** and **208** and the sidewall of the hard masks **106** and **107**.

[0075] As shown in FIG. 77A to FIG. 78B, a polysilicon film **141** is formed on the results of the above-mentioned processing step. In order to suppress the metallic contamination, it is preferable to form the polysilicon film **141** using atmospheric pressure CVD.

In the case of using a high dielectric film for the gate insulating films **139** and **140**, this high dielectric film may act as a source of the metal contamination. By forming the polysilicon film **141**, the gate insulating film **139a** and metal film **137a** are covered with the columnar silicon layer **207**, polysilicon films **135** and **141**, insulating film **129c**, and hard mask **106**. Also, the gate insulating film **140a** and metal film **138a** are covered with the columnar silicon layer **208**, the polysilicon films **136** and **141**, insulating film **129c**, and hard mask **107**. That is, the gate insulating films **139a** and **140a** and metal films **137a** and **138a** acting as the contamination sources are covered with the columnar silicon layers **207** and **208**, the polysilicon films **135**, **136**, and **141**, insulating film **129c**, and hard masks **106** and **107**, and therefore the metal contamination due to a metal included in the gate insulating films **139a** and **140a** and metal films **137a** and **138a** can be suppressed.

After the metal film has been thickly formed and etched to remain in the sidewall shape, and then the gate insulating film has been etched, the polysilicon films is formed, thereby forming the structure in which the gate insulating films and metal films are covered with the columnar silicon layers, polysilicon films, insulating film, and hard masks.

[0076] As shown in FIG. 79A to FIG. 80B, a polysilicon film layer **142** is formed on the results of the above-mentioned processing step so that these results is embedded. Since between the columnar silicon **207** and **208** is embedded, it is preferable to form the polysilicon film **142** using a low-pressure CVD. The gate insulating films **139a** and **140a** and metal films **137a** and **138a** acting as the contamination sources are covered with the columnar silicon layers **207** and **208**, polysilicon films **135**, **136**, and **141**, insulating film **129c**, and hard masks **106** and **107**, and therefore the low pressure CVD can be used.

[0077] As shown in FIG. 81A to FIG. 82B, a chemical mechanical polishing (CMP) is performed by applying the oxide films **130** and **131** into a polishing stopper to planarize the polysilicon film **142**.

[0078] As shown in FIG. 83A to FIG. 84B, the oxide films **130** and **131** is etched. After etching the oxide film, a chemical mechanical polishing may be performed by applying the hard masks **106** and **107** into a polishing stopper.

[0079] As shown in FIG. 85A to FIG. 86B, the polysilicon films **135a**, **136a**, **141** and **142** are etched back, and the polysilicon films **135a**, **136a**, **141** and **142** are removed to a top edge of the gate insulating films **139** and **140** which are formed and a formation scheduled region of the gate electrode. The etch-back determines gate lengths of the SGTs. According to this processing step, the upper region of the metal films **137** and **138** is exposed.

[0080] As shown in FIG. 87A to FIG. 88B, the metal films **137** and **138** of the upper sidewall of the columnar silicon layers **207** and **208** are etched and then removed to form the metal films **137** and **138**.

[0081] As shown in FIG. 89A to FIG. 90B, the gate insulating films **139a** and **140a** of the upper sidewall of the columnar silicon layers **207** and **208** are etched and then removed to form gate insulating films **139** and **140**.

[0082] As shown in FIG. 91A to FIG. 92B, a resist **143** for forming the second n+ type silicon layer **144** in the upper part of the columnar silicon layer **208** is formed.

[0083] As shown in FIG. 93B and FIG. 94A as arrows, arsenic is implanted. Accordingly, as shown in FIG. 93A to FIG. 94B, a second n+ type silicon layer **144** is formed in the upper part of the columnar silicon layer **208**. Assuming that a line vertical to the substrate be 0 degree, an angle at which the arsenic is implanted is in the range of 10 to 60 degrees, and in particular, a high angle of 60 degrees is preferable. This is because the hard mask **107** is disposed on the columnar silicon layer **208**.

[0084] As shown in FIG. 95A - FIG. 96B, the resist **143** is removed. Then, annealing treatment is performed.

[0085] As shown in FIG. 97A to FIG. 98B, a resist **145** for forming the p+ type

silicon layer **146** in the upper part of the columnar silicon layer **207** is formed.

[0086] As shown in FIG. 99A to FIG. 100B, for example, boron is implanted to form the p+ type silicon layer **146** in the upper part of the columnar silicon layer **207**. Assuming that a line vertical to the substrate be 0 degree, an angle at which the boron is implanted is in the range of 10 to 60 degrees, and in particular, a high angle of 60 degrees is preferable. This is because the hard mask **106** is disposed on the columnar silicon layer **207**.

[0087] As shown in FIG. 101A to FIG. 102B, the resist **145** is removed.

[0088] As shown in FIG. 103A to FIG. 104B, an oxide film **147** is formed on the results of the above-mentioned processing step. The oxide film **147** is preferably one formed by atmospheric pressure CVD. The oxide film **147** enables a subsequent nitride film **148** to be formed by low pressure CVD.

[0089] As shown in FIG. 105A to FIG. 106B, a nitride film **148** is formed. The nitride film **148** is preferably one formed by the low pressure CVD. This is because the low-pressure CVD is effective in homogeneity as compared with atmospheric pressure CVD.

[0090] As shown in FIG. 107A to FIG. 108B, the nitride film **148** and oxide film **147** are etched to form a first insulating film sidewall **223** and second insulating film sidewall **224**. The first insulating film sidewall **223** is composed of the nitride film **150** and oxide film **152** which remained by the etching, and the second insulating film sidewall **224** is composed of the nitride film **149** and oxide film **151** which remained by the etching.

The sum of a film thicknesses of the nitride film **149** and oxide film **151**, which are made to remain in the sidewall shape, will correspond to a film thickness of the gate electrodes afterward, and therefore by adjusting the deposition thicknesses and etching conditions of the oxide and nitride films **147** and **148**, the gate electrodes having a desired thickness can be formed.

Also, the sum of a film thickness of the insulating film side walls **223** and **224** and a radius of the columnar silicon layers **207** and **208** is preferably larger than an

outer circumferential radius of a cylinder formed by the gate insulating films **139** and **140** and metal films **137** and **138**. Since the sum of the film thickness of the insulating film side walls **223** and **224** and radius of the columnar silicon layers **207** and **208** is larger than the outer circumferential radius of the cylinder formed by the gate insulating films **139** and **140** and metal films **137** and **138**, metal films **137** and **138** are covered with the polysilicon film after gate etching, and therefore the metal contamination can be suppressed.

Further, on the basis of this processing step, the upper surfaces of the columnar silicon layers **207** and **208** have a structure covered with the hard masks **106** and **107** and insulating film sidewalls **223** and **224**, respectively. The structure eliminates the formation of a metal-semiconductor compound on the surfaces of the columnar silicon layers **207** and **208**. Still further, since the upper surfaces of the columnar silicon layers **207** and **208** have the structure covered with the hard masks **106** and **107** and insulating film sidewalls **223** and **224**, the n+ type silicon layer and p+ type silicon layer are formed before the polysilicon is etched and the gate electrode is formed as explained using FIG. 91A to FIG. 102B.

[**0091**] As shown in FIG. 109A to FIG. 110B, a resist **153** for forming the gate wiring **218** is formed.

[**0092**] As shown in FIG. 111A to FIG. 112B, the polysilicon films **142**, **141**, **135** and **136** are etched to form gate electrodes **209** and **210** and a gate wiring **218**.

The gate electrode **209** is composed of the metal film **137** and polysilicon films **154** and **155** which react to metal to form a metal silicon compound in the following process, and the gate electrode **210** is composed of the metal film **138** and polysilicon films **156** and **157** which react to metal to form a metal silicon compound in the following processing step. The gate wiring **218** which connects between the gate electrode **209** and gate electrodes **210** is composed of the polysilicon films **154**, **155**, **142**, **156** and **157** which react to metal to form a metal silicon compound in the following processing step. In addition, the polysilicon film **154** and**157** is a part which remained after the etching of the polysilicon films **135** and **136**, and the

polysilicon films **155** and **156** are a part which remained after the etching of the polysilicon film **141**. Since the sum of the film thickness of the insulating film side walls **223** and **224** and radius of the columnar silicon layers **207** and **208** is larger than the outer circumferential radius of the cylinder formed by the gate insulating films **139** and **140** and metal films **137** and **138**, the metal films **137** and **138** are covered with the polysilicon films **154**, **155**, **142**, **156** and **157** after the gate etching, and therefore the metal contamination can be suppressed.

[0093] As shown in FIG. 113A to FIG. 114B, the insulating film **129c** is etched to form first insulating films **129a** and second insulating film **129b**, and to expose the surface of the p+ type silicon layer **119** and first n+ type silicon layer **113**. In this embodiment, since the first and second insulating films **129a** and **129b** are formed in the same processing step by using the same material in one piece as above-mentioned, reference numeral **129** denotes the first and second insulating films in the cross-sectional diagram taken in the cutting line **X-X'** of FIG. 113 to FIG. 147.

[0094] As shown in FIG. 115A to FIG. 116B, the resist **150** is removed. There is obtained a structure in which the gate insulating film **140** and metal film **138** are covered with the columnar silicon layer **208**, the polysilicon films **156** and **157**, the first insulating film **129 (129a)**, and first insulating film sidewall **223**, and the second gate insulating film **139** and second metal film **137** are covered with the second columnar silicon layer **207**, polysilicon films **154** and **155**, second insulating film **129 (129b)**, and second insulating film sidewall **224**. Also, there is obtained a structure in which the upper parts of the columnar silicon layers **207** and **208** is covered with the hard masks **106** and **107** and insulating film sidewalls **224** and **223**. Such a structure eliminates the formation of a metal-semiconductor compound in the upper part of the columnar silicon layer **207** and **208**.

[0095] A metal such as Ni or Co is sputtered on the results of the above-mentioned processing step and then subjected to heat treatment to thereby react the gate electrode polysilicon films **154** and **155**, the gate electrode polysilicon films **154**, **155**, **142**, **156**, and **157**, and planar silicon layer with the sputtered metal. Then, an unreacted metal

film is removed by a sulfuric acid/hydrogen peroxide mixed solution or ammonia/hydrogen peroxide mixed solution. Accordingly, as shown in FIG. 117A to FIG. 118B, a metal-silicon compound layer **159 (159a** to **159C)** is formed for the gate electrodes **209** and **210** and gate wiring **218**; a metal-silicon compound layer **158** is formed in the planar silicon layer **211**; and a metal-silicon compound layer **160** is formed in the planar silicon layer **212**. Since the first, third, and seventh metal-silicon compound layers **159a** to **159c** are formed in the same processing step by using the same material in this embodiment, the cross-sectional diagram taken in the cutting line **X-X'** of FIG. 117 to FIG. 147 shows their bundling by the metal-silicon compound layer 159.

On the other hand, the upper surfaces of the columnar silicon layers **207** and **208** have the structure covered with the hard masks **106** and **107** and insulating film sidewalls **224** and **223**, and therefore in this processing step, any metal-silicon compound layer is not formed on the upper surfaces of the columnar silicon layers **207** and **208**.

Between the metal-silicon compound layer **159** and the metal films **137** and **138**, a polysilicon film may be present. Also, under the fourth metal-silicon compound layer 158, the p+ type silicon layer **119** may be present, and under the second metal-silicon compound layer 160, the first n+ type silicon layer **113** may be present.

[0096] A nitride film **161** is formed on the results of the above-mentioned processing step, and an interlayer insulating film **162** is formed so that the results in which the nitride film **161** is formed may be embedded. Next, as shown in FIG. 119A to FIG. 120B, the interlayer insulating film **162** is planarized.

[0097] As shown in FIG. 121A to FIG. 122B, a resist **163** for forming contact holes on the columnar silicon layers **207** and **208** is formed.

[0098] As shown in FIG. 123A to FIG. 124B, the interlayer insulating film **162** is etched by applying the resist **163** as a mask to form contact holes **164** and **165** on the columnar silicon layers **207** and **208**. At this time, it is preferable to etch parts of the nitride film **161** and hard masks **106** and **107** by over etching.

[0099] As shown in FIG. 125A to FIG. 126B, the resist **163** is removed.

[0100] As shown in FIG. 127A to FIG. 128B, a resist **166** for forming contact holes **167**, **168** and **169** in each on the planar silicon layers **211** and **212** and gate wiring **218** is formed.

[0101] As shown in FIG. 129A to FIG. 130B, the interlayer insulating film **162** is etched by applying the resist **166** as a mask, to form the contact holes **167**, **169** and **168** on the planar silicon layers **211** and **212** and gate wiring 218, respectively. The contact holes **164** and **165** on the columnar silicon layers **207** and **208**, and the contact holes **167**, **169** and **168** on the planar silicon layers **211** and **212** and gate wiring **218** are formed in the different processing steps, and therefore an etching condition for forming the contact holes **164** and **165** on the columnar silicon layers **207** and **208**, and an etching condition for forming the contact holes **167**, **169** and **168** on the planar silicon layers **211** and **212** and gate wiring **218** can be optimized, respectively.

[0102] As shown in FIG. 131A to FIG. 132B, the resist **166** is removed.

[0103] As shown in FIG. 133A to FIG. 134B, the nitride film **161** under the contact holes **167**, **168** and **169** is etched to remove, and the hard masks **106** and **107** are further etched to remove.

[0104] As shown in FIG. 135A to FIG. 136B, a barrier metal layer **170** formed by a metal, such as tantalum, tantalum nitride, titanium, or titanium nitride, is formed, and then a metal layer **171** is formed. At this time, a metal which forms the barrier metal layer **170** such as titanium and silicon in the upper parts of the columnar silicon layers **207** and **208** may react to form a compound of metal and silicon, and a fifth metal-silicon compound layer and a sixth metal-silicon compound layer may be formed at interfaces between the barrier metal layer **170** and the columnar silicon layers **207** and **208**. Depending on a material for the barrier metal layer, the fifth metal silicon compound layer and sixth metal silicon compound layer may not be formed.

[0105] As shown in FIG. 137A to FIG. 138B, a metal layer **172** is deposited on the results of the above-mentioned processing step.

[0106] As shown in FIG. 139A to FIG. 140B, the metal layers **172** and **171** and the

barrier metal layer **170** are planarized and etched to form electric contacts **213**, **214**, **215**, **216**, and **217**. The electric contact **213** includes the barrier metal layer **173** and the metal layers **174** and **175**. The electric contact **214** includes the barrier metal layer **176** and the metal layers **177** and **178**. The electric contact **215** includes the barrier metal layer **179** and the metal layers **180** and **181**. The electric contact **216** includes the barrier metal layer **182** and the metal layers **183** and **184**. The electric contact **217** includes the barrier metal layer **185** and the metal layers **186** and **187**.

[**0107**] As shown in FIG. 141A to FIG. 142B, a barrier metal layer **188**, metal layer **189**, and barrier metal layer **190** are sequentially formed on the results of the above-mentioned processing step.

[**0108**] As shown in FIG. 143A to FIG. 144B, resists **191**, **192**, **193** and **194** for forming power source wirings, input wiring, and output wiring are formed.

[**0109**] As shown in FIG. 145A to FIG. 146B, the barrier metal layer **190**, metal layer **189**, and barrier metal layer **188** are etched to form the power source wirings **219** and **222**, input wiring **221**, and output wire **220**. The power source wiring **219** includes barrier metal layer **195**, metal layer **196**, and barrier metal layer **197**. The power source wiring **222** includes barrier metal layer **204**, metal layer **205**, and barrier metal layer **206**. The input wiring **221** includes barrier metal layer **201**, metal layer **202**, and barrier metal layer **203**. The output wire **220** includes barrier metal layer **198**, metal layer **199**, and barrier metal layer **200**.

[**0110**] As shown in FIG. 147A to FIG. 148B, the resists **191**, **192**, **193** and **194** is removed.

[**0111**] According to the above processes, the semiconductor device according to this embodiment is formed.

According to the fabrication method of this embodiment, the electric contacts **214** and **216** can be directly formed on the columnar silicon layers **207** and **208**. Therefore, a thick metal semiconducting compound which may cause occurrence of leakage current is not formed on the columnar silicon layers **207** and **208**. Also, since it is not necessary to thickly form the second n+ type silicon layer **144** and the p+ type

silicon layer **146** comprising the highly doped silicon layers in order to suppress the occurrence of this leakage current, increase of the electrical resistance by the second n+ type silicon layer 144 and the p+ type silicon layer **146** of the highly doped silicon layers **144** and **146** is also avoidable.

Still Also, since the thick metal-silicon compound layers **158** to **160** can be formed in the gate electrodes **209** and **210** and the planar silicon layers **211** and **212** of the lower part of the columnar silicon layers **207** and **208**, the low-resistivity of the gate electrodes **209** and **210** and planar silicon layers **211** and **212** can be achieved. Accordingly, the high-speed operation of SGT becomes enabling.

Also, since the first insulating film **129a** and second insulating film **129b** are formed between the gate electrodes **209** and **210** and the planar silicon layers **211** and **212**, the parasitic capacitance between the gate electrode and the planar semiconductor layer can be reduced.

According to the configuration mentioned above, the low-resistivity and the miniaturization of the semiconductor device are achievable.

[0112] Although the fabrication method of the above-mentioned embodiment was explained using the inverter provided with the NMOS-SGT and PMOS-SGT, it can fabricate NMOS-SGT, PMOS-SGT, or a plurality of SGT(s) by the similar process.

[0113] In the above-mentioned embodiment, the case where the electric contact is contacted to the second highly doped silicon layer on the columnar semiconductor layer was explained. However, the fifth and sixth metal-silicon compound layers formed in the interface between the electric contact and the second highly doped silicon layer from a compound of a metal of the barrier metal layer and a semiconductor may be formed by making the metal of the barrier metal layer react to the silicon of the upper part of the columnar silicon layer when forming electric contact on a columnar silicon layer directly. In this case, since the fifth and sixth metal-silicon compound layers are thinly formed compared with the first to fourth and seventh metal-silicon compound layers, a problem of leakage current mentioned above is not occurred. Also, a metal included in the fifth and sixth metal-silicon compound layers is a metal which forms the

barrier metal layer, and differs from the metal included in the first to fourth and seventh metal-silicon compound layers. In addition, the fifth and sixth metal-silicon compound layers may be formed or may not be formed depending on the material of the barrier metal layer.

[0114] In the above-mentioned embodiment, although the case where the gate electrode includes the metal film was explained, it is not necessary to include the metal film if it can function as a gate electrode.

[0115] In the above-mentioned embodiment, although the transistor of the enhancement type by which the channel is formed in the region of the first silicon layer **114** and second silicon layer **120** by applying voltage to the first gate electrode **210** and second gate electrode **209** was explained, the transistor may be a depression type.

[0116] In the above-mentioned embodiment, although the example which uses silicon is shown as the semiconductor, it also enables to use germanium, a compound semiconductor, etc. if the formation of the SGT enables.

[0117] As for material(s) for forming the metal layer, the insulating film, etc. in the above-mentioned embodiment, well-known material(s) can be also used suitably.

[0118] The substance name(s) mentioned above is exemplifying and therefore the present invention is not limited to this example.

[0119]

Moreover, the present invention, to the extent that it does not deviate from the broad spirit and parameters of the present invention, may have various embodiments and modifications. In addition, the above described embodiment is provided to explain one embodiment of the present invention, but does not restrict the scope of the invention.

CLAIMS

Claim 1

A semiconductor device comprising:

a first planar semiconductor layer;

a first columnar semiconductor layer formed on the first planar semiconductor layer;

a first highly doped semiconductor layer formed in a lower region of the first columnar semiconductor layer and in the first planar semiconductor layer;

a second highly doped semiconductor layer formed in an upper region of the first columnar semiconductor layer and having a conductivity type the same as a conductivity type of the first highly doped semiconductor layer;

a first gate insulating film formed to surround the first columnar semiconductor layer on a sidewall of the first columnar semiconductor layer between the first highly doped semiconductor layer and the second highly doped semiconductor layer;

a first gate electrode formed to surround the first gate insulating film on the first gate insulating film;

a first insulating film formed between the first gate electrode and the first planar semiconductor layer;

a first insulating film sidewall formed to contact a top surface of the first gate electrode and an upper sidewall of the first columnar semiconductor layer, and to surround the upper region of the first columnar semiconductor layer;

a second metal-semiconductor compound layer formed in the same layer as the first planar semiconductor layer to contact the first highly doped semiconductor layer; and

a first contact formed on the second highly doped semiconductor layer,

wherein the first contact and the second highly doped semiconductor layer are connected directly,

the first gate electrode includes a first metal-semiconductor compound layer, and

the second metal-semiconductor compound layer is formed on the entire first planar semiconductor layer excluding a region where the first planar semiconductor layer overlaps with the first gate electrode.

Claim 2

The semiconductor device according to claim 1, further comprising a fifth metal-semiconductor compound layer formed between the first contact and the second highly doped semiconductor layer,

wherein the metal of the fifth metal-semiconductor compound layer is types of metal that are different from the metal of the first metal-semiconductor compound layer and the metal of the second metal-semiconductor compound layer.

Claim 3

The semiconductor device according to claim 1 or 2, wherein the first gate electrode further includes a first metal film formed between the first gate insulating film and the first metal-semiconductor compound layer,

wherein the first metal film contacts with the first metal-semiconductor compound layer.

Claim 4

A semiconductor device comprising: a first transistor and a second transistor,

wherein the first transistor includes:

a first planar semiconductor layer;

a first columnar semiconductor layer formed on the first planar semiconductor layer;

a first highly doped semiconductor layer of a second-conductivity type formed in a lower region of the first columnar semiconductor layer and the first planar semiconductor layer;

a second highly doped semiconductor layer of the second-conductivity type formed in an upper region of the first columnar semiconductor layer;

a first gate insulating film formed to surround the first columnar semiconductor layer on a sidewall of the first columnar semiconductor layer between the first highly doped semiconductor layer and the second highly doped semiconductor layer;

a first gate electrode formed to surround the first gate insulating film on the first gate insulating film;

a first insulating film formed between the first gate electrode and the first planar semiconductor layer;

a first insulating film sidewall formed to contact a top surface of the first gate electrode and an upper sidewall of the first columnar semiconductor layer and to surround the upper region of the first columnar semiconductor layer;

a second metal-semiconductor compound layer formed in the same layer as the first planar semiconductor layer to contact the first highly doped semiconductor layer; and

a first contact formed on the second highly doped semiconductor layer, and

the second metal-semiconductor compound layer is formed on the entire first planar semiconductor layer excluding a region where the first planar semiconductor layer overlaps with the first gate electrode,

wherein the second transistor includes:

a second planar semiconductor layer;

a second columnar semiconductor layer formed on the second planar semiconductor layer;

a third highly doped semiconductor layer of a first conductivity type formed in a lower region of the second columnar semiconductor layer and the second planar semiconductor layer;

a fourth highly doped semiconductor layer of the first conductivity type formed in an upper region of the second columnar semiconductor layer;

a second gate insulating film formed to surround the second columnar semiconductor layer on a sidewall of the second columnar semiconductor layer between the third highly doped semiconductor layer and the fourth highly doped semiconductor layer;

a second gate electrode formed to surround the second gate insulating film on the second gate insulating film;

a second insulating film formed between the second gate electrode and the second planar semiconductor layer;

a second insulating film sidewall formed to contact a top surface of the second gate electrode and an upper sidewall of the second columnar semiconductor layer, and to surround the upper region of the second columnar semiconductor layer;

a fourth metal-semiconductor compound layer formed in the same layer as the second planar semiconductor layer to contact the third highly doped semiconductor layer; and

a second contact formed on the fourth highly doped semiconductor layer, and

the fourth metal-semiconductor compound layer is formed on the entire second planar semiconductor layer excluding a region where the second planar semiconductor layer overlaps with the second gate electrode, and

wherein the first contact and the second highly doped semiconductor layer are connected directly,

the second contact and the fourth highly doped semiconductor layer are connected directly,

the first gate electrode includes a first metal-semiconductor compound layer, and

the second gate electrode includes a third metal-semiconductor compound layer.

Claim 5

The semiconductor device according to claim 4, further comprising:

a fifth metal-semiconductor compound layer formed between the first contact and the second highly doped semiconductor layer; and

a sixth metal-semiconductor compound layer formed between the second contact and the fourth highly doped semiconductor layer,

wherein the metal of the fifth metal-semiconductor compound layer is types of metal that are different from the metal of the first metal-semiconductor compound layer and the metal of the second metal-semiconductor compound layer, and

the metal of the sixth metal-semiconductor compound layer is types of metal that are different from the metal of the third metal-semiconductor compound layer and the metal of the fourth metal-semiconductor compound layer.

Claim 6

The semiconductor device according to claim 4 or 5, wherein the first gate electrode further includes a first metal film formed between the first gate insulating film and the first metal-semiconductor compound layer; and

the second gate electrode further includes a second metal film formed between the second gate insulating film and the third metal-semiconductor compound layer.

Claim 7

The semiconductor device according to claim 6, wherein the first gate insulating film and the first metal film are formed from materials for configuring the first transistor to be an enhancement type, and

the second gate insulating film and the second metal film are formed from materials for configuring the second transistor to be an enhancement type.

Claim 8

A fabrication method for a semiconductor device for fabricating the semiconductor device according to claim 3, the fabrication method of the semiconductor device comprising:

a step of preparing a structure including: the first planar semiconductor layer; the first columnar semiconductor layer formed on the first planar semiconductor layer and having a hard mask formed in a top surface thereof; the first highly doped semiconductor layer formed in a lower region of the first planar semiconductor layer and in the first columnar semiconductor layer; and a third insulating film formed on the hard mask and on the first planar semiconductor layer;

a step of forming a fourth insulating film, a third metal film, and a first semiconductor film in this order on the structure;

a step of etching the first semiconductor film to make the first semiconductor film remain in a shape of a sidewall on the sidewall of the first columnar semiconductor layer;

a step of etching the third metal film to remain on the sidewall of the first columnar semiconductor layer in a shape of the sidewall;

a fourth insulating film etching step of etching the fourth insulating film to remained on the sidewall of the first columnar semiconductor layer in a shape of the sidewall;

a second semiconductor film forming step of forming a second semiconductor film on results of the fourth insulating film etching step;

a step of forming a third semiconductor film to embed results of the second semiconductor film forming;

a step of planarizing the second semiconductor film, the third semiconductor film and the first semiconductor film;

a step of etching back the planarized second semiconductor film, third semiconductor film and first semiconductor film so that an upper region of the third metal film is exposed;

a step of etching the third metal film made remaining in the shape of the sidewall and the fourth insulating film made remaining in the shape of the sidewall to expose the upper sidewall of the first columnar semiconductor layer, to form the first metal film and the first gate insulating film;

a second highly doped semiconductor layer forming step of forming a second highly doped semiconductor layer having a conductivity type the same as the first highly doped semiconductor layer in the upper region of the first columnar semiconductor layer;

a step of forming an oxide film and a nitride film sequentially on results of the second highly doped semiconductor layer forming step;

a step of etching the oxide film and the nitride film so that the oxide film and the nitride film remain in a shape of the sidewall on the upper sidewall of the first columnar semiconductor layer and on a sidewall of the hard mask, to form the first insulating film sidewall;

a semiconductor film etching step of etching the first semiconductor film, the second semiconductor film and the third semiconductor film to make at least a part of the first semiconductor film and the second semiconductor film remain to surround the first metal film on a first metal film sidewall;

a first planar semiconductor layer exposure step of etching the third insulating film

on the first planar semiconductor layer, exposed in the semiconductor film etching step, to be removed and exposing the first planar semiconductor layer;

a metal and semiconductor reaction step of depositing and then annealing a metal on results of the first planar semiconductor layer exposure step, to make the deposited metal react with a semiconductor included in the first planar semiconductor layer, and make the deposited metal react with a semiconductor included in the first semiconductor film and the second semiconductor film made to remain on the first metal film; and

a step of removing unreacted metal in the metal and semiconductor reaction step, to form the second metal-semiconductor compound layer in the first planar semiconductor layer, and form the first metal-semiconductor compound layer in the first gate electrode.

Claim 9

The fabrication method of the semiconductor device according to claim 8, further comprising:

a step of removing the third insulating film on the hard mask; and

a step of directly forming the first contact on the second highly doped semiconductor layer formed in the upper part of the first columnar semiconductor layer.