

(19) World Intellectual Property
Organization
International Bureau



(43) International Publication Date
30 January 2003 (30.01.2003)

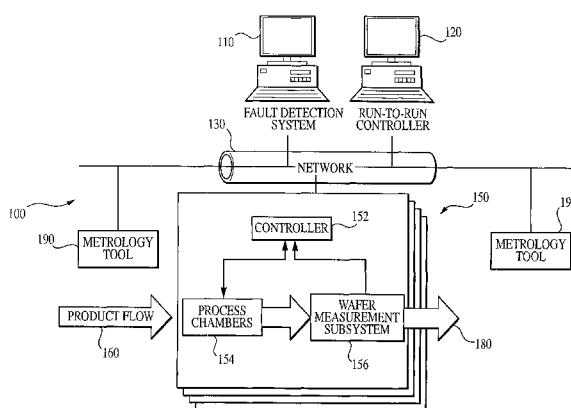
PCT

(10) International Publication Number
WO 2003/009345 A3

- (51) International Patent Classification⁷: **G05B 19/418**, H01L 21/66
- (21) International Application Number: PCT/US2002/021942
- (22) International Filing Date: 12 July 2002 (12.07.2002)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:
60/305,140 16 July 2001 (16.07.2001) US
10/135,405 1 May 2002 (01.05.2002) US
- (71) Applicant: **APPLIED MATERIALS, INC.** [US/US];
P.O. Box 450A, Santa Clara, CA 95052 (US).
- (72) Inventors: **REISS, Terry, P.**; 385 Bay Street, San Jose, CA 95123 (US). **SHANMUGASUNDRAM, Arulkumar, P.**; 428 Madera Avenue #10, Sunnyvale, CA 94086 (US). **SCHWARM, Alexander, T.**; 9303 La Puente Drive, Austin, TX 78749 (US).
- (74) Agents: **ALTER, Scott, M.** et al.; Hale and Dorr LLP, 1455 Pennsylvania Avenue, N.W., Washington, DC 20004 (US).
- (81) Designated States (*national*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZM, ZW.
- (84) Designated States (*regional*): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).
- Published:**
— with international search report
- (88) Date of publication of the international search report:
8 January 2004

[Continued on next page]

(54) Title: INTEGRATION OF FAULT DETECTION WITH RUN-TO-RUN CONTROL



(57) **Abstract:** Semiconductor wafers are processed in conjunction with a manufacturing execution system using a run-to-run controller and a fault detection system. A recipe is received from the manufacturing execution system by the run-to-run controller for controlling a tool. The recipe includes a setpoint for obtaining one or more target wafer properties. Processing of the wafers is monitored by measuring processing attributes including fault conditions and wafer properties using the fault detection system and one or more sensors. Setpoints of the recipe may be modified at the run-to-run controller according to the processing attributes to maintain the target wafer properties, except in cases when a fault condition is detected by the fault detection system. Thus, data acquired in the presence of tool or wafer fault conditions are not used for feedback purposes. In addition, fault detection models may be used to define a range of conditions indicative of a fault condition. In these cases, the fault detection models may be modified to incorporate, as parameters, setpoints of a recipe modified by a run-to-run controller.



For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.