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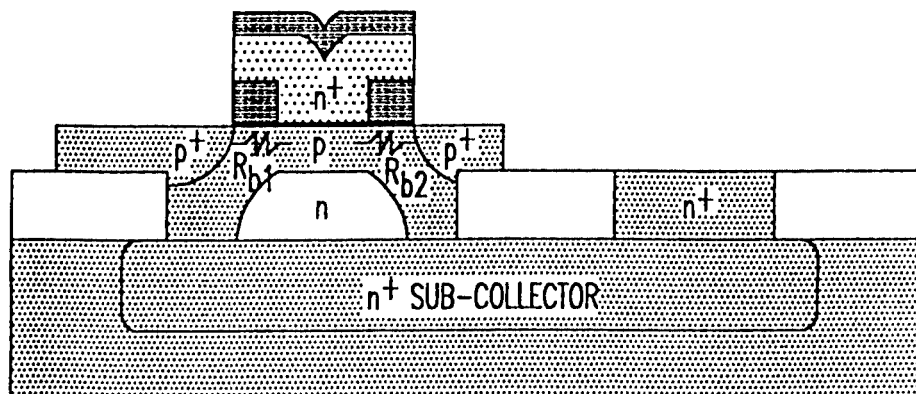
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(54) Title: A NON-SELF-ALIGNED SIGE HETEROJUNCTION BIPOLAR TRANSISTOR



(57) Abstract: A method for making a non-self-aligned, heterojunction bipolar transistor includes forming extrinsic base regions (70) with a PFET source/drain implant aligned with the polysilicon in an emitter stack but which are not directly aligned with an emitter opening defined in that stack. This is achieved by making the emitter pedestal (66) wider than the emitter opening. This advantageously removes the dependency of alignment between the extrinsic base regions and the emitter opening, thereby resulting in fewer process steps, reduced thermal cycles, and improved speed.



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