SEMICONDUCTOR DEVICES

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This patent application claims priority to Korean Patent Application No. 10-2022-0106707, filed on 25 August 2022 in the Korean Intellectual Property Office (KIPO), the contents of which are herein incorporated by reference in their entirety.

TECHNICAL FIELD

[0002] Example embodiments relate to semiconductor devices. More particularly, example embodiments relate to semiconductor devices including a plurality of channels sequentially stacked in a vertical direction.

BACKGROUND

[0003] In a method of manufacturing a semiconductor device including a plurality of channels sequentially stacked in a vertical direction, a dummy gate structure and a gate spacer may be formed on sacrificial lines and semiconductor lines alternately and repeatedly stacked in the vertical direction. An etching process is performed using the dummy gate structure and the gate spacer as an etching mask to etch the semiconductor lines and the sacrificial lines to form semiconductor patterns and sacrificial patterns, respectively. A source/drain layer is formed to contact sidewalls of the semiconductor patterns, an opening is formed through the sacrificial patterns by an etching process, and a gate structure is formed in the opening.

[0004] As the etching processes are performed, a curing process or a cleansing process is performed to cure damage to the patterns and remove an etching residue. Undesired oxide layers may be formed or some of the patterns may be removed by the curing process or the

cleansing process. Accordingly, electrical insulation between some of the patterns may deteriorate, which may cause an electrical short between the patterns.

SUMMARY

[0005] Example embodiments provide a semiconductor device having enhanced characteristics.

[0006] According to example embodiments, there is provided a semiconductor device. The semiconductor device may include channels spaced apart from each other on a substrate in a vertical direction substantially perpendicular to an upper surface of the substrate, a gate structure on the substrate and bordering lower and upper surfaces and a first sidewall of at least a portion of each of the channels, and a source/drain layer on a portion of the substrate adjacent to the gate structure and contacting second sidewalls of the channels. A nitrogen-containing portion may be formed at an upper portion of an uppermost one of the channels, and may be doped with nitrogen.

[0007] According to example embodiments, there is provided a semiconductor device. The semiconductor device may include channels spaced apart from each other on a substrate in a vertical direction substantially perpendicular to an upper surface of the substrate, a gate structure on the substrate and bordering lower and upper surfaces and a first sidewall of at least a portion of each of the channels, a source/drain layer on a portion of the substrate adjacent to the gate structure and contacting second sidewalls of the channels, and an oxide pattern on an upper surface of an end portion of an uppermost one of the channels and including silicon oxynitride.

[0008] According to example embodiments, there is provided a semiconductor device. The semiconductor device may include an active pattern on a substrate, channels spaced apart from each other on the active pattern in a vertical direction substantially perpendicular

to an upper surface of the substrate, a gate structure on the substrate and bordering lower and upper surfaces and a first sidewall of at least a portion of each of the channels, a source/drain layer on a portion of the substrate adjacent to the gate structure and contacting second sidewalls of the channels, a gate spacer on an upper sidewall of the gate structure, a nitrogen-containing portion at an upper portion of an uppermost one of the channels, and an oxide pattern between an upper surface of each of opposite end portions of the uppermost one of the channels and a lower surface of the gate spacer.

[0009] In the semiconductor device in accordance with example embodiments, the electric insulation between the gate structure and the source/drain layer may be enhanced, so that the risk of an electric short between the gate structure and the source/drain layer may be reduced.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] FIGS. 1, 2, 3, 4 and 5 are a plan view and cross-sectional views illustrating a semiconductor device in accordance with example embodiments.

[0011] FIGS. 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17A, 17B, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, 31 and 32 are plan views and cross-sectional views illustrating a method of manufacturing a semiconductor device in accordance with example embodiments.

[0012] FIG. 33 is a cross-sectional view illustrating a semiconductor device in accordance with example embodiments.

[0013] FIG. 34 is a cross-sectional view illustrating a method of manufacturing a semiconductor device in accordance with example embodiments.

[0014] FIG. 35 is a cross-sectional view illustrating a semiconductor device in accordance with example embodiments.

[0015] FIGS. 36 and 37 are cross-sectional views illustrating a method of manufacturing a

semiconductor device in accordance with example embodiments.

[0016] FIGS. 38 and 39 are cross-sectional views illustrating semiconductor devices in accordance with example embodiments.

DESCRIPTION OF EMBODIMENTS

[0017] A semiconductor device and a method of manufacturing the same in accordance with example embodiments will be described more fully hereinafter with reference to the accompanying drawings. Hereinafter in the specifications (and not necessarily in the claims), two directions among horizontal directions substantially parallel to an upper surface of a substrate, which may cross each other, may be referred to as first and second directions D1 and D2, respectively, and a vertical direction substantially perpendicular to the upper surface of the substrate may be referred to as a third direction D3. In example embodiments, the first and second directions D1 and D2 may be substantially perpendicular to each other. Like reference numerals refer to like elements throughout this application. As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items. It is noted that aspects described with respect to one embodiment may be incorporated in different embodiments although not specifically described relative thereto. That is, all embodiments and/or features of any embodiments can be combined in any way and/or combination.

[0018] FIGS. 1 to 5 are a plan view and cross-sectional views illustrating a semiconductor device in accordance with example embodiments. In particular, FIG. 1 is the plan view, and FIGS. 2 to 5 are the cross-sectional views. FIG. 2 is a cross-sectional view taken along line A-A' of FIG. 1, FIG. 3 is a cross-sectional view taken along line B-B' of FIG. 1, and FIG. 5 is a cross-sectional view taken along line C-C' of FIG. 1. FIG. 4 is an enlarged cross-sectional view of region X of FIG. 3.

[0019] Referring to FIGS. 1 to 5, the semiconductor device may include an active pattern 105, an isolation pattern 130, semiconductor patterns 124, a second oxide pattern 124b, a gate structure 290, a gate spacer 180, a capping pattern 300, a source/drain layer 210, first and second contact plugs 330 and 340, and first and second insulating interlayers 230 and 310.

[0020] The substrate 100 may include a semiconductor material, e.g., silicon, germanium, silicon-germanium, etc., or III-V semiconductor compounds, e.g., GaP, GaAs, GaSb, etc. In some embodiments, the substrate 100 may include a silicon-on-insulator (SOI) substrate or a germanium-on-insulator (GOI) substrate.

[0021] The active pattern 105 may have a fin-like shape protruding from an upper surface of the substrate 100, and thus may also be referred to as an active fin. A sidewall of the active pattern 105 may be at least partially covered by the isolation pattern 130. The active pattern 105 may extend in the first direction D1, and a plurality of active patterns 105 may be spaced apart from each other in the second direction D2. The active pattern 105 may include a material substantially the same as that of the substrate 100, and the isolation pattern 130 may include an oxide, e.g., silicon oxide.

[0022] The semiconductor patterns 124 may be formed at a plurality of levels, respectively, that are spaced apart from each other in the third direction D3, and each of the semiconductor patterns 124 may extend in the first direction D1 to a given length. FIGS. 2 and 3 show that the semiconductor patterns 124 are formed at three levels, respectively, however, embodiments of the inventive concept may not be limited thereto.

[0023] FIG. 2 shows that two columns of semiconductor patterns 124 that are spaced apart from each other at each level (i.e., level in the D3 direction) on the active pattern 105 extending in the first direction D1, however, embodiments of the inventive concept may not be limited thereto, and a plurality of semiconductor patterns 124 may be spaced apart from

each other at each level (i.e., level in the D3 direction) on the active pattern 105.

[0024] In example embodiments, the semiconductor pattern 124 may be a nano-sheet or nano-wire including a semiconductor material, e.g., silicon, germanium, etc. In example embodiments, the semiconductor pattern 124 may serve as a channel in a transistor, and thus may also be referred to as a channel.

[0025] In example embodiments, a second nitrogen-containing portion 122a may be formed at an upper portion and a lateral portion of the semiconductor pattern 124, and the second nitrogen-containing portion 122a may include silicon doped with nitrogen.

[0026] In particular, the second nitrogen-containing portion 122a may be formed at an upper portion and opposite lateral portions in the second direction D2 of an uppermost one of the semiconductor patterns 124, and may be formed at opposite lateral portions in the second direction D2 of other ones of the semiconductor patterns 124 under the uppermost one of the semiconductor patterns 124.

[0027] In example embodiments, the second nitrogen-containing portion 122a at the upper portion of the uppermost one of the semiconductor patterns 124 may be formed at an upper portion of a central portion in the second direction D2 of the uppermost one of the semiconductor patterns 124, and may protrude in the third direction D3 upwardly when compared to edge portions in the second direction D2 of the uppermost one of the semiconductor patterns 124.

[0028] The second oxide pattern 124b may be formed on the edge portions in the second direction D2 of the uppermost one of the semiconductor patterns 124, and may be spaced apart from the second nitrogen-containing portion 122a. In example embodiments, the second oxide pattern 124b may be formed at a level in the D3 direction substantially the same as that of the second nitrogen-containing portion 122a. Thus, lower and upper surfaces of the second oxide pattern 124b may be formed at respective levels in the D3

direction substantially the same as those of lower and upper surfaces of the second nitrogen-containing portion 122a.

[0029] In example embodiments, the second oxide pattern 124b may include silicon oxide.

[0030] The gate structure 290 may extend in the second direction D2 on the active pattern 105 and the isolation pattern 130, and may include a gate insulation pattern 260, a first conductive pattern 270, and a second conductive pattern 280. The first and second conductive patterns 270 and 280 may form a gate electrode.

[0031] In example embodiments, the gate structure 290 may border and at least partially surround a central portion in the first direction D1 of each of the semiconductor patterns 124, and may be on and at least partially cover lower and upper surfaces and opposite sidewalls in the second direction D2 of the central portion of each of the semiconductor patterns 124.

[0032] In example embodiments, the second nitrogen-containing portion 122a at the upper portion of the central portion of the uppermost one of the semiconductor patterns 124 may overlap the gate structure 290 in the third direction D3, and a width in the first direction D1 of the second nitrogen-containing portion 122a may be less than a width in the first direction D1 of the gate structure 290.

[0033] In example embodiments, the gate insulation pattern 260 and the first conductive pattern 270 may be stacked on a surface of each of the semiconductor patterns 124, an upper surface of the active pattern 105, an upper surface of the isolation pattern 130, a sidewall of the source/drain layer 210, an inner sidewall of the gate spacer 180 and an inner sidewall of the second oxide pattern 124b, and the second conductive pattern 280 may be in and at least partially fill a space between the semiconductor patterns 124 spaced apart from each other in the third direction D3, a space between the active pattern 105 and a lowermost one of the semiconductor patterns 124, and a space between the gate spacers 180 spaced

apart from each other in the first direction D1 on an uppermost one of the semiconductor patterns 124.

[0034] Hereinafter, a portion of the gate structure 290 on the uppermost one of the semiconductor patterns 124 in the D3 direction may be referred to as an upper portion of the gate structure 290, and other portions of the gate structure under the upper portion may be referred to as a lower portion of the gate structure 290.

[0035] The gate insulation pattern 260 may include an oxide, e.g., silicon oxide. Each of the first and second conductive patterns 270 and 280 may include a metal nitride, e.g., titanium nitride, titanium aluminum nitride, tantalum nitride, tantalum aluminum nitride, etc., a metal alloy, e.g., titanium aluminum, titanium aluminum carbide, titanium aluminum oxynitride, titanium aluminum carbonitride, titanium aluminum oxycarbonitride, etc., a metal carbide, a metal oxynitride, a metal carbonitride, a metal oxycarbonitride, and/or a low resistance metal, e.g., tungsten, aluminum, copper, tantalum. The first and second conductive patterns 270 and 280 may include substantially the same material as each other or different materials from each other.

[0036] The gate spacer 180 may be formed on each of opposite sidewalls in the first direction D1 of the gate structure 290.

[0037] In example embodiments, the gate spacer 180 may include a lower portion 180a having a relatively large width in the first direction D1 and an upper portion 180b having a relatively small width in the first direction D1. A sidewall of the lower portion 180a of the gate spacer 180 facing the gate structure 290 may be convex in the first direction D1, and a sidewall of the upper portion 180b of the gate spacer 180 facing the gate structure 290 may be substantially perpendicular to the upper surface of the substrate 100.

[0038] The second oxide pattern 124b may overlap the gate spacer 180 in the third direction D3. In example embodiments, an outer sidewall of the second oxide pattern

124b between the uppermost one of the semiconductor patterns 124 and the gate spacer 180 may be aligned with neither a sidewall of the uppermost one of the semiconductor patterns 124 nor an outer sidewall of the gate spacer 180, and may have a second recess 195 that is concave in the first direction D1.

[0039] In an example embodiment, the second oxide pattern 124b may not overlap the gate structure 290 in the third direction D3, however, embodiments of the inventive concept may not be limited thereto.

[0040] The capping pattern 300 may contact an upper surface of the gate structure 290 and the inner sidewall of the gate spacer 180.

[0041] Each of the gate spacer 180 and the capping pattern 300 may include an insulating nitride, e.g., silicon nitride.

[0042] The source/drain layer 210 may be formed on a portion of the active pattern 105 adjacent to the gate structure 290, and may commonly contact each of opposite sidewalls in the first direction D1 of the semiconductor patterns 124. In some embodiments, the source/drain layer 210 may contact the outer sidewall of the gate spacer 180.

[0043] In an example embodiment, the source/drain layer 210 may include single crystalline silicon-germanium doped with p-type impurities. Alternatively, the source/drain layer 210 may include single crystalline silicon doped with n-type impurities or single crystalline silicon carbide doped with n-type impurities.

[0044] In example embodiments, the source/drain layer 210 may contact the outer sidewall of the second oxide pattern 124b on each of opposite end portions in the first direction D1 of the uppermost one of the semiconductor patterns 124. The second oxide pattern 124b may include the second recess 195 on the outer sidewall thereof that may be concave from the sidewall of the uppermost one of the semiconductor patterns 124 and the outer sidewall of the gate spacer 180, and thus a portion of the source/drain layer 210 contacting the

second oxide pattern 124b may protrude in the first direction D1 toward the gate structure 290 from other portions thereof.

[0045] The first insulating interlayer 230 may be formed on the substrate 100, and may at least partially cover an upper surface of the source/drain layer 210 and the outer sidewall of the gate spacer 180. The second insulating interlayer 310 may be formed on the first insulating interlayer 230, the capping pattern 300, and the gate spacer 180.

[0046] Each of the first and second insulating interlayers 230 and 310 may include an insulating material, e.g., silicon oxycarbide, silicon oxide, silicon nitride, silicon oxynitride, silicon carbonitride, and/or silicon oxycarbonitride, etc.

[0047] The first contact plug 330 may extend through the first and second insulating interlayers 230 and 310 and an upper portion of the source/drain layer 210 to be electrically connected thereto. An ohmic contact pattern 320 may be formed between the first contact plug 330 and the source/drain layer 210.

[0048] The second contact plug 340 may extend through the second insulating interlayer 310 and the capping pattern 300, and may contact the second conductive pattern 280 included in the gate electrode.

[0049] Each of the first and second contact plugs 330 and 340 may include, e.g., a metal, a metal nitride, etc., the ohmic contact pattern 320 may include a metal silicide, e.g., cobalt silicide, nickel silicide, titanium silicide, etc.

[0050] Upper wirings may be formed on the first and second contact plugs 330 and 340 to apply electric signals thereto.

[0051] The semiconductor device may be a multi-bridge channel field effect transistor (MBCFET) including the semiconductor patterns 124 spaced apart from each other in the third direction D3 and serving as channels, respectively.

[0052] In the semiconductor device, the gate spacer 180 may be formed between the upper

portion of the gate structure 290 and the source/drain layer 210, and the second oxide pattern 124b between the uppermost one of the semiconductor patterns 124 and the gate spacer 180 may also be formed between the upper portion of the gate structure 290 and the source/drain layer 210. Thus, the upper portion of the gate structure 290 and the source/drain layer 210 may be electrically insulated from each other by the gate spacer 180 and the second oxide pattern 124b, and the risk of an electrical short between the gate structure 290 and the source/drain layer 210 may be reduced or prevented.

[0053] FIGS. 6 to 32 are plan views and cross-sectional views illustrating a method of manufacturing a semiconductor device in accordance with example embodiments. Particularly, FIGS. 6, 13, 20, 25 and 30 are the plan views, and FIGS. 7-12, 14-19, 21-24, 26-29 and 31-32 are the cross-sectional views.

[0054] FIGS. 7, 9, 11 and 14 are cross-sectional views taken along lines A-A' of corresponding plan views, respectively, FIGS. 8, 10, 12, 15-19, 21-22, 24, 26, 28-29 and 31-32 are cross-sectional views taken along lines B-B' of corresponding plan views, respectively, and FIG. 23 and 27 are cross-sectional views taken along line C-C' of corresponding plan views, respectively. FIGS. 17, 19, 22, 24, 29 and 32 are enlarged cross-sectional views of the region X of corresponding plan views, respectively.

[0055] Referring to FIGS. 6 to 8, a sacrificial layer and a semiconductor layer may be alternately and repeatedly stacked on a substrate 100, a first etching mask extending in the first direction D1 may be formed on an uppermost one of the semiconductor layers, and the semiconductor layers, the sacrificial layers and an upper portion of the substrate 100 may be etched using the first etching mask.

[0056] Thus, an active pattern 105 extending in the first direction D1 may be formed on the substrate 100, and a fin structure including sacrificial lines 112 and semiconductor lines 122 alternately and repeatedly stacked in the third direction D3 may be formed on the active

pattern 105. In example embodiments, the fin structure may extend in the first direction D1 on the substrate 100, and a plurality of fin structures may be spaced apart from each other in the second direction D2 on the substrate 100.

[0057] FIG. 7 shows three sacrificial lines 112 and three semiconductor lines 122 at three levels in the D3 direction, respectively, however, embodiments of the inventive concept may not be limited thereto. The sacrificial lines 112 may include a material having an etching selectivity with respect to the substrate 100 and the semiconductor lines 122, e.g., silicon-germanium.

[0058] An isolation pattern 130 may be formed on the substrate 100 to at least partially cover a sidewall of the active pattern 105.

[0059] Referring to FIGS. 9 and 10, a dummy gate insulation layer 140 may be formed on the substrate 100 to at least partially cover the fin structure and the isolation pattern 130.

[0060] The dummy gate insulation layer 140 may include an oxide, e.g., silicon oxide.

[0061] Referring to FIGS. 11 and 12, a nitridation process, e.g., a plasma nitridation process may be performed on the dummy gate insulation layer 140.

[0062] Thus, the dummy gate insulation layer 140 may be converted into a sacrificial gate insulation layer 145 include an insulating nitride, e.g., silicon oxynitride.

[0063] During the nitridation process, nitrogen may permeate into and remain at an upper surface and a sidewall of the semiconductor line 122 and a sidewall of the sacrificial line 112. Thus, a second nitrogen-containing portion 122a including silicon doped with nitrogen may be formed at the upper surface and the sidewall in the second direction D2 of the semiconductor line 122, and a first nitrogen-containing portion 112a including silicon-germanium doped with nitrogen may be formed at the sidewall in the second direction D2 of the sacrificial line 112.

[0064] Referring to FIGS. 13 to 15, a dummy gate electrode layer and a dummy gate mask

layer may be sequentially formed on the sacrificial gate insulation layer 145, a second etching mask extending in the second direction D2 may be formed on the dummy gate mask layer, and the dummy gate mask layer may be etched using the second etching mask to form a dummy gate mask 160.

[0065] The dummy gate electrode layer and the sacrificial gate insulation layer 145 may be etched using the dummy gate mask 160 as an etching mask to form a dummy gate electrode 150 and a sacrificial gate insulation pattern 147, respectively, on the substrate 100.

[0066] The sacrificial gate insulation pattern 47, the dummy gate electrode 150 and the dummy gate mask 160 sequentially stacked in the third direction D3 on the active pattern 105 and a portion of the isolation pattern 130 adjacent thereto may form a dummy gate structure 170. In example embodiments, the dummy gate structure 170 may extend in the second direction D2 on the fin structure and the isolation pattern 130, and may be on and at least partially cover an upper surface and opposite sidewalls in the second direction D2 of the fin structure.

[0067] Referring to FIGS. 16 and 17A, a portion of the sacrificial gate insulation pattern 147 under an edge portion of the dummy gate electrode 150 may be removed by an etching process to form a first recess 149 on a sidewall of the sacrificial gate insulation pattern 147 under the dummy gate electrode 150.

[0068] The sacrificial gate insulation pattern 147 may include, e.g., silicon oxynitride, and thus an etch rate of the sacrificial gate insulation pattern 146 may be relatively low when compared to a layer including, e.g., silicon oxide. Thus, an amount of a portion of the sacrificial gate insulation pattern 147 removed during the etching process may be relatively easily controlled.

[0069] In example embodiments, during the etching process, lower and upper portions of the sacrificial gate insulation pattern 147 may be etched by substantially the same amount,

and thus the sacrificial gate insulation pattern 147 remaining after the etching process may be generally symmetric in the third direction D3 with reference to an imaginary plane passing a central portion in the third direction D3 of the sacrificial gate insulation pattern 147. Additionally, the sacrificial gate insulation pattern 147 after the etching process may not protrude toward an outside of the dummy gate electrode 150 in a plan view, and may be formed only in an area of the dummy gate electrode 150 in a plan view.

[0070] Referring to FIG. 17B, if the nitridation process illustrated with reference to FIGS. 11 and 12 is not performed, a dummy gate insulation pattern 142 that may be formed by patterning the dummy gate insulation layer 140 may include silicon oxide. Thus, during the etching process, an etch rate of the dummy gate insulation pattern 142 may be high so that an amount of a portion of the dummy gate insulation pattern 142 removed during the etching process may be difficult to control.

[0071] Accordingly, during the etching process, lower and upper portions of the dummy gate insulation pattern 142 may not be etched by the same amount, and for example, the lower portion may be etched less than the upper portion so that the dummy gate insulation pattern 142 remaining after the etching process may not be symmetric in the third direction D3. Additionally, the dummy gate insulation pattern 142 after the etching process may protrude toward the outside of the dummy gate electrode 150 to be formed at the outside of the dummy gate electrode 150 in a plan view.

[0072] Referring to FIGS. 18 and 19, a curing process may be performed on surfaces of the fin structure and the dummy gate structure 170, which may be damaged during the etching process for forming the dummy gate structure 170.

[0073] In example embodiments, the curing process may be performed using, e.g., HF and SC1 solution, and the surfaces of the fin structure and the dummy gate structure 170 may be oxidized by oxygen included in the SC1 solution.

[0074] Thus, a portion of the second nitrogen-containing portion 122a at the upper surface and the sidewall of the semiconductor line 122, which may include silicon doped with nitrogen, particularly, a portion of the second nitrogen-containing portion 122a not covered by the sacrificial gate insulation pattern 147 may be converted into a second oxide layer 122b including silicon oxynitride. Additionally, a portion of the first nitrogen-containing portion 112a at the sidewall of the sacrificial line 112, which may include silicon-germanium doped with nitrogen, may be converted into a first oxide layer (not shown).

[0075] A third oxide layer 150a may be formed at a sidewall of the dummy gate electrode 150 including, e.g., polysilicon may be formed to include silicon oxide, a fourth oxide layer 160a may be formed at an upper surface, and a sidewall of the dummy gate mask 160 may be formed to include silicon oxynitride.

[0076] However, an additional oxide layer may not be formed on a sidewall of the sacrificial gate insulation pattern 147 including silicon oxynitride, and a volume of the sacrificial gate insulation pattern 147 may slightly increase. Thus, a portion of the second oxide layer 122b that may be formed by the curing process may partially contact an edge portion of the sacrificial gate insulation pattern 147.

[0077] Referring to FIGS. 20 to 23, a gate spacer 180 may be formed on the sidewall of the dummy gate structure 170.

[0078] Particularly, a spacer layer may be formed on the substrate 100 having the fin structure, the isolation pattern 130 and the dummy gate structure 170 and may not be anisotropically etched to form the gate spacer 180 on each of opposite sidewalls in the first direction D1 of the dummy gate structure 170.

[0079] During the anisotropic etching process, a portion of the fourth oxide layer 160a on the upper surface of the dummy gate mask 160 may be removed.

[0080] The fin structure and an upper portion of the active pattern may be etched using the dummy gate structure 170 and the gate spacer 180 as an etching mask to form a first opening 190.

[0081] Thus, the sacrificial lines 112 and the semiconductor lines 122 under the dummy gate structure 170 and the gate spacers 180 may be transformed into sacrificial patterns 114 and semiconductor patterns 124, respectively, and the fin structure extending in the first direction D1 may be divided into a plurality of parts spaced apart from each other in the first direction D1.

[0082] During the etching process, the first oxide layer and the second oxide layer 122b may also be partially etched to form a first oxide pattern (not shown) and a second oxide pattern 124b.

[0083] Hereinafter, the dummy gate structure 170, the gate spacer 180 on each of opposite sidewalls of the dummy gate structure 170 and the fin structure may be referred to as a stack structure. In example embodiments, the stack structure may extend in the second direction D2, and a plurality of stack structures may be spaced apart from each other in the first direction D1.

[0084] Referring to FIG. 24, a cleansing process may be performed on the substrate 100 having the stack structure thereon.

[0085] By the cleansing process, a lateral portion of the second oxide pattern 124b exposed by the first opening 190 may be removed to form a second recess 195.

[0086] As illustrated above, the second oxide pattern 124b may include, e.g., silicon oxynitride, and thus the amount of the portion of the second oxide pattern 124b removed during the cleansing process may be relatively small when compared to a layer including, e.g., silicon oxide. Thus, the second recess 195 on the outer sidewall of the second oxide pattern 124b may be formed only in an area of the gate spacer 180 in a plan view, and may

not overlap the dummy gate structure 170 in the third direction D3.

[0087] Referring to FIGS. 25 to 27, a selective epitaxial growth (SEG) process may be performed using the upper surface of the active pattern 105 and the sidewalls of the semiconductor patterns 124 and the sacrificial patterns 114 exposed by the first openings 190 as a seed to a source/drain layer 210 in the first opening 190.

[0088] In an example embodiment, the SEG process may be performed using a silicon source gas, e.g., dichlorosilane (SiH_2Cl_2) gas, a germanium source gas, e.g., germane (GeH_4) gas, and thus a single crystalline silicon-germanium layer may be formed as the second source/drain layer 210. A p-type impurity source gas, e.g., diborane (B_2H_6) gas may also be used so that a single crystalline silicon-germanium layer doped with p-type impurities may be formed as the second source/drain layer 210.

[0089] In another example embodiment, the SEG process may be performed using a silicon source gas, e.g., disilane (Si_2H_6) gas and a carbon source gas, e.g., SiH_3CH_3, and thus a single crystalline silicon carbide layer may be formed as the first source/drain layer 210. An n-type impurity source gas, e.g., PH_3, $POCl_3$, P_2O_5, etc., may also be used so that a single crystalline silicon carbide layer doped with n-type impurities may be formed as the first source/drain layer 210. In other embodiments, the SEG process may be performed using the silicon source gas and the impurity source gas so that a single crystalline silicon layer doped with n-type impurities may be formed as the first source/drain layer 210.

[0090] A first insulating interlayer 230 may be formed on the substrate 100 to be on and at least partially cover the stack structure and the source/drain layer 210.

[0091] Referring to FIGS. 28 and 29, a planarization process may be performed until an upper surface of the dummy gate electrode 150 included in the stack structure is exposed so that an upper portion of the first insulating interlayer 230 and the dummy gate mask 160 included in the dummy gate structure 170 may be removed. During the planarization

process, the fourth oxide layer 160a on the sidewall of the dummy gate mask 160 may also be removed.

[0092] The dummy gate electrode 150, the sacrificial gate insulation pattern 147 and the sacrificial patterns 114 may be removed by, e.g., by using a wet etching process and/or a dry etching process, and the third oxide layer 150a on the sidewall of the dummy gate electrode 150 and a portion of the second oxide pattern 124b contacting the sacrificial gate insulation pattern 147 may also be removed.

[0093] However, in example embodiments, the second oxide pattern 124b may not be entirely removed, and for example, a portion of the second oxide pattern 124b not overlapping the dummy gate electrode 150 in the third direction D3 may remain.

[0094] Thus, a second opening 240 exposing an inner sidewall of the gate spacer 180 and an upper surface of an uppermost one of the semiconductor patterns 124, and a third opening 250 exposing a sidewall of the third source/drain layer 210, surfaces of the semiconductor patterns 124, and an upper surface of the active pattern 105 may be formed. Additionally, a surface of the second nitrogen-containing portion 122a at the upper surface and the sidewall of the semiconductor pattern 124 and a sidewall of the second oxide pattern 124b may be exposed by the second opening 240.

[0095] Referring to FIGS. 30 to 32, a gate insulation layer and a first conductive layer may be sequentially stacked on the inner sidewall of the gate spacer 180, the surfaces of the semiconductor patterns 124, the sidewall of the second oxide pattern 124b, the upper surface of the active pattern 105, the upper surface of the isolation pattern 130, and the sidewall of the source/drain layer 120 exposed by the second and third openings 240 and 250. An upper surface of the first insulating interlayer 230 and a second conductive layer may be formed on the first conductive layer to at least partially fill remaining portions of the second and third openings 240 and 250.

[0096] In an example embodiment, an interface pattern including, e.g., silicon oxide may be further formed on the upper surface of the active pattern 105 and the surfaces of the semiconductor patterns 124.

[0097] The first and second conductive layers and the gate insulation layer may be planarized until the upper surface of the first insulating interlayer is exposed. Thus, a gate structure 290 at least partially filling the second and third openings 240 and 250 and including a gate insulation pattern 260, a first conductive pattern 270, and a second conductive pattern 280 may be formed. The first and second conductive patterns 270 and 280 may form a gate electrode.

[0098] Referring to FIGS. 1 to 5, an upper portion of the gate structure 290 may be removed to form a third recess, and a capping pattern 300 may be formed in the third recess.

[0099] A second insulating interlayer 310 may be formed on the capping pattern 300, the gate spacer 180, and the first insulating interlayer 230. A first contact plug 330 extending through the first and second insulating interlayers 230 and 310 and an upper portion of the source/drain layer 210 and a second contact plug 340 extending through the second insulating interlayer 310 and the capping pattern 300 to contact an upper surface of the second conductive pattern 280 may be formed.

[00100] In an example embodiment, an ohmic contact pattern 320 may be further formed between the first contact plug 330 and the source/drain layer 210.

[00101] Upper wirings may be further formed on the first and second contact plugs 330 and 340 to complete the fabrication of the semiconductor device.

[00102] As illustrated above, after forming the dummy gate insulation layer 140 including, e.g., silicon oxide on the fin structure including the sacrificial line 112 and the semiconductor line 122 alternately stacked on the active pattern 105, a nitridation process may be performed on the dummy gate insulation layer 140 to form the sacrificial gate

insulation layer 145 including, e.g., silicon oxynitride, and the second nitrogen-containing portion 122a including silicon doped with nitrogen may be formed at the upper portion of the semiconductor line 122.

[00103] During the formation of the dummy gate structure 170, the sacrificial gate insulation layer 145 may be patterned to form the sacrificial gate insulation pattern 147, and the lateral portion of the sacrificial gate insulation pattern 147 may be further etched by an additional etching process to form the first recess 149. The sacrificial gate insulation layer 145 may include, e.g., silicon oxynitride instead of silicon oxide, and thus the etch rate of the sacrificial gate insulation pattern 147 may be relatively low during the additional etching process, so that the amount of the portion of the sacrificial gate insulation pattern 147 removed by the additional etching process may be relatively easily controlled, and that the sacrificial gate insulation pattern 147 may be formed only in the area of the dummy gate electrode 150 in a plan view.

[00104] The curing process may be performed on the fin structure and the dummy gate structure 170 using, e.g., HF and SC1 solution, and the portion of the second nitrogen-containing portion 122a not covered by the sacrificial gate insulation pattern 147 may be converted by oxygen included in the SC1 solution into the second oxide layer 122b including silicon oxynitride, while the volume of the sacrificial gate insulation pattern 147 including oxygen may barely increase.

[00105] After forming the gate spacer 180 on the sidewall of the dummy gate structure 170, the fin structure and the upper portion of the active pattern 105 may be etched by an etching process using the dummy gate structure 170 and the gate spacer 180 as an etching mask to form the first opening 190, and the sacrificial line 112 and the semiconductor line 122 may be transformed into the sacrificial pattern 114 and the semiconductor pattern 124, respectively, and the second oxide layer 122b may be transformed into the second oxide

pattern 124b.

[00106] During the cleansing process, the second oxide pattern 124b exposed by the first opening 190 may be partially removed, however, only a small amount of the second oxide pattern 124b may be removed when compared to a layer including silicon oxide.

[00107] After forming the source/drain layer 210 in the first opening 190, when the dummy gate structure 170 and the sacrificial pattern 114 are removed to form the second and third openings 240 and 250, the second oxide pattern 124b adjacent to the sacrificial gate insulation pattern 147 may also be partially removed, but may not be entirely removed.

[00108] Thus, when the gate structure 290 is formed in the second and third openings 240 and 250, not only the gate spacer 180 but also the second oxide pattern 124b may be formed between a portion of the gate structure 290 in the second opening 240, that is, the upper portion of the gate structure 290 on the uppermost one of the semiconductor patterns 124 and the source/drain layer 210, so that the risk of an electrical short between the gate structure 290 and the source/drain layer 210 may be reduced or prevented.

[00109] FIG. 33 is a cross-sectional view illustrating a semiconductor device in accordance with example embodiments, and may correspond to FIG. 4.

[00110] This semiconductor device may be substantially the same as or similar to that of FIGS. 1 to 5, except for the second oxide pattern 124b and the gate insulation pattern 260, and thus repeated explanations thereof are omitted herein.

[00111] Referring to FIG. 33, the second oxide pattern 124b may not be spaced apart from but may contact the second nitrogen-containing portion 122a.

[00112] Thus, the gate insulation pattern 260 may not be interposed between the second oxide pattern 124b and the second nitrogen-containing portion 122a, and may not contact a sidewall of the second nitrogen-containing portion 122a and an inner sidewall of the second oxide pattern 124b.

[00113] In an example embodiment, a portion of the second oxide pattern 124b may overlap the gate structure 290 in the third direction D3.

[00114] FIG. 34 is a cross-sectional view illustrating a method of manufacturing a semiconductor device in accordance with example embodiments, and may correspond to FIG. 19.

[00115] This method may include processes substantially the same as or similar to those illustrated with reference to FIGS. 6 to 32 and FIGS. 1 to 5, and thus repeated explanations thereof are omitted herein.

[00116] Referring to FIG. 34, processes substantially the same as or similar to those illustrated with reference to FIGS. 1 to 19 may be performed.

[00117] However, after the curing process, the second oxide layer 122b on each of opposite end portions of the uppermost one of the semiconductor patterns 124 may not contact an edge portion of the sacrificial gate insulation pattern 147.

[00118] Processes substantially the same as or similar to those illustrated with reference to FIGS. 20 to 29 may be performed, however. During the formation of the second opening 240, the second oxide pattern 124b may not contact the sacrificial gate insulation pattern 147, and thus no portion of the second oxide pattern 124b may be removed.

[00119] Processes substantially the same as or similar to those illustrated with reference to FIGS. 30 to 32 and FIGS. 1 to 5 may be performed to complete the fabrication of the semiconductor device.

[00120] FIG. 35 is a cross-sectional view illustrating a semiconductor device in accordance with example embodiments, and may correspond to FIG. 4.

[00121] This semiconductor device may be substantially the same as or similar to that of FIGS. 1 to 5, except for the second nitrogen-containing portion 122a, the second oxide pattern 124b, and the gate insulation pattern 260, and thus repeated explanations thereof are

omitted herein.

[00122] Referring to FIG. 35, the second nitrogen-containing portion 122a at the upper portion of the uppermost one of the semiconductor patterns 124 may be formed not only at the central portion in the first direction D1 but also at the edge portions in the first direction D1, and thus the second oxide pattern 124b may not be formed.

[00123] The second nitrogen-containing portion 122a may include silicon doped with nitrogen, and thus may not be removed during the cleansing process or the formation of the second and third openings 240 and 250 for forming the gate structure 290. Accordingly, the electrical insulation between the gate structure 290 and the source/drain layer 210 may be acquired.

[00124] FIGS. 36 and 37 are cross-sectional views illustrating a method of manufacturing a semiconductor device in accordance with example embodiments, and may correspond to FIGS. 24 and 29, respectively.

[00125] This method may include processes substantially the same as or similar to those illustrated with reference to FIGS. 6 to 32 and FIGS. 1 to 5, and thus repeated explanations thereof are omitted herein.

[00126] Processes substantially the same as or similar to those illustrated with reference to FIGS. 1 to 17 may be performed.

[00127] The curing process illustrated with reference to FIGS. 18 and 19 may not be performed. Thus, the end portions of the second nitrogen-containing portion 122a at the upper portion of the uppermost one of the semiconductor patterns 124 may not be converted into the second oxide layer 122b.

[00128] Referring to FIG. 36, processes substantially the same as or similar to those illustrated with reference to FIGS. 20 to 24 may be performed.

[00129] However, instead of the second oxide pattern 124b including, e.g., silicon

oxynitride, the second nitrogen-containing portion 122a including silicon doped with nitrogen may be formed at the end portions of the uppermost one of the semiconductor patterns 124, so that the second recess 195 may not be formed when the cleansing process is performed.

[00130] Referring to FIG. 37, processes substantially the same as or similar to those illustrated with reference to FIGS. 25 to 29 may be performed.

[00131] However, the second nitrogen-containing portion 122a contacting the sacrificial gate insulation pattern 147 may include silicon doped with nitrogen so as not to be removed when the sacrificial gate insulation pattern 147 is removed to form the second opening 240.

[00132] Referring to FIG. 35, processes substantially the same as or similar to those illustrated with reference to FIGS. 30 to 32 and FIGS. 1 to 5 may be performed to complete the fabrication of the semiconductor device.

[00133] FIGS. 38 and 39 are cross-sectional views illustrating semiconductor devices in accordance with example embodiments, and may correspond to FIG. 3.

[00134] These semiconductor devices may be substantially the same as or similar to that of FIGS. 1 to 5, except for the shape of the source/drain layer 210 or further including an inner spacer, and thus repeated explanations thereof are omitted herein.

[00135] Referring to FIG. 38, a sidewall in the first direction D1 of the source/drain layer 210 may not be substantially perpendicular to the upper surface of the substrate 100, but may have varying slopes with respect to the upper surface of the substrate 100.

[00136] The sidewall of the source/drain layer 210 may have a width in the first direction D1 that may change in the third direction D3. In some embodiments, the width may periodically change in the third direction D3. Thus, the sidewall of the source/drain layer 210 may have concave portions and convex portions in the first direction D1 that may be alternately and repeatedly stacked in the third direction D3. In example embodiments, a

width of the source/drain layer 210 facing the semiconductor pattern 124 may be less than a width of the source/drain layer 210 facing the lower portion of the gate structure 290.

[00137] Referring to FIG. 39, an inner spacer 350 may be formed between the source/drain layer 210 and the lower portion of the gate structure 290.

[00138] In an example embodiment, the inner spacer 350 may have a convex shape toward the gate structure 290. The inner spacer 350 may include an insulating nitride, e.g., silicon nitride.

[00139] The foregoing is illustrative of example embodiments and is not to be construed as limiting thereof. Although a few example embodiments have been described, those skilled in the art will readily appreciate that many modifications are possible in the example embodiments without materially departing from the novel teachings and advantages of the present inventive concept. Accordingly, all such modifications are intended to be included within the scope of the present inventive concept as defined in the claims. In the claims, means-plus-function clauses are intended to cover the structures described herein as performing the recited function and not only structural equivalents but also equivalent structures. Therefore, it is to be understood that the foregoing is illustrative of various example embodiments and is not to be construed as limited to the specific example embodiments disclosed, and that modifications to the disclosed example embodiments, as well as other example embodiments, are intended to be included within the scope of the appended claims.

What is claimed is:

1. A semiconductor device, comprising:

channels spaced apart from each other on a substrate in a vertical direction substantially perpendicular to an upper surface of the substrate;

a gate structure on the substrate, the gate structure bordering lower and upper surfaces and a first sidewall of at least a portion of each of the channels; and

a source/drain layer on a portion of the substrate adjacent to the gate structure, the source/drain layer contacting second sidewalls of the channels,

wherein a nitrogen-containing portion is formed at an upper portion of an uppermost one of the channels, the nitrogen-containing portion being doped with nitrogen.

2. The semiconductor device as claimed in claim 1, wherein the nitrogen-containing portion protrudes from other portions of the uppermost one of the channels in the vertical direction.

3. The semiconductor device as claimed in claim 1 or claim 2, wherein each of the channels extends in a first direction substantially parallel to the upper surface of the substrate, and

wherein the nitrogen-containing portion is formed at an upper portion of a central portion in the first direction of the uppermost one of the channels.

4. The semiconductor device as claimed in claim 3, further comprising an oxide pattern on an upper surface of each of opposite end portions in the first direction of the uppermost one of the channels, the oxide pattern including silicon oxynitride.

5. The semiconductor device as claimed in claim 4, wherein the oxide pattern is formed at substantially a same level in the vertical direction as that of the nitrogen-containing portion.

6. The semiconductor device as claimed in claim 4, wherein a portion of the gate structure is interposed between the nitrogen-containing portion and the oxide pattern.

7. The semiconductor device as claimed in claim 4, wherein the nitrogen-containing portion and the oxide pattern contact each other.

8. A semiconductor device, comprising:

channels spaced apart from each other on a substrate in a vertical direction substantially perpendicular to an upper surface of the substrate;

a gate structure on the substrate, the gate structure bordering lower and upper surfaces and a first sidewall of at least a portion of each of the channels;

a source/drain layer on a portion of the substrate adjacent to the gate structure, the source/drain layer contacting second sidewalls of the channels; and

an oxide pattern on an upper surface of an end portion of an uppermost one of the channels, the oxide pattern including silicon oxynitride.

9. The semiconductor device as claimed in claim 8, further comprising a gate spacer on an upper sidewall of the gate structure,

wherein the oxide pattern is interposed between the uppermost one of the channels and the gate spacer.

10. A semiconductor device, comprising:

an active pattern on a substrate;

channels spaced apart from each other on the active pattern in a vertical direction substantially perpendicular to an upper surface of the substrate;

a gate structure on the substrate, the gate structure bordering lower and upper surfaces and a first sidewall of at least a portion of each of the channels;

a source/drain layer on a portion of the substrate adjacent to the gate structure, the source/drain layer contacting second sidewalls of the channels;

a gate spacer on an upper sidewall of the gate structure;

a nitrogen-containing portion at an upper portion of an uppermost one of the channels; and

an oxide pattern between an upper surface of each of opposite end portions of the uppermost one of the channels and a lower surface of the gate spacer.