HYPER THERMALLY ENHANCED SEMICONDUCTOR PACKAGE SYSTEM COMPRISING HEAT SLUGS ON OPPOSITE SURFACES OF A SEMICONDUCTOR CHIP

TECHNICAL FIELD

The present invention relates generally to semiconductor package systems, and more particularly to thermally enhanced semiconductor package systems.

BACKGROUND ART

The increasing density of electrical connections in semiconductor devices has pushed conventional packages to their design limit. Heat generated by the semiconductor devices needs to be dissipated immediately to prevent them from overheating. As the semiconductor devices become denser, the generated heat also increases correspondingly. More and more packages are now designed with heat sinks or heat slugs to enhance the ability to dissipate heat.

With smaller package footprint, ball grid array (BGA) packages have been introduced and developed several years ago. BGA includes a family of package 'styles', differentiated primarily by construction materials and techniques, such as plastic (PBGA) or ceramic (CBGA). Other BGA packages include tape automated bonding ball grid array (TAB-BGA) and cavity down (CD-BGA) type of construction.

Higher device working frequency (3.3MHz and above) with increased clock speed rates have required the creation of other versions of BGA: enhanced BGA (EBGA), thermally enhanced BGA (TEBGA I & II), heat spreader BGA (HS-BGA), and micro super BGA (mBGA or m Super-BGA). However, all BGA packages, regardless of package style, utilize solder attachments (balls) located directly underneath the package body. Thus, during reflow, a significant portion of the heat energy required to melt these connections must be conducted through the package body itself. Consequently, the materials and their relative locations within the package can influence the thermal profile of the package.

A BGA package typically includes a substrate, such as printed circuit board, made from reinforced polymer laminate material, i.e. bismaleimide triazine (BT) or a polyimide

resin with series of metal traces on the top side. The metal traces are connected by vias to the bottom side of the substrate, and redistributed in an array grid around the periphery of the

The semiconductor chip 106 is flipped-over for chip-attach using flip-chip bonding to a substrate 116.

The substrate 116 is a multi-layer substrate having a substrate opening 128 and a recessed cavity 119. The substrate opening 128 and the recessed cavity 119 reduce the total package weight and enhance substrate structural flexibility. The substrate is generally a reinforced polymer laminate material, such as organic bismaleimide triazine (BT), or a polymide resin, containing through vias for connecting top and bottom conductive traces.

Solder pillars/ball bumps 110 are formed connected to the top traces and in a solder mask 118, which is pre-plated on non-contact areas of the substrate 116. The substrate 116 also includes vertical build-up wings 124. The vertical build-up wings 124 are designed to control the solder mask structure and solder joint sustainability during chip mount reflow as well as to enhance internal package structural robustness during the second re-flow after ball mounting.

The stud bumps 114 are mounted on the solder pillars/ball bumps 110 and then heat reflow forms interconnections of the semiconductor chip 106 to the substrate 116. The substrate 116 includes the vertical build-up wings 124 circumscribed by vertical planes of a perimeter of, and spaced apart from, the semiconductor chip 106. During reflow, the solder pillars/ball bumps 110 self-realign to the exact location of the bond pads 111 and the solder mask 118 strengthens the solder pillars/ball bumps 110 after heat reflow.

Once the semiconductor chip 106 is mounted, an adhesive 120 including a non-brittle interconnect material, such as soft solder paste or epoxy, is applied to the formerly bottom surface of the semiconductor chip 106 which is facing upward after chip-attach. The adhesive 120 can be conductive to enhance heat conduction between the semiconductor chip 106 and the top heat slug 102. The cap flash 108 of the top heat slug 102 is coated with a non-conductive adhesive (NCA) 122 or a non-conductive elastomer (NCE) to enhance sealing.

Then, the top heat slug 102 is placed, using a pattern recognition system, ~~on~~above the substrate 116 to be attached thereto by the NCA 122 . The cap flash 108 of the top heat slug 102 serves as a platform for sealing against the substrate 116. Heat from about 175°C. and 180°C. is applied in-line during the sealing process to cure the adhesive 120. The semiconductor chip 106 may be hermetically sealed to the substrate 116 using a vacuum applied through the substrate opening 128.

A further sealant or heat conductive epoxy 129 can be injected through the substrate opening 128 to also help provide a hermetic seal around the semiconductor chip 106.

The substrate opening 128 is then used to enable the bottom heat slug 104 to penetrate through the substrate 116 and directly make contact with the semiconductor chip 106 for enhanced heat conduction. Because most of the active circuit layers are in the top of the semiconductor chip 106 adjacent the bond pads 111, there is a need to have a faster heat dissipation path on the top to channel out all heat generated to the package ambient. The bottom heat slug 104 performs this function by under hanging the substrate 116 in the recessed cavity 119 to provide additional heat convention surface area for the HTEBGA package 100. The bottom heat slug 104 is connected to the substrate 116 at a horizontal plane 125 of the substrate 116 at or above a horizontal plane 127 of the substrate 116, which connects to the top heat slug 102.

The under hang feature includes: the thickness of the bottom heat slug 104 exceeding the thickness of the substrate 116, the bottom heat slug 104 protruding from the substrate 116 during flip-over and after mounting. The protrusion of the bottom heat slug 104 is, however, less than the standoff height required after solder balls attachment with a minimum clearance of 1.25mm reserved. The bottom heat slug 104 is engaged with the substrate 116.

The size of the bottom heat slug 104 is almost equal to the size of the opening of the substrate opening 128 in the substrate 116. The bottom heat slug 104 is attached to the bottom surface of the semiconductor chip 106 by the conductive adhesive 123 and to the substrate 116 by the NCA 122. The bottom surface of the semiconductor chip 106 may include a phosphosilicate glass (PSG) or SiN polyimide capping layer 121 around the stud bumps 114. The bottom heat slug 104 passes through the substrate opening 128 of the substrate 116, using a package flip-over and drop-in method. Connection of the bottom heat slug 104 is achieved using a conductive adhesive 123.

Once connection of the bottom heat slug 104 is made, solder balls 112 are prepared at a blank substrate-mounting template having an exact imprint of the bottom surface of the substrate 116 including metal connector pads 126, which are connected to the bond pads 111 on the semiconductor chip 106. The enclosed package (with the top heat slug 102 and the bottom heat slug 104) is then picked up to be flip-over again, using a pattern recognition system to align the edges of the substrate 116 to the substrate-mounting template edge which contains the solder balls 112 in a pre-determined pattern. Mounting is achieved once the placement is done and subjected to package reflow. The embodiment of the present invention is ready for testing and branding.

Referring now to FIG. 2, therein is shown a schematic diagram of a cross-sectional view of a hyper thermally enhanced ball grid array (HTEBGA) package 200 in accordance with a second embodiment of the present invention. A top heat slug 202 and a bottom heat

slug 204 encapsulate and protect the semiconductor chip 106 mounted inside the HTEBGA package 200. The top heat slug 202 is above the substrate 116. The HTEBGA package 200 includes similar elements from the HTEBGA package 100 of FIG. 1.

The top heat slug 202 has a top recess 206 or a reduced top surface thickness, or thinner by 3/5 of the total heat slug thickness, in the form of round or rectangular indentation in the center of the top heat slug 202. The bottom heat slug 204 also has a bottom recess 208, or a reduced surface thickness in the form of a round or rectangular indentation in the center of the bottom heat slug 204. Such embodiment further enhances heat dissipation capability due to larger effective heat dissipation area as well as reducing vertical thermal mismatch loading.

Referring now to FIG. 3, therein is shown a schematic diagram of a cross-sectional view of a hyper thermally enhanced ball grid array (HTEBGA) package 300 in accordance with a third embodiment of the present invention.

A top heat slug 302 and a bottom heat slug 304 encapsulate and protect the semiconductor chip 106 mounted inside the HTEBGA package 300. The top heat slug 302 is above the substrate 116. The HTEBGA package 300 includes similar elements from the HTEBGA package 100 of FIG. 1.

The top heat slug 302 and the bottom heat slug 304 include heat-spreader fins 306 and 308, respectively. The heat-spreader fins 306 and 308 are built-in vertically and appear from the respective top and bottom surfaces of the top heat slug 302 and the bottom heat slug 304 (after mounting) to the inner part of the top heat slug 302 and the bottom heat slug 304 with 3/5 depth of fin length. Such design further enlarges the total effective area for heat dissipation as well as promotes air circulation for faster cooling effect.

Referring now to FIG. 4, therein is shown a schematic diagram of a bottom view of a hyper thermally enhanced ball grid array package in accordance with a first embodiment of the present invention corresponding to FIG. 1. The bottom heat slug 104 is located in the center the substrate 116. The solder balls 112 are shown around the bottom heat slug 104.

Referring now to FIG. 5, therein is shown a schematic diagram of a bottom view of a hyper thermally enhanced ball grid array package in accordance with a second embodiment of the present invention. The bottom heat slug 204 is located in the center the substrate 116. The bottom heat slug 204 includes the bottom recess 208 in its the center. The solder balls 112 are shown around the bottom heat slug 104.

THE INVENTION CLAIMED IS:

1. A semiconductor package ~~system~~method comprising:

mounting a semiconductor chip to a substrate having a substrate opening and a vertical build-up wing, and the vertical build-up wing is circumscribed by vertical planes of a perimeter of, and spaced apart from, the semiconductor chip;

attaching a first heat slug to the substrate at a first horizontal plane and to a first surface of the semiconductor chip, the first heat slug at least partially encapsulating the semiconductor chip; and

attaching a second heat slug ~~to~~ above the substrate at a second horizontal plane above the first horizontal plane and to a second surface of the semiconductor chip through the substrate opening.

2. The ~~system~~method as claimed in claim 1 wherein:

mounting the semiconductor chip further comprises reflow soldering stud bumps on the semiconductor chip to solder pillars/ball bumps on the substrate.

3. The ~~system~~method as claimed in claim 1 further comprising:

hermetically sealing the first heat slug to the substrate using a vacuum.

4. The ~~system~~method as claimed in claim 1 wherein:

attaching the first heat slug further comprises providing the first heat slug with a top recess on a top surface thereof; or

attaching the second heat slug further comprises providing the second heat slug with a bottom recess on a bottom surface thereof.

5. The ~~system~~method as claimed in claim 1 wherein:

attaching the first heat slug further comprises providing the first heat slug with a first fin on a top surface thereof; or

attaching the second heat slug further comprises providing the first heat slug with a second fin on a bottom surface thereof.

6. A semiconductor package ~~system~~method comprising:

mounting a semiconductor chip by flipping and electrically connecting former top bonding pads to a substrate having a substrate opening and a vertical build-up wing, and the vertical build-up wing is circumscribed by vertical planes of a perimeter of, and spaced apart from, the semiconductor chip;

attaching a top heat slug above the substrate at a first horizontal plane and to a first surface of the semiconductor chip using a conductive bond, the top heat slug at least partially encapsulating the semiconductor chip; and

attaching a bottom heat slug to the substrate at a second horizontal plane above the first horizontal plane and using a conductive bond to a second surface of the semiconductor chip through the substrate opening.

7. The ~~system~~method as claimed in claim 6 wherein:

mounting the semiconductor chip further comprises reflow soldering stud bumps on the semiconductor chip to solder pillars/ball bumps on the substrate;

attaching the top heat slug further comprises attaching the top heat slug with a non-conductive bond to the top of the substrate; and

attaching the bottom heat slug further comprises attaching the bottom heat slug with a non-conductive bond to the bottom of the substrate.

8. The ~~system~~method as claimed in claim 6 further comprising:

hermetically sealing the top heat slug to the substrate by applying a vacuum or a further sealant through the substrate opening.

9. The ~~system~~method as claimed in claim 6 wherein:

attaching the top heat slug further comprises providing the top heat slug with a top recess in the center of a top surface thereof;

attaching the bottom heat slug further comprises providing the bottom heat slug with a bottom recess in the center of a bottom surface thereof; or

attaching the bottom heat slug further comprises attaching the bottom heat slug in a recessed cavity in the substrate.

10. The ~~system~~method as claimed in claim 6 wherein:

attaching the top heat slug further comprises providing the top heat slug with a first plurality of fins on a top surface thereof;

attaching the bottom heat slug further comprises providing the bottom heat slug with a second plurality of fins on a bottom surface thereof; or

further comprising attaching a ball grid array on the bottom of the substrate electrically connected to the semiconductor chip.

~~11. A semiconductor package system comprising:~~

~~a semiconductor chip;~~

~~a substrate having a substrate opening, the substrate having the semiconductor chip mounted thereon;~~

~~a first heat slug attached to a first surface of the semiconductor chip, the first heat slug at least partially encapsulating the semiconductor chip; and~~

~~a second heat slug attached to a second surface of the semiconductor chip through the substrate opening.~~

12. The system as claimed in claim 11 wherein:

the substrate further comprises solder pillars/ball bumps; and

the semiconductor chip further comprises stud bumps for conductively connecting the semiconductor chip to the solder pillars/ball bumps on the substrate.

13. The system as claimed in claim 11 wherein:

the substrate further comprises a vertical built-up wing; and

a solder mask on the substrate within the vertical built-up wing.

14. The system as claimed in claim 11 wherein:

the first heat slug further comprises a top recess on a top surface thereof;

the second heat slug further comprises a bottom recess on a bottom surface thereof; or

the first and second heat slugs provide at least 80% of the surface area of the semiconductor package system.

15. The system as claimed in claim 11 wherein:

the first heat slug further comprises a first fin on a top surface thereof; or

the second heat slug further comprises a second fin on a bottom surface thereof.

16. A semiconductor package system comprising:

a semiconductor chip;

a substrate having a substrate opening, the substrate having the semiconductor chip flipped and electrically mounted thereon;

a top heat slug to a first surface of the semiconductor chip using a conductive adhesive, the top heat slug at least partially encapsulating the semiconductor chip; and

a bottom heat slug using a conductive adhesive to a second surface of the semiconductor chip through the substrate opening.

17. The system as claimed in claim 16 wherein:

the semiconductor chip further comprises stud bumps on the semiconductor chip electrically connected to solder pillars/ball bumps on the substrate;

the top heat slug further comprises a non-conductive adhesive attaching the top heat slug to the top of the substrate; and

the bottom heat slug further comprises a non-conductive adhesive attaching the bottom heat slug to the bottom of the substrate.

~~18. The system as claimed in claim 16 wherein:~~

~~the substrate further comprises a vertical built-up wing; and~~

~~further comprising:~~

~~a solder mask on the substrate within the vertical built-up wing; and~~

~~solder pillars/ball bumps on the substrate in openings in the solder mask.~~

~~19. The system as claimed in claim 16 wherein:~~

~~the top heat slug further comprises a top recess in the center of a top surface thereof;~~

~~the bottom heat slug further comprises a bottom recess in the center of a bottom surface thereof;~~

~~the bottom heat slug further comprises the bottom heat slug in a recessed cavity in the substrate; or~~

~~the first and second heat slugs provide at least 85% of the surface area of the semiconductor package system.~~

~~20. The system as claimed in claim 16 wherein:~~

~~the top heat slug further comprises a first plurality of fins on a top surface thereof;~~

~~the bottom heat slug further comprises a second plurality of fins on a bottom surface thereof; or~~

~~further comprising a ball grid array on the bottom of the substrate electrically connected to the semiconductor chip.~~