WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a substrate including a cell array region and a connection region extending in a first direction from the cell array region;

an electrode structure including a bottom electrode structure which includes a plurality of bottom electrodes stacked on the substrate to be separated from one another and a top electrode structure which includes a plurality of top electrodes stacked on the bottom electrode structure to be separated from one another and has a stepped structure which includes a plurality of stepping surfaces, in the connection region; and

a plurality of recess holes formed to a first depth from the stepping surfaces, and having bottom surfaces which expose the bottom electrode structure,

wherein the first depth is ~~the~~ substantially the same as a height of the top electrode structure, and distances of the bottom surfaces of the recess holes from the substrate are different from one another.

2. The semiconductor memory device according to claim 1,

wherein each of the top electrodes includes a top pad region which is exposed by another top electrode positioned thereon, and

wherein each of the bottom electrodes includes a bottom pad region which is exposed by the top electrodes and one or more bottom electrodes positioned thereon, under each of the recess holes.

3. The semiconductor memory device according to claim 1, wherein the stepping surfaces of the stepped structure are disposed closer to the substrate as distances thereof from the cell array region in the first direction increase.

4. The semiconductor memory device according to claim 3, wherein the bottom surfaces of the recess holes are disposed closer to the substrate as distances thereof from the cell array region in the first direction increase.

5. The semiconductor memory device according to claim 1, wherein the stepped structure has a step height corresponding to a vertical pitch of the top electrodes.

6. The semiconductor memory device according to claim 1, further comprising:

first key grooves vertically penetrating the top electrode structure from the stepping surfaces.

7. The semiconductor memory device according to claim 6, wherein the first key grooves have a depth corresponding to the vertical pitch of the top electrodes.

8. The semiconductor memory device according to claim 6,

wherein at least one recess hole and at least one first key groove which are formed in the same stepping surface are disposed to be separated in a second direction, and the second direction is a direction parallel to the substrate intersecting with the first direction.

9. The semiconductor memory device according to claim 1, further comprising:

second key grooves formed at bottoms of the recess holes and vertically penetrating the bottom electrode structure from the bottom surfaces of the recess holes.

10. The semiconductor memory device according to claim 9, wherein the second key grooves have a depth corresponding to a vertical pitch of the bottom electrodes.

11. The semiconductor memory device according to claim 1, wherein the bottom electrode structure has a non-stepped structure in the connection region.

12. The semiconductor memory device according to claim 1, wherein the recess holes are disposed in a zigzag pattern in the first direction.

13. A semiconductor memory device comprising:

a substrate defined with a cell array region and a connection

region which extends in a first direction from the cell array region;

a first bottom electrode structure including a plurality of first bottom electrodes which are stacked on the substrate to be separated from one another;

a second bottom electrode structure including a plurality of second bottom electrodes which are stacked on the first bottom electrode structure to be separated from one another;

a top electrode structure including a plurality of top electrodes which are stacked on the second bottom electrode structure to be separated from one another, and having a stepped structure which includes a plurality of stepping surfaces, in the connection region;

a plurality of first recess holes formed to a first depth from the stepping surfaces, and having bottom surfaces which expose the second bottom electrode structure; and

a plurality of second recess holes formed to a second depth from the stepping surfaces, and having bottom surfaces which expose the first bottom electrode structure,

wherein the first depth is the substantially same as a height of the top electrode structure, the second depth is substantially equal to sum of the height of the top electrode structure and a height of the second bottom electrode structure, and distances of bottom surfaces of the first and second recess holes from the substrate are different from one another.

14. The semiconductor memory device according to claim 13,

wherein each of the top electrodes includes a top pad region which is exposed by another top electrode positioned thereon,

wherein each of the second bottom electrodes includes a first bottom pad region which is exposed by the top electrodes and one or more second bottom electrodes positioned thereon, under each of the first recess holes, and

wherein each of the first bottom electrodes includes a second bottom pad region which is exposed by the top electrodes, the second bottom electrodes and one or more first bottom electrodes positioned thereon, under each of the second recess holes.

15. The semiconductor memory device according to claim 13, wherein, based on a position spaced apart by the first depth from a bottom surface of each second recess hole, a diameter of a lower portion thereof is smaller than a diameter of an upper portion thereof.

16. The semiconductor memory device according to claim 13, wherein the first and second bottom electrode structures have a non-stepped structure in the connection region.

17. The semiconductor memory device according to claim 13, wherein the stepped structure has a step height corresponding to a vertical pitch of the top electrodes.

18. The semiconductor memory device according to claim 13, wherein at least one first recess hole, at least one second recess hole and at least one first key groove which are formed in the same stepping surface are disposed to be separated in a second direction, and the second direction is a direction that intersects with the first direction on a plane parallel to the substrate.