

A TRANSMITTER-RECEIVER SYSTEM

Technical field

The present inventive concept relates to a transmitter-receiver system.

5 Background

Radar has historically been used for determining the location of and to track objects such as aircrafts or vehicles over relatively great distances. Although this field of use for radar technology still is important new short range applications requiring high precision and low power consumption are now
10 also emerging for the industrial, the medical, the security and the consumer market. Examples of applications include not only determining distances to and positions of nearby objects, but also investigation of material properties such as thickness, size, dielectric properties, material composition etc.

Although radar technology as such is a mature technical field the
15 emerging applications introduces new challenges and requirements for the design of radar systems.

In a typical radar implementation an electromagnetic signal is transmitted and reflected by an object. The reflected signal is received and analyzed. Available technologies include for example pulse-based, Doppler or
20 frequency modulated radars.

Pulse-based radar systems measure the time-of-flight between the transmitter and the receiver for a measurement wavelet. For example, a reflected wavelet may be mixed with a locally generated reference wavelet which is delayed by a known time with respect to the transmitted wavelet. The
25 delay for which the maximum mixing product is achieved corresponds to the time of flight. Due to the pulsed nature of the measurement signals, this type of radar system lends itself for applications where low power consumption is a desirable. However, in order to provide high precision measurements, the delay between the reflected wavelet and the reference wavelet needs to be
30 precisely controlled.

Summary of the inventive concept

In view of the above, a general object of the present inventive concept is to provide a transmitter-receiver system enabling accurate control of a delay between transmission of a wavelet and generation of a reference wavelet.

5 According to an aspect of the inventive concept there is provided a transmitter-receiver system comprising: a transmitter arranged to transmit a wavelet; a receiver arranged to receive a wavelet; a wavelet generator arranged to generate a reference wavelet; and timing circuitry arranged to receive a reference clock signal, output a first trigger signal for triggering
10 transmission of a wavelet and output a second trigger signal for triggering generation of a reference wavelet. The timing circuitry further comprises a delay line including at least one delay element and being arranged to receive a signal at an input of the delay line and transmit a delayed signal at an output of the delay line, wherein a state of each delay element of at least a
15 subset of said at least one delay elements is switchable between at least a first state and a second state. A delay element in said first state, i.e. switched to its first state, presents a first propagation delay. A delay element in said second state, i.e. switched to its second state, presents a second propagation delay which differs from the first propagation delay by a value which is smaller
20 than a period of the reference clock signal. Thereby a total propagation delay of the delay line is configurable by controlling the state of each delay element of said subset. The system further comprises a controller arranged to control a delay between the first trigger signal and the second trigger signal by controlling the total propagation delay of the delay line. The system is
25 arranged to correlate the reference wavelet with a received wavelet for at least one setting of the total propagation delay.

By the subset of switchable delay elements the total propagation delay of the delay line may be digitally controlled without varying the number of active delay elements in the delay line. Rather the total propagation delay of
30 the delay line may be adjusted, in a step-wise manner, by the controller controlling the states of the switchable delay element(s). The delay line and the controller hence enables the total propagation delay to be varied between a minimum value of the total propagation delay of the delay line and a maximum value of the total propagation delay of the delay line in (preferably)
35 a plurality of discrete steps of a size smaller than the period of the reference clock signal, and even more preferably in steps of a size smaller than half the period of the reference clock signal.

The system provides control of the delay between the output of the first trigger signal and the output of the second trigger signal, wherein the delay between the transmission of a wavelet and the generation of a reference wavelet may be controlled. The accurate and digital control of the delay line renders in turn a precise and convenient control of the correlation measurement, enabling accurate determination of for example the time of flight for a transmitted and received wavelet.

Advantageously, the delay line is arranged such that the total propagation delay of the delay line is adjustable between a plurality of different total propagation delays, ranging from a minimum total propagation delay to a maximum total propagation delay and being adjustable between the minimum and maximum propagation delay in a plurality of steps of a same size. For example, said subset of delay elements may include at least two delay elements being switchable between at least the respective first and second states. Alternatively, or additionally, said at least one delay element of said subset may be switchable between at least said first, said second and a third state, a delay element in the third state presenting a third propagation delay which differs from the first and the second propagation delay by a value which is smaller than a period of the reference clock signal.

Advantageously, the difference between the second propagation delay and the first propagation delay for each delay element of the said subset is equal to one or more units of a step size parameter, which step size parameter is the same for all delay elements of said subset. The delay line may thereby be arranged to provide a total propagation delay which may be adjusted in one or more steps of a size equal to the step size parameter. Preferably, the step size parameter is smaller than the first propagation delay of each delay element of said subset.

In accordance with the above-mentioned aspect, said subset of delay elements may include at least two delay elements arranged such that each of said at least two delay elements receives the signal, one after another, and transmits the signal after a propagation delay of the delay element.

With reference to the above-mentioned aspect "a wavelet" refers to an electro-magnetic oscillating signal having an amplitude envelope beginning at zero amplitude, increasing to a maximum amplitude, and then decreasing to zero amplitude. A wavelet may comprise one or more oscillations.

The second trigger signal may trigger generation of a reference wavelet, wherein the wavelet generator is arranged to generate the reference wavelet with an initial predetermined instantaneous phase.

The wavelet generator may include a pulsed oscillator circuitry
5 switchable between an off-state and an on-state. The pulsed oscillator circuitry may be arranged to switch from the off-state to the on-state in response to the second trigger signal, wherein generation of a reference wavelet is initiated. The pulsed oscillator circuitry may be arranged to switch back to the off-state after a predetermined duration (i.e. relative to the
10 switching to the on-state), the predetermined duration defining the duration of the generated reference wavelet. The oscillator circuitry may include a tank circuit. The “on-state” may be defined as the state wherein the tank circuit oscillates, i.e. is active. The “off-state” may be defined as the state wherein the tank circuit does not oscillate, i.e. is inactive. A pulsed oscillator circuitry
15 provides the advantage that the initial instantaneous phase of the reference wavelet always may be defined with a high accuracy, regardless of the delay. This may be contrasted with systems employing a pulse modulated continuous wave carrier (e.g. mixing a base-band pulse with an output of a continuously running carrier wave source) wherein different delays of the
20 base-band pulse may result in different phase relationships between the base-band pulse and the carrier. Hence, in such systems the delay may not be arbitrarily varied without altering the initial instantaneous phase of the reference pulse. The accuracy of such systems may thus be sensitive to phase noise of the carrier wave source since the initial instantaneous phase
25 of the reference wavelet is uncorrelated with the timing of the base-band pulse. Advantageously, also the wavelets transmitted by the transmitter may be generated by a wavelet generator arranged to generate a wavelet to be transmitted with an initial predetermined instantaneous phase in response to the first trigger signal. A transmit wavelet generator may be configured in a
30 manner corresponding to the above-mentioned reference wavelet generator. Especially, the same wavelet generator may be used to generate both transmit wavelets and reference wavelets.

According to one embodiment the system is arranged to correlate the reference wavelet with a received wavelet for at least one setting of the total
35 propagation delay in a measurement mode of the system.

In the measurement mode, the system may be arranged to correlate a reference wavelet with a received wavelet for a plurality of different settings of

the total propagation delay of the delay line. This enables probing or scanning for an object for a plurality of different total propagation delays of the delay line and thus for a plurality of different time of flight values. This may be advantageous in applications wherein a distance to a monitored object not is known a priori. It may also be advantageous for improving the accuracy of a time of flight determination since correlation results for a plurality of different total propagation delays may be compared.

According to one embodiment each delay element comprises a logic circuit element. If the delay line comprises more than one delay element the logic circuit elements of the delay elements may be interconnected. Logic circuit elements may provide a power and cost-effective implementation of a delay line.

According to one embodiment each delay element comprises a logic circuit element, wherein each delay element of said subset is switchable between at least the first state and the second state by varying a capacitive load of the logic circuit element. The variable capacitive load may be connected to an output of the logic circuit element. The variable capacitive load of a delay element may be varied between a first capacitance, wherein said delay element presents the first propagation delay, and a second capacitance, wherein said delay element presents the second propagation delay. This provides a comparably simple implementation of a switchable delay element.

According to one embodiment each delay element comprises a logic circuit element, wherein each delay element of said subset is switchable between at least a first state and a second state by varying a current supplied to the logic circuit element. A delay element may be switchable between said at least first and second state by varying a charge/discharge current of the logic circuit element. The current may be varied between a first current, wherein said delay element presents the first propagation delay, and a second current, wherein said delay element presents the second propagation delay. This provides a comparably simple implementation of a switchable delay element. In particular, the logic circuit element may be switchable between a first current limited state and a second current limited state.

According to one embodiment an adjustment range of the total propagation delay of the delay line corresponds to at least a period of the reference clock signal or a half period of the reference clock signal. The total propagation delay of the delay line may hence be adjusted in a step-wise

manner throughout at least a half or whole period of the reference clock signal. This may improve the flexibility of the system.

According to one embodiment the timing circuitry further comprises trigger circuitry arranged to receive, at an input of the trigger circuitry, a clock signal and transmit, at an output of the trigger circuit, the second trigger signal in response to receiving a number of rising and/or falling edges of the clock signal, wherein the controller is arranged to control a delay between the output of the first trigger signal and the second trigger signal by controlling the total propagation delay of the delay line and said number of rising and/or falling edges. The trigger circuitry may thus be arranged to delay an output of the second trigger signal with respect to an output of the first trigger signal by a number of periods (or half periods) of the clock signal. The second trigger signal may be transmitted to the output of the timing circuitry. According to these embodiments, the delay between the transmitted wavelet and the generation of the reference wavelet may be controlled using two different mechanisms: by controlling the total propagation delay of the delay line (what may be referred to as a fine delay control), and by controlling the trigger event of the trigger circuitry (what may be referred to as a coarse delay control). Additionally, the dynamic range of the system may be improved. Greater changes of the delay between the transmitted wavelet and the reference wavelet (i.e. changes which exceed the step size of the coarse delay control) may be achieved by the coarse delay control (i.e. by controlling the number of rising and/or falling edges) in combination with the fine delay control. Meanwhile, smaller changes of the delay (i.e. changes which fall below the step size of the coarse delay control) may be achieved by the fine delay control.

According to one embodiment the clock signal received by the trigger circuitry is a delayed reference clock signal transmitted by the delay line. The delay line may be arranged to receive, at the input of the delay line, the reference clock signal from an input of the timing circuitry and transmit, at the output of the delay line, a delayed reference clock signal to the input of the trigger circuitry. Thus the fine delay control may be applied prior to the coarse delay control.

According to one embodiment the system is arranged to, for at least one setting (preferably at least two settings) of said number of rising and/or falling edges for the trigger circuitry, correlate a reference wavelet with a received wavelet for a set of different total propagation delays of the delay

line. Thereby correlation results for a set of different delays between a transmitted wavelet and a reference wavelet may be determined, which set may span over an interval greater than one or more reference clock signal periods or half reference clock signal periods. The correlation results may be
5 obtained for delay values which differ by the step size of the fine delay control. The correlations may be performed in a measurement mode of the system.

The first propagation delay (of the first state) may be smaller than the second propagation delay (of the second state) for each delay element of the
10 subset of delay elements. Thus, a propagation delay of a switchable delay element may be increased by switching from the first to the second state. In particular, the second state of each delay element of the subset may be the state (of each delay element) resulting in the greatest propagation delay of said at least first and second states (of each delay element). At least one
15 delay elements of the subset of switchable delay elements may further be switchable between more than two states, wherein the second state for each delay element switchable between more than two states is the state resulting in the greatest propagation delay for said delay element.

According to one embodiment the delay line includes at least one
20 tunable delay element having a propagation delay which is tunable, wherein the controller is arranged to control or set each delay element of said subset of delay elements to said first state and thereafter tune the propagation delay of said at least one tunable delay element such that the total propagation delay of the delay line corresponds to an integer number of periods of the
25 reference clock signal or half periods of the reference clock signal. Thereby a first end point of the adjustment range of the total propagation delay of the delay line may be tuned to correspond to an integer number of half periods of the reference clock signal.

Said at least one tunable delay element may be formed by the delay
30 elements of the subset of switchable delay elements. Accordingly, according to one embodiment the controller is arranged to control or set each delay element of said subset of delay elements to said first state and thereafter tune the first propagation delay of each delay element of said subset of delay elements such that the total propagation delay of the delay line corresponds
35 to an integer number of periods of the reference clock signal or half periods of the reference clock signal. Thereby a first end point of the adjustment range of the total propagation delay of the delay line may be tuned to correspond to

an integer number of half periods of the reference clock signal. The first end point may then be used as a reliable reference from which the total propagation delay of the delay line may be adjusted by changing the states of the delay elements. If used in combination with the trigger circuitry, in accordance with any of the above embodiments, the first end point may serve as a reliable reference for any setting of the number of rising and/or falling edges for the trigger circuitry.

Alternatively, said at least one tunable delay element may be formed by an additional delay element, not forming part of the subset of switchable delay elements. Accordingly, according to an alternative embodiment the delay line includes an additional delay element having a propagation delay which is tunable, wherein the controller is arranged to control or set each delay element of said subset of delay elements to said first state and thereafter tune the propagation delay of said additional delay element such that the total propagation delay of the delay line corresponds to an integer number of periods of the reference clock signal or half periods of the reference clock signal. This embodiment provides advantages corresponding to the embodiment for tuning the first propagation delay. Additionally, tuning the additional delay element, compared to tuning each delay element of said subset of delay elements, may simplify the implementation of the controller and/or the delay line.

According to one embodiment the controller is further arranged to control or set each delay element of said subset of delay elements to said second state and tune the second propagation delay of each delay element of said subset of delay elements such that the total propagation delay of the delay line corresponds to an integer number of periods of the reference clock signal or half periods of the reference clock signal.

This embodiment may be combined with any of the above-mentioned embodiments tuning the first end point of the adjustment range of the total propagation delay, e.g. either the embodiment for tuning the first propagation delay or the embodiment for tuning the propagation delay of the additional delay element. According to the embodiment a second end point of the adjustment range of the total propagation delay of the delay line may be tuned to correspond to an integer number of half periods of the reference clock signal. The second end point may then be used as a reliable reference from which the total propagation delay of the delay line may be adjusted by changing the states of the delay elements. If used in combination with the

trigger circuitry, in accordance with any of the above embodiments, the second end point may serve as a reliable reference for any setting of the number of rising and/or falling edges for the trigger circuitry. In particular, tuning of the second propagation delay of a delay element may comprise
5 tuning the size of the step size parameter defined above.

According to an embodiment combining the embodiment for tuning the first propagation delay and the embodiment for tuning the second propagation delay, the controller of the system is arranged to:

control or set each delay element of said subset of delay elements to
10 said first state and thereafter tune the first propagation delay of each delay element of said subset of delay elements such that the total propagation delay of the delay line corresponds to a first integer number of periods of the reference clock signal or half periods of the reference clock signal, and

control or set each delay element of said subset of delay elements to
15 said second state and thereafter tune the second propagation delay of each delay element of said subset of delay elements such that the total propagation delay of the delay line corresponds to a second integer number of periods of the reference clock signal or half periods of the reference clock signal.

20 This embodiment provides similar advantages as the above mentioned embodiments for tuning the first and the second propagation delay or the propagation delay of the additional delay element.

Also an embodiment combining tuning of the first and the second propagation delay may be particularly advantageous for a system comprising
25 the trigger circuitry in accordance with any of the above embodiments. Since the first end point of the adjustment range of the delay line corresponds to a first integer number of (half) reference clock signal periods and the second end point corresponds to a second integer number of (half) reference clock signal periods, a linear control of the delay between the first trigger signal for
30 triggering transmission of a wavelet and the second trigger signal for triggering generation of a reference wavelet is possible. If the first propagation delay is smaller than the second propagation delay for each switchable delay element the first end point of the adjustment range of the delay line may correspond to a minimum end point of the adjustment range, i.e. a minimum
35 value of the total propagation delay of the delay line. Further, if the second state of each delay element of the subset is the state resulting in the greatest propagation delay of the at least first and second states of each delay

element the second end point of the adjustment range of the delay line may correspond to a maximum end point of the adjustment range, i.e. a maximum value of the total propagation delay of the delay line. Assuming, as an example, that the second integer is equal to the first integer plus one a same delay between the first and the second trigger signal output by the trigger circuitry may be obtained by either setting the number of rising and/or falling edges for the trigger circuitry to X and setting all switchable delay elements to their respective second state, or by setting the number of rising and/or falling edges for the trigger circuitry to X+1 and setting all switchable delay elements to their respective first state. Thus the linearity of the control of the delay between the first trigger signal and the second trigger signal may be improved. An associated advantage is that overlaps or gaps in correlation measurements for a range of delays, which range exceeds one (half) period of the reference clock signal, may be avoided since the adjustment range for the fine delay control (i.e. the total propagation delay of the delay line) may be tuned to correspond to precisely one (half) period of the reference clock signal. Consequently, an accurate estimate of the step size of the total propagation delay of the delay line may be obtained by dividing the length of a (half) reference clock signal period by the number of steps in which the total propagation delay of the delay line may be adjusted.

The controller may be arranged to perform the acts in any of the above embodiments including tuning of the first propagation delay, the second propagation delay or both, or the propagation delay of the additional delay element in a calibration mode of the system.

According to one embodiment the controller is further arranged to determine a phase difference between the reference clock signal, received at the input of the delay line, and a delayed reference clock signal, output from the delay line, and tune the first propagation delay and/or the second propagation delay of each delay element of said subset of delay elements based on the phase difference. In an embodiment wherein the delay line includes an additional delay element having a propagation delay which is tunable the controller may also be arranged to tune the propagation delay of the additional delay element based on the phase difference. The controller may tune the respective propagation delay until the determined phase difference differs from zero by less than a threshold (if tuning for correspondence with entire reference clock signal periods), or until the determined phase difference differs from 180 degrees by less than a

threshold (if tuning for correspondence with half periods of the reference clock signal). These embodiments may be applied to any of the above embodiments including tuning of the first propagation delay, the second propagation delay or both. Detecting a phase difference provides an accurate way of determining when the total propagation delay of the delay line sufficiently corresponds to a number of (half) periods of the reference clock signal.

According to one embodiment the controller is arranged to tune the first and/or the second propagation delay of each delay element of said subset of delay elements using a control signal which is common for the delay elements of said subset. Thereby a same tuning of all switchable delay elements may be achieved during tuning. This may simplify the implementation of the controller and/or the delay line. Additionally it may facilitate an equal tuning for all switchable delay elements.

According to one embodiment each delay element comprises a logic circuit element, wherein each delay element of said subset is switchable between at least the first state and the second state by varying a capacitive load of the logic circuit element between a first capacitance and a second capacitance, and wherein the tuning of the first propagation delay comprises tuning the first capacitance and the tuning of the second propagation delay comprises tuning the second capacitance. This provides a comparably simple and accurate implementation of the delay line and the calibration.

According to one embodiment each delay element comprises a logic circuit element, wherein each delay element of said subset is switchable between at least a first state and a second state by varying a current supplied to the logic circuit element between a first current and a second current, and wherein the tuning of the first propagation delay comprises tuning the first current and the tuning of the second propagation delay comprises tuning the second current. This provides a comparably simple and accurate implementation of the delay line and the calibration.

In the above-mentioned embodiment wherein the delay line includes an additional delay element having a propagation delay which is tunable, the additional delay element may comprise a logic circuit element wherein tuning the propagation delay of the additional delay element may comprise tuning a capacitive load of the logic circuit element or a current supplied to the logic circuit element.

According to one embodiment the controller is arranged to determine a first setting of the states of the delay elements of said subset of delay elements, resulting in a total propagation delay of the delay line corresponding to a first integer number of periods of the reference clock signal or half periods of the reference clock signal. Thereby, a first setting of the states resulting in a total propagation delay corresponding to a (first) integer number of (half) periods of the reference clock signal may be determined. The first setting may then be used as a reliable reference from which the total propagation delay of the delay line may be adjusted, i.e. by changing the setting of one or more of the delay elements. The controller may be arranged to determine the first setting by controlling or setting a number of the delay elements of said subset of delay elements to their respective first state and thereafter repeatedly change the state of one or more of the delay elements of the subset until the total propagation delay of the delay line corresponds to a first integer number of (half) reference clock signal periods.

In addition to a first setting of the states of the delay elements of the subset the controller may be arranged to determine a second setting of the states of the delay elements of said subset of delay elements, resulting in a total propagation delay of the delay line corresponding to a second integer number of periods of the reference clock signal or half periods of the reference clock signal. The controller may be arranged to determine the second setting by setting or controlling the states of the delay elements of the subset in accordance with the determined first setting and thereafter repeatedly changing the state of one or more of the delay elements of the subset until the total propagation delay of the delay line corresponds to the second integer number of (half) reference clock signal periods. The first and the second settings may then be used as settings defining end points of the adjustment range of the total propagation delay.

The first setting of the states may result in a total propagation delay which is smaller than a total propagation delay resulting from the second setting of the states.

The first propagation delay may be smaller than the second propagation delay for each switchable delay element wherein the first setting may be determined by setting or controlling each delay element of the subset to the respective first state and thereafter repeatedly change the state of one or more of the delay elements to increase the total propagation delay until the total propagation delay of the delay line corresponds to the first integer

number of (half) reference clock signal periods. Further, the second setting may be determined by setting or controlling each delay element of the subset in accordance with the determined first setting and thereafter repeatedly change the state of one or more of the delay elements to increase the total propagation delay until the total propagation delay of the delay line corresponds to the second integer number of (half) reference clock signal periods.

Also this embodiment may be particularly advantageous for a system comprising trigger circuitry, in accordance with any of the above embodiments. Since the first setting of the states results in a total propagation delay corresponding to a first integer number of (half) reference clock signal periods and the second setting results in a total propagation delay corresponding to a second integer number of (half) reference clock signal periods, a linear control of the delay between the first trigger signal for triggering transmission of a wavelet and the second trigger signal for triggering generation of a reference wavelet is possible. Assuming, as an example, that the second integer is equal to the first integer plus one a same delay between the first and the second trigger signal output by the trigger circuitry may be obtained by either setting the number of rising and/or falling edges for the trigger circuitry to X and setting the switchable delay elements in accordance with the determined second setting, or by setting the number of rising and/or falling edges for the trigger circuitry to $X+1$ and setting the switchable delay elements in accordance with the determined first setting. Thus the linearity of the control of the delay between the first trigger signal and the second trigger signal may be improved. An associated advantage is that overlaps or gaps in correlation measurements for a range of delays exceeding one (half) period of the reference clock signal may be avoided since the adjustment range for the fine delay control (i.e. the total propagation delay of the delay line) may be determined to correspond to precisely one (half) period of the reference clock signal. Consequently, an estimate of the step size of the total propagation delay of the delay line may be obtained by dividing the length of a (half) reference clock signal period by the number of steps in which the total propagation delay of the delay line may be adjusted between the first and the second setting. A maximum error of this estimate will correspond to the step size of the total propagation delay.

According to one embodiment the controller is further arranged to determine a phase difference between the reference clock signal, received at

the input of the delay line, and a delayed reference clock signal, output from the delay line, and determine said first and/or second settings by repeatedly changing the state of one or more of the delay elements of said subset of delay element based on the determined phase difference. The controller may
5 change the state of one or more of the delay elements of said subset until the determined phase difference differs from zero by less than a threshold (if tuning for correspondence with entire reference clock signal periods), or until the determined phase difference differs from 180 degrees by less than a
10 threshold (if tuning for correspondence with half periods of the reference clock signal). This embodiment may be applied to any of the above embodiments including determination of the first or second settings or both. Determining a phase difference provides an accurate way of determining when the total propagation delay of the delay line sufficiently corresponds to a number of (half) periods of the reference clock signal.

15 According to an alternative embodiment the system may be arranged to, during a measurement mode of the system, for each correlation between a reference wavelet and a received wavelet, determine and record a phase difference between the reference clock signal received at the input of the delay line and a delayed reference clock signal transmitted at the output of
20 the delay line. This makes it possible to determine the above-mentioned first and the second settings of the states of the delay elements of said subset during post-processing, i.e. by finding the settings of the states of the delay elements of the delay line which result in a desired phase difference (e.g. approximately zero degrees or approximately 180 degrees). Consequently,
25 the delay between a transmitted wavelet and generation of a reference wavelet resulting from each setting of the delay line, as well as the step size, may be estimated during post-processing.

Brief description of the drawings

The above, as well as additional objects, features and advantages of the
30 present inventive concept, will be better understood through the following illustrative and non-limiting detailed description of preferred embodiments of the present inventive concept, with reference to the appended drawings, where like reference numerals will be used for like elements, wherein:

Fig. 1 is a schematic illustration of a general layout of a transmitter-
35 receiver system in accordance with an embodiment.

Fig. 2 schematically illustrates an embodiment of the timing circuitry in Fig. 1.

Fig. 3 illustrates a delay line in accordance with one embodiment.

Fig. 4 illustrates a delay line in accordance with one embodiment.

5 Figs 5-7 illustrates aspects of an embodiment of a transmitter-receiver system in use.

Fig. 8 illustrates an embodiment of a timing circuitry and a controller.

Fig. 9 illustrates an embodiment of a timing circuitry and a controller.

Fig. 10 illustrates an embodiment of a timing circuitry and a controller.

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Detailed description of preferred embodiments

Detailed embodiments of aspects of the present inventive concept will now be described with reference to the drawings.

Fig. 1 generally illustrates a layout of a transmitter-receiver system 100 in accordance with an embodiment. For brevity, the transmitter-receiver system will in the following be referred to as the system 100. The system 100 comprises a transmitter 102 and a receiver 108. The transmitter 102 includes a first wavelet generator 104. The transmitter 102 is arranged to transmit wavelets generated by the first wavelet generator 104. As will be described in greater detail below the first wavelet generator 104 may be arranged to generate a wavelet in response to a trigger signal P_tx. The receiver 108 is arranged to receive wavelets originally transmitted by the transmitter 102 and reflected by an external object, the type of object being dependent on the particular application of the system 100. The receiver 108 includes a second wavelet generator 110. As will be described in greater detail below the second wavelet generator 110 may be arranged to generate a wavelet in response to a trigger signal P_rx. Wavelets generated by the second wavelet generator 110 may in the following be referred to as reference wavelets.

The receiver 108 further comprises a correlator circuit 111 arranged to correlate a reference wavelet with a wavelet received by the receiver 108, if any. More generally, the correlator circuit 111 may be arranged to correlate a reference wavelet received at a first input of the correlator circuit 111 with a signal received at a second input of the correlator circuit 111. The signal may or not may not include a received wavelet depending on the timing of the reference wavelet. The result of the correlation may be provided at an output of the receiver 108. According to a preferred embodiment, the correlator circuit 111 includes a mixer for mixing a reference wavelet with a received

wavelet. The product W_{mix} may be provided to an integrator (not shown in Fig. 1) which may form part with the receiver 108 or be arranged external to the receiver 108. The integrated product W_{int} may be provided to an analog-to-digital converter (ADC) and a digital signal processor (DSP) for further processing and analysis. Moreover, the integrated product W_{int} may also be amplified or attenuated before being provided to an ADC in order to optimize the signal level with respect to the dynamic range of the ADC. The amplification or attenuation may be variable to accommodate different signal levels to the ADC dynamic range.

As schematically indicated in Fig. 1 the transmitter 102 may include a transmitting antenna 106 wherein the transmitter 102 may be arranged to transmit wavelets via the transmitting antenna 106. Similarly, the receiver 108 may include a receiving antenna 112 wherein the receiver 108 may be arranged to receive wavelets via the receiving antenna 112. In that case, an input of the correlator circuit 111 may be connected to an output of the receiving antenna 112. The transmitting antenna 106 and a receiving antenna 112 may provide improved range for the system 100 as well as an improved directional control. Although illustrated as physically separate antennas, the system 100 may alternatively use a same antenna for transmitting and receiving wavelets. If needed, additional amplifiers (not shown) may be provided in connection to both the transmitter and receiver antennas. The antenna(s) may be provided in an integrated antenna implementation such as a patch antenna configuration. Further non-limiting examples include a slot configuration, a ring configuration, a spiral configuration, a bow-tie configuration, a Vivaldi configuration, and a quasi-yagi configuration.

The system 100 further comprises timing circuitry, as generally indicated by reference numeral 118 in Fig. 1. The timing circuitry 118 is arranged to receive a reference clock signal Ref_clock at an input of the timing circuitry 118 and output a first trigger signal Tx_trigg and a second trigger signal Rx_trigg , wherein the outputs of the signals Tx_trigg and Rx_trigg are delayed with respect to each other. Various forms of Tx_trigg and Rx_trigg are possible. For example, the timing circuitry 118 may be arranged to output Tx_trigg by increasing or decreasing a voltage level at the Tx_trigg output of the timing circuitry 118. Similarly the timing circuitry 118 may be arranged to output Rx_trigg by increasing or decreasing a voltage level at the Rx_trigg output of the timing circuitry 118. Each of Tx_trigg and Rx_trigg may thus comprise a rising or a falling edge. Alternatively, each of

the first trigger signal Tx_trigg and the second trigger signal Rx_trigg may comprise one or more rising and/or falling edges. Each of Tx_trigg and Rx_trigg may for example include a pulse or a train of pulses.

The reference clock signal Ref_clock may be a periodic signal
5 oscillating between a high and a low level or state (e.g. a first voltage level and a second voltage level). The Ref_clock may be provided by a reference clock comprised in the system 100 or arranged external from the system 100. The duration of a period of the Ref_clock signal will in the following be denoted T_ref. Ref_clock forms a control signal for the system 100 providing
10 a time basis for the system. The frequency of the reference clock signal will depend on the application of the system 100. As a non-limiting example the reference clock signal may have a frequency in the 10 MHz to 10 GHz range.

Optionally, the timing circuitry 118 may be preceded by a frequency multiplier or up-converter (not shown) arranged to receive a clock signal at a
15 base frequency and output a clock signal having a frequency which is a multiple of the base frequency. A frequency multiplier may for example be implemented using a phase-locked loop (PLL) arranged to receive and lock on to the phase of the received clock signal and up-convert the received clock signal by a factor P, e.g. an optionally configurable fraction or integer number.
20 Thereby a higher frequency reference signal may be used to control the relative timing of generation of transmission wavelets and reference wavelets while avoiding high frequency clock signals in other (not shown) parts connected to the system 100. In the following, the reference clock signal Ref_clock received by the timing circuitry may thus be a reference clock
25 signal of the base frequency or an up-converted frequency.

The system 100 further comprises a first pulse generator 114. The first pulse generator 114 is arranged to receive the first trigger signal Tx_trigg from the timing circuitry 118. The pulse generator 114 is further arranged to output a pulsed signal P_tx in response to receiving the first trigger signal
30 Tx_trigg. Tx_trigg may thus trigger the output of the first pulse generator 114. More specifically, P_tx may be a baseband pulse. P_tx may have a duration of Ptx_dur. The pulse generator 114 may comprise a combination of digital gates, such as INV, NOR, and NAND, where the configuration of the gates enables that a rising or falling edge received at the input of the first pulse
35 generator 114 triggers the generation of a pulse on the pulse generator output. As an example, the input signal may be fed to a first input of a NOR gate and to an input of an INV gate. The output of the INV gate may be

connected to a second input of the NOR gate. By this configuration a pulse P_tx may be triggered each falling edge of the input signal, where the duration of the pulse corresponds to the propagation delay of the INV gate. However, as this is one example of the pulse generator implementation there are other methods that provide the same functionality using digital gates, transistors, diodes and passive devices.

The first wavelet generator 104 is arranged to output a wavelet in response to the signal P_tx. More specifically, the first wavelet generator 104 may be arranged to generate and output a wavelet in response to receiving P_tx. Advantageously the first wavelet generator 104 may be arranged to generate a wavelet with a duration equal to P_tx_dur.

The system 100 further comprises a second pulse generator 116. The second pulse generator 116 is arranged to receive the second trigger signal Rx_trigg from the timing circuitry 118. The pulse generator 116 is further arranged to output a pulsed signal P_rx in response to receiving the second trigger signal Rx_trigg. Rx_trigg may thus trigger the output of the second pulse generator 116. More specifically, P_rx may be a baseband pulse. P_rx may have a duration of P_rx_dur. P_rx_dur may be equal to T_rx_dur.

Referring to Fig. 1, the second wavelet generator 110 is arranged to output a wavelet, forming a reference wavelet, in response to the pulsed signal P_rx. More specifically, the second wavelet generator 110 may be arranged to generate and output a wavelet in response to receiving P_rx. Advantageously the duration of the wavelet output by the second wavelet generator 110 corresponds to P_rx_dur.

If Tx_trigg and Rx_trigg include a single rising and/or rising edge, the output of Tx_trigg and Rx_trigg may result in the output of a single pulsed signal P_rx and T_rx by the first pulse generator 114 and the second pulse generator 116, respectively. If Tx_trigg and Rx_trigg include a plurality of rising and/or falling edges, the output of Tx_trigg and Rx_trigg may result in the output of a plurality of pulsed signals P_rx and T_rx by the first pulse generator 114 and the second pulse generator 116, respectively. Thus a single output of a trigger signal (Tx_trigg or Rx_trigg) may result in generation of a plurality of wavelets (transmit wavelets by the first wavelet generator 114 or reference wavelets by the second wavelet generator 110).

Although in Fig. 1 the first pulse generator 114 has been illustrated as being a separate component from the first wavelet generator 104 this distinction has been made to facilitate understanding. For example the

functionality of the first pulse generator 114 may be implemented in a same circuitry as the first wavelet generator 104. According to this example the system may comprise a first wavelet generator 104 arranged to output a wavelet in response to receiving the trigger signal Tx_trigger from the timing
5 circuitry 118. Additionally, although in Fig. 1 being provided outside the transmitter 102, the first pulse generator 114 may also form part of the transmitter 102. This discussion applies correspondingly to the second pulse generator 116 and the second wavelet generator 110. Moreover, although the system 100 includes two separate wavelet generators, the present inventive
10 concept is equally applicable to a system using a same wavelet generator for generation of the transmission wavelet and the reference wavelet. For example, a switch may be arranged at the output of the wavelet generator allowing a generated wavelet to be provided to the transmit antenna 106 or to the correlator circuit 111.

15 The first wavelet generator 104 and the second wavelet generator 110 may each include a pulsed oscillator circuitry arranged to be switched from an off-state to an on-state and back to the off-state, wherein the oscillator circuitry during the on-state generates and outputs an oscillating signal for forming a transmit wavelet or a reference wavelet with an initial
20 predetermined instantaneous phase. The initial instantaneous phase (i.e. the instantaneous phase at start-up of the oscillation of the generated wavelet) may be the same for each of the transmit wavelets and/or the reference wavelet(s) (for example an instantaneous phase of 0°). However variation of the initial instantaneous phase has also been contemplated (for example
25 generating a first set of one or more transmit or reference wavelets with an initial instantaneous phase of 0° and a subsequent set of one or more transmit or reference wavelets with an initial instantaneous phase of 180°). According to a preferred example, the first wavelet generator 104 and second wavelet generator 110 may be implemented using a transceiver module as
30 described in PCT/EP2011/058847 in transmitter operation. The transceiver module comprises: a tank circuit, a variable differential conductance (VDC), preferably in the form of a resonant tunneling diode (RTD), coupled to the tank circuit, and a variable resistance coupled to the VDC and arranged to bias the VDC into a region of positive differential conductance during a first
35 state of operation of the transceiver, and bias the VDC into a region of negative differential conductance during a second state of operation of the transceiver. During the transceivers first state of operation no output signal is

generated and during the second state of operation a sinusoidal radio frequency signal is generated. Thus by switching the transceiver from the first state to the second state and back to first state again, a wavelet signal may be generated where the duration of the wavelet corresponds to the time the transceiver is in its second state of operation. The transceiver may switch to the second state in response to receiving the pulsed signal (i.e. P_tx or P_rx) and maintain the second state for the duration of the pulsed signal. Compared with other methods of wavelet generation, this implementation offers a low-complexity method for generating wavelets with a well-defined start position and duration and a coherent phase content within the wavelet which enables phase dependent system implementation such as the system 100 and low power consumption due to the pulsed operation. This particular implementation may enable generation of wavelets of a duration between 10 ns and 10 ps in the mm-wave band, which gives a theoretical range resolution of 1.5 m to 1.5 mm, respectively. The wavelet generator described above may be implemented by using other oscillator configurations, for example, relying on negative differential conductance or positive feedback, where it is possible to start and quench the oscillations rapidly. Alternative implementations of wavelet generators include passing a continuous oscillation through a switchable amplifier, filtering of a baseband pulse, up-conversion of a baseband pulse, or using digital gates to create the desired waveform.

With reference to Fig. 1, the system 100 comprises a controller 120. The controller 120 is arranged to control a delay between, on the one hand, a rising or falling edge of Ref_clock and the output of the trigger signal Tx_trigg, and on the other hand, a delay between said rising or falling edge of Ref_clock and the output of the trigger signal Rx_trigg. Thereby, the controller 120 may control a relative delay between Tx_trigg and Rx_trigg as will be described in greater detail below. By controlling the delay between the trigger signals Tx_trigg and Rx_trigg, the controller 120 may control a delay between transmission of a wavelet and generation of a reference wavelet.

Fig. 2 schematically illustrates an embodiment of the timing circuitry 118. The timing circuitry 118 comprises a delay circuit 122 and trigger circuitry which will be disclosed in greater detail below. The delay circuit 122 includes delay elements 123-1 to 123-A which will be commonly referenced 123. The delay elements 123 of the delay line 122 are arranged in a sequence to form a delay line. In the following, the delay circuit 122 may thus be referred to as a delay line 122. The number of delay elements 123,

denoted A, may vary for different implementations as may be understood from the following.

In Fig. 2, each delay element 123 is illustrated as including a logic circuit element in the form of an inverter. Inverters may enable a reliable and power efficient implementation of a delay line. However other types of logic circuit elements are also possible, such as AND-gates and OR-gates. More generally any circuit element may be used which is arranged to receive a signal at an input and transmit the received signal at an output after a certain time, i.e. the propagation delay of the circuit element. The circuit element may for example receive a signal at the input and transmit a signal at an output in response to a signal level (e.g. a voltage level) of the received signal exceeding a predetermined threshold. In the context of this application, a propagation delay of a delay element or another component may be defined as the length of time between a changed signal level at the input results in a changed signal level at the output. More specifically, a propagation delay may be determined as the time passing from an instant at which a level of an input signal crosses 50 % of a maximum input amplitude to a following instant at which a level of an output signal crosses 50 % of a maximum output amplitude. These definitions correspond to established conventions in the art.

Returning to Fig. 2, the delay line 122 is arranged to receive the reference clock signal Ref_clock at an input of the delay line 122 and transmit a delayed reference clock signal at an output of the delay line 122. The delay element 123-1 may receive Ref_clock from the input of the delay line 122. Each delay element 123-2 to 123-A may then, one after another, receive a (partially) delayed representation of Ref_clock from a previous delay element 123-1 to 123-(A-1) and transmit a (partially) delayed representation of Ref_clock to a next delay element 123-2 to 123-A.

In accordance with the present inventive concept each delay element 123 is arranged to be switchable, independently from the other delay elements 123 of the delay line 122 (if any) between two states. In the following, reference will be made to the A delay elements 123 of the delay line 122. However it should be noted that the delay line 122 may include further delay elements which may, or may not, be switchable delay elements. The delay elements 123 may thus form a subset of delay elements of the delay line 122. A delay element 123-i switched to a first state may present a propagation delay τ_i ($i = 1 \dots A$). A delay element 123-i switched to a second state may present a propagation delay $\tau_i + \Delta t_i$. It may be understood that τ_i may

vary between the delay elements, e.g. due to imperfections during manufacturing or slightly different electric environments. As may be understood from the following variations of τ_i between different delay elements need not negatively affect the usability of the delay line 122 with respect to the system 100. Additionally Δt_i may vary slightly between the delay elements 123. The delay line 122 should preferably be designed such that any variations of Δt_i between the delay elements 123 are minimized or at least reduced. To simplify understanding of the present inventive concept it will in the following discussion be assumed that these differences are negligible and that τ_i and Δt_i are substantially equal for all delay elements, wherefore the index i may be omitted.

By controlling the states (i.e. switching the delay elements between their respective states), a total propagation delay of the delay line 122 may be varied in discrete steps of size Δt (thus forming a step size for the delay line) from $A \cdot \tau$ to $A \cdot (\tau + \Delta t)$. Optionally, one or more of the delay elements 123 may be switchable between three states wherein a propagation delay of a delay element 123 may be switched between any one of τ , $\tau + \Delta t$ or $\tau + 2 \cdot \Delta t$. More generally, a delay element may be switchable between $D+1$ different states, where $D \geq 1$. A propagation delay for such a delay element may thereby be varied between a propagation delay of duration τ to $\tau + D \cdot \Delta t$ in discrete steps of size Δt .

In one example, all A delay elements 123 are switchable between $D+1$ states wherein the total propagation delay of the delay line 122 may be changed in discrete steps of the step size Δt from $A \cdot \tau$ to $A \cdot (\tau + D \cdot \Delta t)$. However, it is not a requirement that all A delay elements are switchable between a same number of states. Neither is it a requirement that the difference between a first propagation delay of a first state, and a second propagation delay of a second state is the same for different delay elements. In one example, the delay line 122 may include one switchable delay element 123 ($A=1$), the delay element 123 being switchable between a plurality of states, each successive state increasing the propagation delay of the delay element 123 by the step size Δt . In one example, the delay line 122 may include two delay elements 123, a first delay element being switchable between $D+1$ states, the propagation delay in a state s being $\tau + \Delta t \cdot (s-1)$ (where $1 \leq s \leq D+1$), and a second delay element being switchable between two states of propagation delay τ and $\tau + \Delta t \cdot D$, respectively. The total propagation delay of the delay line 122 may thereby be adjusted between $2 \cdot \tau$ and $2 \cdot \tau + \Delta t \cdot 2 \cdot D$ in

steps of size Δt . More generally, each delay element 123 may be switchable between two or more states, wherein the difference between the propagation delays of any two of the states is equal to one or more units of the step size Δt . Moreover, the delay elements 123 in combination contribute to a total
5 propagation delay of the delay line 122 which may be adjusted in a plurality of steps of size Δt between a minimum total propagation delay and a maximum total propagation delay.

Generally, the system parameters A and τ are preferably determined such that $A \cdot \tau$ corresponds to one or more periods of Ref_clock, i.e. T_{ref} .
10 Alternatively as will be further described below, A and τ may be such that $A \cdot \tau$ corresponds to one or more half periods of Ref_clock, i.e. $T_{\text{ref}} / 2$. Moreover, the step size Δt is preferably smaller than the period of the Ref_clock. Advantageously Δt is determined such that a plurality of units of Δt is required to correspond to the period of Ref_clock. The adjustment range of the delay
15 line 122 preferably meets or exceeds the period time T_{ref} of Ref_clock.

Optionally, the delay line 122 may include an additional, non-switchable, delay element (not shown). The additional delay element may act as a buffer stage arranged at the output of the delay line 122. A buffer stage may in some cases improve the accuracy and predictability of the system 100
20 by providing a well-defined output capacitance for the delay line 122. The buffer stage may for example include an inverter of a same type as the delay elements 123. For corresponding reasons, a buffer stage may also be arranged at the input of the delay line 122. As may be understood, a buffer stage may contribute to the total propagation delay of the delay line 122 by a
25 certain amount. The contribution of a buffer stage to the total propagation delay of the delay line 122 will however in general be constant regardless of the switching states of the delay elements 123 and will therefore, to simplify understanding, be disregarded in the following.

To facilitate understanding of the present inventive concept, it will in
30 the following be assumed that the delay line 122 includes A number of delay elements 123, each being switchable between $D+1$ states. Referring to Fig. 2, the controller 120 is arranged to control the total propagation delay of the delay line 122 by controlling the states of the delay elements 123. The controller 120 may control the delay line 122 using a digital control signal
35 Rx_fine output by the controller 120 and received by the delay line 122. As will be described in more detail below, the controller 120 may include an arithmetic logic unit for determining Rx_fine. Rx_fine may be arranged to

indicate to the delay line 122 which states each delay element 123 should be switched to, i.e. indicate the setting of the states of the delay elements 123. A particular setting of the states of the delay elements 123 may be referred to as a configuration of the delay line 122. The delay line 122 may thus provide
 5 a digital-to-time transfer function, i.e. converting a digital value represented by the digital control signal Rx_fine to a total propagation delay of the delay line 122. The control signal Rx_fine may for example be transmitted to the delay line 122 on a serial or parallel bus. The control of the delay line 122 may be implemented in a number of different ways:

10 In one implementation, Rx_fine may be a digital signal comprising A number of signal portions or components, each of the A signal portions or components indicating for each of the A delay elements 123 the number of units of Δt (i.e. 0 to D) to be added to τ of each delay element 123.

In one implementation, the delay line 122 may comprise a plurality of
 15 digital inputs, one set of inputs per delay element 123, each set comprising D number of inputs wherein a control signal component provided by the controller 120 to each input may control whether an additional propagation delay Δt is to be added to τ of an associated delay element 123. For example, providing a first signal level (e.g. a high level) to d number of the D digital
 20 inputs a delay element 123 and a second signal level (e.g. a low level compared to said high level) to the remaining ($= D - d$) number of digital inputs of the delay element 123 may cause the delay element 123 to add d units of Δt to τ for the delay element 123.

The control signal Rx_fine may be a digital thermometer coded control
 25 signal of $A \cdot D$ bits. A thermometer coded control signal may enable stable and convenient control of the switching of the delay elements 123. In particular, the total propagation delay of the delay line 122 may be increased by Δt by changing the state of only one delay element 123 and thus the value of only one bit of the control signal. Using a thermometer code, the control signal
 30 may comprise A groups of D bits, wherein each group controls the state of a specific delay element 123. For example Rx_fine may have the format

$$\{ [a_1, \dots, a_D]_1, \dots, [x_1, \dots, x_D]_A \}$$

wherein $[a_1, \dots, a_D]_1$ controls the state of the D digital inputs of the delay
 element 123-1 and $[x_1, \dots, x_D]_A$ controls the state of the D digital inputs of the
 35 delay element 123-A.

Alternatively, Rx_fine may be a digital binary coded control signal of $\log_2(A \cdot D)$ bits. Rx_fine may thereby indicate the number of units of Δt to be

added to the total propagation delay of the delay line 122. The delay line 122 may be arranged to control, based on Rx_fine, the states of the delay elements 123 accordingly. For example, the delay line 122 may be arranged to apply a binary-to-thermometer code conversion to Rx_fine wherein a code
5 having the format illustrated in the previous paragraph may be obtained.

Although being referred to as a digital control signal, it is also possible to control the switching of the delay elements 123 using an analog control signal Rx_fine. Rx_fine may for example be an analog signal indicating to the delay line 122 the number of delay elements to be switched to each state
10 using frequency or amplitude modulation. The delay line 122 may include a de-modulator for decoding the information and thereafter control the switching of the delay elements 123 accordingly.

According to one embodiment each one of the delay elements 123 includes a logic circuit element and a variable capacitive load, wherein each
15 delay element is switchable between its respective states by varying a capacitive load of the logic circuit element. The capacitive load may be arranged at the output of the associated logic circuit element. More specifically, the logic circuit elements of the delay elements 123 may be interconnected wherein an interconnection between adjacent logic circuit
20 elements includes the variable capacitive load. By varying the capacitive load for a delay element between two or more levels the delay element may be switched between two or more states, each providing a different propagation delay.

A preferred embodiment of a delay line 322 including delay elements
25 having a variable capacitive load is illustrated in Fig. 3. The delay line 322 may be used as the delay line 122 in the system 100. In the following reference will be made to the delay element 323-1 (corresponding to delay element 123-1), however the discussion applies correspondingly to the further delay elements of the delay line 322. The delay element 323-1 comprises a
30 logic circuit element in the form of an inverter 360. The output of the inverter 360 is connected to an input of an inverter of a subsequent delay element. The delay element 323-1 further comprises a group of one or more varactors, each varactor being switchably connected to the output of the inverter 360. Each varactor and its associated switch (commonly referenced 370) thus
35 forms a variable capacitive load 370 for the inverter 360, which load may be varied between zero (when disconnected) and C (when connected), C being the capacitance of the varactor of the variable capacitive load 370 such that

the propagation delay of the delay element 323-1 is increased by Δt . Each connected varactor may thus increase the time required for the output of the delay element 323-1 to reach a trigger level of the subsequent delay element by Δt . With reference to the previous discussion the number of variable
5 capacitive loads 370 of the delay element 323-1 may be denoted D. According to an alternative arrangement, the switch of each variable capacitive load 370 may instead be arranged between the varactor and ground. In any case, the switches may be controllable by the control signal Rx_fine as described above. For example, the switch connected to each
10 varactor of a variable capacitive load 370 may be controlled based on a signal received at an associated digital input of the delay line 322.

The delay element 323-1 further comprises a varactor 380 which is permanently connected to the output of the inverter 360. When the switch of each of the D variable capacitive loads 370 is open, the propagation delay of
15 the delay element 323-1 (denoted τ) is defined by the propagation delay of the inverter 360 and the capacitance of the varactor 380. The varactor 380 thus enables the propagation delay τ of the delay element 323-1 to be tuned within a range $\tau_{\min}$ to $\tau_{\max}$ determined by the limits of the tuning range of the varactor 380. This tuning may for example be used for calibrating the delay
20 line 323, as will be described below. In case tuning is not necessary the varactor 380 may be omitted wherein the propagation delay τ of the delay element 323-1 will be defined by the propagation delay of the inverter 360.

The varactors of the delay element 323-1 may for example be varactor diodes, MOSFET varactors, Schottky-diode varactors. These types of
25 varactors allow the capacitance to be varied by controlling the depletion region. A further example is a MEMS varactor wherein the capacitance may be varied by mechanically adjusting the separation between the capacitor plates by controlling an electrical field applied to the varactor. Implementing the capacitive loads using varactors provides the advantage of enabling the
30 capacitive loads (e.g. C) to be tuned. Thus, Δt provided by each variable capacitive load 370 may be tuned within a range $\Delta t_{\min}$ to $\Delta t_{\max}$ determined by the limits of the tuning range of the varactors. This may improve the flexibility of the delay line 322 by introducing further degrees of freedom. This tuning may
35 for example be used for calibrating the delay line 323, as will be described below. Varactors may also allow post-manufacturing adjustment to ensure that Δt is substantially constant throughout the adjustment range of the total propagation delay of the delay line 322. However, if such tunability is not

required a variable capacitive load capacitive load may also be provided by one or more capacitors having fixed and well-defined capacitances and being switchably connected to the output of the inverter 360. Additionally, as discussed above, other types of logic circuit elements may be used instead of the inverter 360.

Although in Fig. 3 all delay elements includes a group of D number of varactors having a same capacitance C , other arrangements are also possible. For example a delay element 323-1 may include a switchably connected varactor/capacitor of capacitance C , a delay element 323-2 may include a switchably connected varactor/capacitor of capacitance $2 \cdot C$ or two parallel varactors/capacitors of capacitance C connected to the output of the associated inverter via a same switch, and so on up to a delay element 323-A including a switchably connected varactor/capacitor of capacitance $2^{(A-1)} \cdot C$ or $2^{(A-1)}$ parallel varactors/capacitors of capacitance C connected to the output of the associated inverter via a same switch. The total propagation delay of such a delay line would be controllable using a binary coded control signal, each bit position controlling the state of the switch for a respective delay element.

According to an alternative embodiment of a delay line, a delay element may be switched between its respective states by varying a capacitive load of the logic circuit element by varying the capacitance of a controllable varactor between at least a first capacitance C_1 a second capacitance C_2 ($C_2 > C_1$). A variable capacitive load may thus be arranged without using switches. With reference to the previous discussion each delay element may for example include D number of such controllable varactors. Each delay element may thereby be switched between $D+1$ different states.

With reference to Fig. 2, according to an alternative embodiment each one of the delay elements 123 comprises a logic circuit element and is arranged to be switchable between its respective states by varying a current supplied to the logic circuit element. By varying the current supplied to a logic circuit element of a delay element between two or more levels the delay element may be switched between two or more states, each providing a different propagation delay.

A preferred embodiment of a delay line 422 including delay elements being switchable by varying the supply current is illustrated in Fig. 4. The delay line 422 may be used as the delay line 122 in the system 100. In the following reference will be made to the delay element 423-1 (corresponding to delay element 123-1), however the discussion applies correspondingly to the

further delay elements of the delay line 422. The delay element 423-1 comprises an inverter 460 and a group of D number of current limiting transistors 470a and 470b arranged in pairs and being arranged to vary a charge and discharge current, respectively of the inverter 460 by limiting the current supplied to the inverter 460. Each pair of current limiting transistors 470a and 470b is switchable between a state in which the current limiting transistor limits the current of the inverter 460 to a non-zero value and a state in which the current limiting transistor does not supply a current to the inverter 460. In Fig. 4 a respective switch is arranged between an associated current limiting transistor 470a and ground, however a same function may also be provided by arranging the switch between the current limiting transistor 470a and the inverter 460. This is also the case for the current limiting transistor 470b and respective switch. The delay element 423-1 further comprises a current limiting transistor 480a and 480b arranged to limit the current of the inverter 460. The current limiting transistor 480a and 480b are permanently connected to the inverter 460.

As may be understood by the person skilled in the art, in the circuit implementation illustrated in Fig. 4 the current limited by the current limiting transistors 470a and 480a may control the fall time of the output of the inverter 460 and thus only the output high-to-low propagation delay of the inverter 460. Correspondingly, the set of current limiting transistors, 480b and 470b, may control the rise time of the output of the inverter 460, which corresponds to the output low-to-high propagation delay. Preferably, the current limiting transistors 470a and 470b may be connected in D pairs such that the propagation delay of the delay element 423-1 is independent of rising or falling edge propagation. However, the implementation is not limited by using both current limiting transistors 470a and 470b or that they are controlled in pairs.

In a first state of the delay element 423-1, each current limiting transistor 470a and 470b may be connected to the inverter 460. In the first state, the sum of currents of the current limiting transistors 470a and 480a respectively 470b and 480b are arranged such that the propagation delay for the delay element 423-1 is τ . Preferably, the sum of currents supplied to the inverter 460 by the current limiting transistor 470a (i.e. when connected) and the current limiting transistor 480a respectively the current limiting transistor 470b (i.e. when connected) and the current limiting transistor 480b is such that the inverter 460 operates in a regime where the charge/discharge current

is mainly limited by the inverter 460. By disconnecting the current limiting transistors 470a and 470b in a pair wise manner, one pair after another, the inverter 460 may enter an (increasingly) current limited regime. More specifically, by disconnecting one pair of the current limiting transistors 470a and 470b (and thus switching the delay element 423-1 to a different state) the total current supplied to the inverter 460 will decrease by an amount equal to the current limited by the disconnected pair of current limiting transistors 470a and 470b. The decrease in current supplied to the inverter 460 is such that the propagation delay of the inverter 460, and thus the delay element 423-1 is increased by Δt . By controlling the number of current limiting transistors 470a and 470b pairs supplying current to the inverter 460 the propagation delay for the delay element 423-1 may thus be varied between τ and $\tau + D \cdot \Delta t$. The state of each current limiting transistor pair 470a and 470b may be controllable by the control signal Rx_fine as described above. For example, the switch connected to each current limiting transistor pair 470a and 470b may be controlled based on a signal received at an associated digital input of the delay line 422.

Analogous to the discussion in connection with Fig. 3, all delay 423 elements need not include a same number of current limiting transistors. For example, similar to the varactors above, a delay element 323-i may include $2^{(i-1)}$ parallel current limiting transistors, each limiting the current supplied to the inverter by an amount increasing the propagation delay by Δt .

The limiting current of the current limiting transistors 470a and 470b may be tunable. Implementing the current limiting transistors 470a and 470b as controlled current limiters provides the advantage of enabling the limited current to be tuned. This may improve the flexibility of the delay line 422 by introducing further degrees of freedom. It may further enable analog calibration of the delay line 422 as will be described in detail below. Controlled current limiting transistors may also allow post-manufacturing adjustment to ensure that Δt is substantially constant throughout the adjustment range of total propagation delay of the delay line 422. The controlled current limiting transistors 470a and 470b may for example be implemented as current mirrors. Also the current limiting transistors 480a and 480b may have a tunable limiting current. Advantages of arranging also the current limiting transistors 480a and 480b with a tunable limiting current may be understood from the below. However, the current limiting transistor with tunable limiting current may be implemented using other types of current

limiting devices such as tunable resistors. Additionally, as discussed above, other types of logic circuit elements may be used instead of the inverter 460.

Furthermore, the propagation delay of a delay element may also be controlled by controlling the voltage supplied to a logic circuit element of the delay element. The level of the supply voltage may be generated by a configurable low drop-out regulator to both generate a voltage which corresponds to current limiting transistor pair 480a and 480b, and voltages corresponding to the switchable current limiting transistor pair 470a and 470b.

In the above, reference has been made to the parameters A , τ , D and Δt . As will be understood by a person skilled in the art the actual values of A , τ , D and Δt are design choices which may vary for different implementations and applications of the system 100. As a non-limiting example applicable for mm-wave applications, the propagation delay of logic circuit element of a delay element 123, 323, 423 (e.g. an inverter) may be in the range of 15 to 30 picoseconds and the step size of Δt in the range of 0.5 to 10 picoseconds. Further, if, for example, the number of delay elements A is 10 and the number of switchable states $D+1$ of each delay elements is 20, each state adding Δt to the propagation delay of the delay element 123, 323, 423, the total propagation delay of the delay line 122, 322, 422 would be adjustable between 200 picoseconds and 400 picoseconds.

Returning to Fig. 2, the timing circuitry 118 may further comprise trigger circuitry, which in Fig. 2 is represented by the trigger circuit 124 and the trigger circuit 126. The trigger circuit 124 is arranged to receive the delayed reference clock signal from the delay line 122 and output the trigger signal Rx_trigg after a configurable integer number of periods Rx_coarse of the delayed reference clock signal. As may be understood from the above the period of the delayed reference clock signal output from the delay line 122 is T_{ref} . The number of periods Rx_coarse may be controlled by the controller 120. The controller 120 may for example provide a digital signal indicating the value of Rx_coarse in a binary format to a digital input Rx_coarse of the trigger circuit 124. The value of Rx_coarse may be recorded in a register of the trigger circuit 124. The trigger circuit 124 may further include a counter which is incremented by one in response to receiving a rising or falling edge of the delayed reference clock signal. The trigger circuit 124 may be arranged to output the Rx_trigg signal in response to the counter being equal to Rx_coarse . The trigger circuit 124 may further include a reset input $Reset$ enabling the controller 120 to reset the counter of the trigger

circuit 124 to zero by providing a first predetermined control signal. The trigger circuit 124 may further be arranged to be unresponsive to received clock signals for a duration of the reset control signal. The trigger circuit 124 may be arranged to become responsive to received clock signals in response to the controller 120 providing a second predetermined control signal to the reset input Reset. The Reset input may hence be used to control the repetition frequency of the wavelet generation (i.e. the pulse repetition frequency).

As illustrated in Fig. 2 the system 100 may further comprise a trigger circuit 126 arranged to receive the reference clock signal Ref_clock and output the trigger signal Tx_trigg after a configurable number of periods Tx_coarse of the reference clock signal Ref_clock. The control signal Tx_coarse may be transmitted to the trigger circuit 126 on a serial or a parallel bus. The description of the trigger circuit 124 applies correspondingly to the trigger circuit 126 and will therefore not be repeated.

By the delay line 122, the trigger circuit 124 and the additional trigger circuit 126 a delay between (i.e. a relative timing of) the output of Tx_trigg and the output of Rx_trigg may be controlled by the controller 120. More specifically the delay may be controlled in a digital manner. In particular the timing difference may be expressed as:

$$(Eq. 1) \quad \text{Delay} = (Rx_coarse - Tx_coarse) * T_ref + Rx_fine * \Delta t + A * \tau$$

The controller 120 may include a calculation unit arranged to determine the variables Rx_coarse, Tx_coarse and Rx_fine based for a desired value of Delay provided to the controller 120 and the parameters τ , Δt and A. The system 100 thus enables changes to the delay between a transmission of a wavelet and a generation of a reference wavelet which are greater than T_ref to be achieved by the controller 120 varying Tx_coarse and/or Rx_coarse. Meanwhile, changes which are smaller than T_ref may be achieved by the controller 120 varying Rx_fine. The trigger circuitry formed by the trigger circuits 124 and 126 thus provides a “coarse delay control” with a step size or resolution of T_ref. Meanwhile the delay line 122 provides a “fine delay control” with a step size or resolution of Δt .

In an alternative embodiment, an analogous function may be obtained if the delay line 122 is arranged to output the delayed reference clock signal to the trigger circuit 126 instead of to the trigger circuit 124. In a further

alternative embodiment, the trigger circuitry formed by the trigger circuit 124 and 126 may be omitted from the timing circuitry 118 wherein the first and second pulse generators 114 and 116 may be arranged to output P_tx and P_rx, respectively, in response to receiving the reference clock signal Ref_clock and the delayed reference clock signal output by the delay line 122, respectively. In such an embodiment the reference clock signal Ref_clock and the delayed reference clock signal may function as trigger signals for the generation of a transmit wavelet and a reference wavelet. This embodiment may be used in applications where delay adjustment range of the delay line 122 meets the maximum delay requirements for the application. In a further alternative embodiment the trigger circuit 124 may be arranged before the delay line 122 and thus be arranged to receive the reference clock signal Ref_clock and output the trigger signal Rx_trigg to the delay line 122. The delay line 122 may thus be arranged to receive Rx_trigg at the input of the delay line 122 and transmit Rx_trigg at the output of the delay line 122 after the total propagation delay of the delay line. The second pulse generator 126 may further be arranged to output P_rx in response to receiving Rx_trigg from the delay line 122.

Optionally, a tap may be arranged at the output of the trigger circuit 124 for providing the trigger signal ADC_trigg for triggering an ADC to sample and digitize the output W_int from the correlator circuit 111.

Alternatively, or additionally, the trigger circuits 124 and 126 may be arranged to count a number of both rising and falling edges of the received clock signal. For a reference clock signal having a duty cycle of 50 % this enables trigger circuits 124 and 126 to output the trigger signals Tx_trigg and Rx_trigg after a configurable number of half periods of length $T_{ref} / 2$. If the trigger circuits 124 and 126 are arranged to count both rising and falling edges the term T_{ref} in Eq. 1 should be replaced by $T_{ref} / 2$.

An example describing the system 100 in a measurement mode of operation will now be given with reference to Figs 5-7. The trigger signals Tx_trigg and Rx_trigg triggers the first and the second pulse generators 114, 116 wherein a first and a second pulsed signal P_tx and P_rx are generated. The delay between P_tx and P_rx is given by Eq. 1 and is configured by the controller 120 determining values of Rx_coarse, Tx_coarse and Rx_fine to obtain the desired delay ("Delay" in Eq. 1). P_tx triggers the first wavelet generator 104 to generate a wavelet W_tx for transmission by the transmitter 102. After reflection by one or several objects the wavelet may be received by

the second antenna 112 of the receiver 108. The output of the antenna 112 W_{rx} is coupled to the correlator circuit 111 and mixed with a reference wavelet W_{ref} received from the second wavelet generator 110. The mixed signal W_{mix} may then be provided to the integrator. As described above the integrated signal W_{int} may be sampled by an ADC and supplied to a DSP for further processing. These steps may be repeated for a plurality of different delays between the transmission of a wavelet W_{tx} and the generation of a reference wavelet W_{ref} to determine a set of correlations. Identical delays may be used for more than one measurement to enable averaging of W_{rx} , W_{mix} and/or W_{int} and increase the SNR for a certain delay. The delay for which W_{int} is maximum corresponds to the time of flight of a transmitted wavelet (W_{tx}), then reflected and thereafter received wavelet (W_{rx}).

Fig 6 illustrates a received signal in a situation where two objects are present within the range of the system 100. Fig. 7 illustrates a set of correlations resulting from mixing and integrating the received signal in Fig. 6 with a reference wavelet W_{ref} for a plurality of different delays between W_{tx} and W_{ref} . The set of correlations are shown as a function of an integer X , representing the relative delay between W_{ref} and W_{tx} in units of Δt (or analogously the relative delay between Tx_trigg and Rx_trigg). The two reflections may be individually identified if they are separated by at least the wavelet length (which may be controlled by the duration of P_{tx} , i.e. Ptx_dur as described above). The algorithm which may describe the process of retrieving the set of correlations in Fig. 7 may be described as a two level nested loop function. The X -value corresponds to the delay setting Delay of ALU 850, where the Delay equal to zero may correspond to Tx_coarse , Rx_coarse , and Rx_fine all equal to zero as an example. Further, the Delay equal to one may correspond to Rx_fine equal to one while Tx_coarse and Rx_coarse are still zero. After each correlation, Delay may be increased by one step which will affect the Rx_fine value, such that for each stepwise increase of Delay the Rx_fine value may also increase stepwise. However, when Rx_fine has reached its maximum value (i.e. when the total propagation delay of the delay line is maximized), it is reset to zero while Rx_coarse is increased one step. This is repeated until the Delay has reached the maximum X -value found in Fig. 7.

Although the system 100 in the above has been described in the context of a range-finding or radar application the system 100 may also be used in other contexts. For example the system 100 may be used for

detecting proximity of an object by fixing the delay between to a specific value and monitor for a correlation between the reference wavelet and a received wavelet exceeds a predetermined threshold value, thus indicating that an object reflecting the transmitted wavelet is present at a distance

5 corresponding to the specific delay value.

As may be understood from the above, the system 100 provides two independently controllable mechanisms of adjusting a relative timing of the Tx_trigger signal and the Rx_trigger signal: a coarse delay control controlling Tx_coarse and Rx_coarse and a fine delay control controlling Rx_fine.

10 Preferably, the system 100 is arranged such that the adjustment range of the fine delay control, i.e. the adjustment range of the total propagation delay of the delay line 122 (or 322 or 422) (or synonymously the dynamic range of the delay line) corresponds to at least one period of Ref_clock of length T_{ref} (or if applicable $T_{ref} / 2$). A lower end point of the adjustment
15 range (e.g. the minimum value of the total propagation delay of the delay line 122, i.e. $A * \tau$) is preferably such that the reference clock signal is delayed by an integer number of periods of Ref_clock (i.e. T_{ref} or if applicable $T_{ref} / 2$). An upper end point of the adjustment range (e.g. the maximum value of the total propagation delay of the delay line 122, i.e. $A * \tau + A * D * \Delta t$) preferably
20 differs from the lower end point by T_{ref} (or if applicable $T_{ref} / 2$). During design of the system 100 the parameters A , τ , D and Δt and the frequency of the reference clock signal Ref_clock may be chosen such that the desired lower and upper end points are obtained.

In some cases it may be difficult to accurately determine these
25 parameters during design and construction such that the above-mentioned preferred characteristics of the system 100 and the delay line 122 are obtained. For example temperature variations or inaccuracies during manufacturing may result in deviations. Consequently, in some cases the digital-to-time transfer function provided by the timing circuitry 118 may have
30 overlaps or gaps. An "overlap scenario" may result when the dynamic range of the delay line 122, 322 or 422 is greater than the period time T_{ref} (or $T_{ref} / 2$). A same delay ("Delay" in Eq. 1) between W_{tx} and W_{ref} may thus be obtained for different settings of Tx_coarse and Rx_coarse. This may result in redundant data points and an increased measurement time.
35 Conversely, a "gap scenario" may be exhibited when the dynamic range of the delay line 122, 322 or 422 is smaller than T_{ref} (or $T_{ref} / 2$). This may result in loss of data points since the digital-to-time transfer function provided

by the timing circuit 118 will have discontinuities with unknown width. In the following embodiments will be described which address these matters.

An embodiment of an analog calibration of a delay line will now be described with reference to Fig. 8. In Fig. 8 elements 818-826 correspond to
 5 elements 118-126 in Figs 1 and 2. The controller 820 is arranged to, during a calibration mode, enter a first operational state (a first stage of the calibration) and set each switchable delay element of the delay line 822 to a respective first state in which each delay element presents a first propagation delay. In particular, the first state of each delay element may be the state for which the
 10 delay element presents its minimum propagation delay (e.g. which in line with the above discussion may be τ). The controller 820 is further arranged to, during a one or more periods or half periods of the reference clock signal Ref_clock, tune the first propagation delay of each delay element until a total propagation delay of the delay line 822 corresponds to an integer number of
 15 periods I_1 of Ref_clock (or half periods of Ref_clock).

The controller 820 is further arranged to enter a second operational state (a second stage of the calibration) and set each switchable delay element to a respective second state in which each delay element presents a second propagation delay. In particular, the second state of each delay
 20 element may be the state for which the delay element presents its maximum propagation delay (e.g. which in line with the above discussion may be $\tau + D * \Delta t$), or at least a propagation delay which is greater than the first propagation delay of the delay element. The controller 820 is further arranged to, during one or more periods or half periods of Ref_clock, tune the second
 25 propagation delay of each delay element (e.g. which in line with the above discussion may include tuning Δt) until the total propagation delay of the delay line 822 corresponds to an integer number of periods I_2 ($I_2 > I_1$, preferably $I_2 = I_1 + 1$) of Ref_clock (or half periods of Ref_clock). The calibration is then complete wherein the controller 820 may start operating in accordance with a
 30 measurement mode. In other words, by the calibration a first total propagation delay of the delay line 822 may be tuned to correspond to I_1 periods or half periods of Ref_clock and a second total propagation delay of the delay line 822 may be tuned to correspond to I_2 periods or half periods of Ref_clock.

As illustrated in Fig. 8 the controller 820 includes a phase
 35 comparator 840. The phase comparator 840 is arranged to determine a phase difference between Ref_clock and Delay_ref. The phase comparator 840 may receive Ref_clock and Delay_ref at a respective input

and output a signal representing the determined phase difference. If Ref_clock lags Delay_ref the phase comparator 840 may determine a positive phase difference and if Ref_clock leads Delay_ref the phase comparator may determine a negative phase difference, however the opposite function is also possible. The phase comparator 840 may be an analog phase comparator, a digital phase comparator or a phase frequency detector arranged to output a (possibly low-pass filtered) signal with a voltage proportional to the determined phase difference. As a further example, the phase comparator 840 may include a sampling circuit for (while keeping a propagation delay of each delay element of the delay line 822 constant) sampling Ref_clock and Delay_ref during one or more periods of Ref_clock and calculate a phase difference between the sampled clock signals. The calculated phase difference may be converted to a corresponding analog signal using a digital-to-analog converter and thereafter be output by the phase comparator 840.

In an alternative embodiment wherein the input of the delay line 822 is connected to the output of the trigger circuit 824 the timing circuitry 818 may include a signal path arranged in parallel with the trigger circuit 824 and allowing Ref_clock to by-pass the trigger circuit 824 during the calibration mode. The signal path may for example include a switch which may be opened by the controller 820 during a measurement mode and closed by the controller 820 during a calibration mode.

Returning to Fig. 8, the controller 820 comprises a first controlled voltage source 842 arranged to output a first control signal v_{offset} and a second controlled voltage source 844 arranged to output a second control signal v_{slope} . The delay line 822 comprises corresponding inputs for receiving v_{offset} and v_{slope} from the controller 820. As will be described in detail below, v_{offset} and v_{slope} may be used for tuning the total propagation delay of the delay line 822. In Fig. 8 the phase comparator 840 is connected to both voltage sources 842 and 844. However, it would be equally possible to provide a first phase comparator having an output connected to the voltage source 842 and a second phase comparator having an output connected to the voltage source 844. The voltage source 842 may operate in a first mode and a second mode. In the first mode the voltage source 842 is arranged to keep the output voltage of v_{offset} constant. In the second mode the voltage source 842 is arranged to vary the output voltage of v_{offset} based on the voltage of the signal received from the phase comparator 840.

The controlled voltage source 844 is arranged in a manner analogous to the voltage source 842 however in relation to v_{slope} instead of v_{offset} .

The phase comparator 840 may instead of being arranged to output a voltage proportional to the phase difference between Ref_clock and Delay_ref be arranged to output a first predetermined signal if the phase difference is positive, a second predetermined signal if the phase difference is negative and a third predetermined signal if the phase difference is zero (or deviates from zero by less than a threshold value). The predetermined signals may for example present different and predetermined DC voltages. The controlled voltage source 842 may include a charge pump and a sample and hold circuit. An input of the charge pump may be connected to the output of the phase comparator 840. An output of the charge pump may be connected to the sample and hold circuit. The charge pump may be arranged to output a decreasing voltage in response to receiving the first predetermined signal, an increasing voltage in response to receiving the second predetermined signal and a constant voltage in response to receiving the third predetermined signal. In the first mode, the sample and hold circuit outputs v_{offset} at a voltage which tracks the voltage of the signal received from the charge pump. In the second mode the sample and hold circuit stops tracking the voltage of the signal received from the charge pump and keeps the output voltage of v_{offset} constant. The voltage source 844 may be arranged in a corresponding manner in relation to v_{slope} .

If the trigger circuits 824 and 826 are arranged to count a number of rising or falling edges of a clock signal (thus effectively counting a number of periods of the clock signal) the voltage source 842 and the voltage source 844 may, in its second mode, be arranged to control the voltage of v_{offset} and v_{slope} , respectively, to achieve a phase difference between Ref_clock and Delay_ref which corresponds to zero degrees (or deviates from zero by less than a threshold). The voltage source 842 and 844 may for example be arranged to determine a voltage level of a signal received from the phase detector 840 and reduce the voltage of v_{offset} and v_{slope} , respectively, in response to the determined voltage level indicating a positive phase difference and increase the voltage of v_{offset} and v_{slope} , respectively, in response to the determined voltage level indicating a negative phase difference.

Alternatively, if the trigger circuits 824 and 826 are arranged to count both rising and falling edges of a clock signal (thus effectively counting a

number of half periods of the clock signal), the voltage source 842 may, in its second mode, be arranged to control the voltage of v_{offset} to achieve a phase difference between Ref_clock and Delay_ref which corresponds to zero degrees (or deviates from zero by less than a threshold). The voltage source 844 may, in its second mode, be arranged to change the voltage of v_{slope} to achieve a phase difference between Ref_clock and Delay_ref which corresponds to 180 degrees (e.g. deviates from 180 degrees by less than a threshold). Alternatively, the voltage source 842 may be arranged to change the voltage of v_{offset} to achieve a phase difference which corresponds to 180 degrees and the voltage source 844 may be arranged to change the voltage of v_{slope} to achieve a phase difference which corresponds to zero degrees. Other variations are also possible. For example the phase comparator 840 may in the first stage of the calibration be arranged to output a signal representing a deviation of the phase difference from zero and in the second stage of the calibration be arranged to output a signal representing a deviation of the phase difference from 180 degrees, or vice versa.

The controller 820 further comprises a calibration control block CCB 846 which is arranged to, during the calibration mode, control the operations of the controller 820. More specifically the CCB 846 is arranged to control whether v_{offset} (in the first operational state) or v_{slope} (in the second operational state) should be controlled based on the phase difference determined by the phase comparator 840. In the first operational state the CCB 846 may cause the voltage source 842 to operate in its second mode and the voltage source 844 to operate in its first mode. In the second operational state the CCB 846 may cause the voltage source 842 to operate in its first mode and the voltage source 844 to operate in its second mode. The mode of the voltage source 842 may for example be controlled by a control signal Cal_offset output by the CCB 846. Analogously, the mode of the voltage source 844 may for example be controlled by a control signal Cal_slope output by the CCB 846. Cal_offset and Cal_slope may for example be digital control signals wherein a first signal level causes the voltage source 842 and 844, respectively, to operate in its first mode and a second signal level causes the voltage source 842 and 844, respectively, to operate in its second mode.

The controller 820 may further comprise a calculation unit 848 arranged to determine and output the control signals Rx_fine , Rx_coarse and

Tx_coarse having the respective functions described in connection with Fig. 2. In response to entering the first operational state of the controller 820, the calculation unit 848 is arranged to output a control signal Rx_fine such that each switchable delay element of the delay line 822 is set to its
5 respective first states for the duration of the first operational state. In response to entering the second operational state of the controller 820, the calculation unit 848 is arranged to output a control signal Rx_fine such that each switchable delay element of the delay line 822 is set to its respective second state for the duration of the second operational state. In the
10 calibration mode the CCB 846 may for example provide a first predetermined signal (e.g. a signal having a first predetermined voltage) to the computation unit 848 to indicate entry into the first operational state and a second predetermined signal (e.g. a signal having a second predetermined voltage) to indicate entry into the second operational state. Advantageously, during the
15 calibration mode the computation unit 848 may be arranged to output a reset signal Reset to the trigger circuits 824 and 826, causing their counters to be reset and causing the trigger circuits 824 and 826 to become unresponsive to any received clock signals for the duration of the calibration.

To determine when the first and the second stages of the calibration is
20 complete the controller 820 may implement lock detection. For example, as illustrated in Fig. 8 the phase comparator 840 may be arranged to transmit a lock detection signal LD to the CCB 846 in response to the phase difference between Ref_clock and Delay_ref falling below a predetermined threshold. In response to receiving the lock detection signal LD for a first time during the
25 calibration mode the CCB 846 may cause the controller 820 to transition from the first operational state to the second operational state. In response to receiving the lock detection signal for a second time during the calibration mode the CCB 846 may cause the controller 820 to finish the calibration mode and transition into a measurement mode. The lock detection may
30 however also be implemented directly in the CCB 846. The CCB 846 may for example be arranged to monitor an amplitude of an oscillation of the output of the phase comparator 840 or of v_offset (i.e. in the first operational state) and v_slope (i.e. in the second operational state) as output by the voltage sources 846 and 844, respectively.

35 According to one embodiment the delay line 822 may be implemented in a same manner as the delay line 322 however with the addition of respective inputs for receiving the control signals v_offset and v_slope from

the controller 820. A control terminal of each varactor 380 may be connected to the v_offset input of the delay line 822 wherein the voltage of v_offset may tune the capacitance of the varactor 380 and thus tune a first propagation delay of each delay element (e.g. which in line with the above discussion may be τ). A control terminal of each varactor of the variable capacitive loads 370 of each delay element may be connected to the v_slope input of the delay line 822 wherein the voltage the voltage of v_slope may tune the capacitance of all varactors of the variable capacitive loads 370 and thus tune a second propagation delay of each delay element (e.g. which in line with the above discussion may be $\tau + D * \Delta t$). In the first operational state, the controller 820 may open the switch of each variable capacitive load 370 of each delay element (e.g. using the control signal Rx_fine). The voltage source 842 of the controller 820 may thereafter tune the first propagation delay of each delay element by controlling the voltage of v_offset until the desired phase relation between Ref_clock and $Delay_ref$ is achieved. In the second operational state, the controller 820 may close the switch of each variable capacitive load 370 of each delay element (e.g. using the control signal Rx_fine). The voltage source 844 of the controller 820 may thereafter tune the second propagation delay of each delay element by controlling the voltage of v_slope until the desired phase relation between Ref_clock and $Delay_ref$ is achieved.

In an alternative embodiment, each delay elements of the delay line 822 need not include a varactor 380. Instead the delay line 822 may include an additional delay element including an inverter similar to the inverter 360 (or some other type of logic circuit element) and a varactor (similar to the varactor 380) connected to the output of the inverter. A control terminal of the varactor of the additional delay element may be connected to the v_offset input of the delay line 822 wherein the capacitance of the varactor and thus the propagation delay of the additional delay element may be tuned by controlling v_offset . In response to initiating the calibration, the controller 820 may enter a first operational state and open the switch of each variable capacitive load 370 as described above. The voltage source 842 of the controller 820 may thereafter tune the capacitance of the varactor of the additional delay element by controlling the voltage of v_offset until the desired phase relation between Ref_clock and $Delay_ref$ is achieved. The controller 820 may thereafter proceed in accordance with the second operational state described in the preceding paragraph.

According to one embodiment the delay line 822 may be implemented in a same manner as the delay line 422 however with the addition of respective control terminals (i.e. inputs) for receiving the control signal v_{offset} and v_{slope} from the controller 820. The discussion of the calibration of the delay line 322 in the above applies correspondingly to the present embodiment. However, instead of tuning the capacitance of varactors, v_{offset} may tune the current limited by the transistors 480a and 480b of each delay element and v_{slope} may tune the current limited by the transistors 470a and 470b of each delay element (i.e. the current limited when associated switches of the transistors 470a and 470b are closed).

Calibrating the delay line 822 in accordance with any of the above embodiments enables an accurate control of the step size Δt . A short and well-defined Δt allows, among others, for high accuracy estimation of distances to objects. An estimate of the step size Δt of the delay line 822 (and thus the step size of the digital-to-timing transfer function provided by the timing circuitry 818) may be obtained as $T_{\text{ref}} / (A \cdot D)$ or $T_{\text{ref}} / (A \cdot D \cdot 2)$. More generally, the step size may be determined by dividing T_{ref} or $T_{\text{ref}} / 2$ by the total number of steps in which the total propagation delay of the delay line 822 may be changed. Additionally, the calibration enables the linearity of the control over the delay between a transmitted wavelet and a reference wavelet to be improved and the digital-to-time transfer function provided by the timing circuit 818 to be improved since the difference between the dynamic range of the delay line 822 and the period time T_{ref} or $T_{\text{ref}} / 2$ may be minimized.

In the above embodiments the controller 820 is advantageously arranged to, in the first operational state, open each switch of each variable capacitive load 370 (or close each switch associated with each transistor 470a, 470b) of each delay element of the delay line 822 and, in the second operational state, close each switch of each variable capacitive load 370 (or open each switch associated with each transistor 470a, 470b) to thereby maximize the number of steps in which the total propagation delay of the delay line 822 may be adjusted between $I_1 \cdot T_{\text{ref}}$ and $I_2 \cdot T_{\text{ref}}$ (or $I_1 \cdot T_{\text{ref}} / 2$ and $I_2 \cdot T_{\text{ref}} / 2$), and thus minimize the step size. However if a minimum step size not is critical in a particular application it is in principle possible to open and close only a subset of the switches of the delay elements during the first and second operational state, respectively, without departing from the principles of the analog calibration.

In the above the control signals v_{offset} and v_{slope} have been described as analog control signals. However alternative implementations are also possible. For example, the controller 820 need not include the first and second controlled voltage sources 842 and 844. Instead, the controller 820
5 may directly output the signal representing the phase difference between Ref_clock and Delay_ref to the delay line 822. The delay line 822 may include circuitry providing a same functionality as the voltage sources 842 and 844, as described above. The controller 820 may additionally provide a control signal indicating to the delay line 822 (e.g. using a first and second
10 predetermined voltage level) whether the varactors 370 or 380 (or transistors 480a, b or 470a, b) should be controlled based on the phase difference.

According to one embodiment an overlap or gap scenario may be addressed using, what may be referred to as, a digital calibration of a delay line. An embodiment of a digital calibration of a delay line will now be
15 described with reference Fig. 9. In Fig. 9 elements 918-940 correspond to elements 818-840 in Fig. 8. The controller 920 is arranged to, during a calibration mode, enter a first operational state (a first stage of the calibration) and determine a first setting of the states of the switchable delay elements of the delay line 922 such that the first setting results in a total propagation delay
20 of the delay line 922 which corresponds to a first integer number I_1 of periods of Ref_clock (or half periods of Ref_clock). The controller 920 is further arranged to enter a second operational state (a second stage of the calibration) and determine a second setting of the states of the switchable delay elements of the delay line 922 such that the second setting results in a
25 total propagation delay of the delay line 922 which corresponds to a second integer number I_2 of periods of Ref_clock (or half periods of Ref_clock) ($I_2 > I_1$, preferably $I_2 = I_1 + 1$).

In line with the above discussion the first setting may correspond to a first value or configuration of Rx_fine and the second setting may correspond
30 to a second value or configuration of Rx_fine . By varying Rx_fine between the first value and the second value the total propagation delay of the delay line 922 may thus be adjusted between a first end point corresponding to I_1 periods of Ref_clock (or half periods of Ref_clock) and a second end point corresponding to I_2 periods of Ref_clock (or half periods of Ref_clock).
35 Overlaps or gaps in the digital-to-time transfer function provided by the timing circuitry 918 may thus be avoided by varying Rx_fine between and not beyond the first and second end points.

As may be understood a calibration in accordance with the above is particularly efficient if used in combination with a delay line which is configurable to provide a plurality of different total propagation delays, ranging from a minimum total propagation delay (e.g. which in line with the previous discussion may be $A \cdot \tau$) to a maximum total propagation delay (e.g. which in line with the previous discussion may be $A \cdot D \cdot \Delta t$) and being adjustable between the minimum and maximum propagation delay in a plurality of steps of equal size (e.g. of size Δt), and wherein the minimum total propagation delay is smaller than $I_1 \cdot T_{\text{ref}}$ (or $I_1 \cdot T_{\text{ref}} / 2$) and the maximum total propagation delay is greater than $I_2 \cdot T_{\text{ref}}$ (or $I_2 \cdot T_{\text{ref}} / 2$).

After calibration, an estimate of the step size Δt may be obtained by dividing the T_{ref} (or $T_{\text{ref}} / 2$) by the number of steps in which the total propagation delay of the delay line 922 may be adjusted between the determined first and the second end points of the adjustment range. A maximum error of this estimate will be Δt .

In the first (and the second) operational state of the calibration mode, the controller 920 is advantageously arranged to repeatedly determine a phase difference between Ref_clock and Delay_ref and change the states of one or more delay elements of the delay line 922 until the determined phase difference differs from zero by less than a threshold. If calibrating in relation to half periods of Ref_clock, the controller 920 may in its first operational state change the states of one or more delay elements of the delay line 922 until the determined phase difference differs from zero (or 180 degrees) by less than a threshold, and in its second operational state change the states of one or more of the delay elements of the delay line until the determined phase difference differs from 180 degrees (or zero degrees) by less than a threshold. The phase difference is determined by a phase comparator 940, similar to the phase comparator 840.

Instead of the voltage sources 842 and 844, the controller 920 comprises a first counter 942 and a second counter 944. The first counter 942 may operate in a first mode and a second mode. The first counter 942 includes a register storing the value of a count variable Rx_fine_start. The first counter 942 is arranged to output a signal representing the currently stored value of Rx_fine_start to the calculation unit 946 of the controller 920. In the first mode the first counter 942 is arranged to maintain the current value of Rx_fine_start. In the second mode the first counter 942 is arranged to increase or decrease the value of Rx_fine_start based on the phase

difference between Ref_clock and Delay_ref. The second counter 944 is arranged in a manner analogous to the first counter 942 however includes a register storing the value of a count variable Rx_fine_stop.

5 If the trigger circuits 924 and 926 are arranged to count a number of rising or falling edges of a clock signal (thus effectively counting a number of periods of the clock signal) the phase comparator 940 may be arranged to output a first predetermined signal in each period (or half period) of Ref_clock in which the phase difference is negative, a second predetermined signal in each period (or half period) of Ref_clock in which the phase difference is positive and a third predetermined signal in each period (or half period) of Ref_clock in which the phase difference deviates from zero by less than a predetermined threshold. When the first counter 942 is in its second mode the first counter 942 may increase the value of Rx_fine_start in response to receiving the first predetermined signal, decrease the value of Rx_fine_start in response to receiving the second predetermined signal and maintain the value of Rx_fine_start in response to receiving the third predetermined signal. The second counter 944 may operate analogously however with respect to Rx_fine_stop.

20 Alternatively, if the trigger circuits 924 and 926 are arranged to count both rising and falling edges of a clock signal (thus effectively counting a number of half periods of the clock signal), the phase comparator 940 may be arranged to, in the first stage of the calibration, output a first predetermined signal in each period (or half period) of Ref_clock in which the phase difference is negative, a second predetermined signal in each period (or half period) of Ref_clock in which the phase difference is positive and a third predetermined signal in each period (or half period) of Ref_clock in which the phase difference deviates from zero by less than a predetermined threshold, and in the second stage of the calibration, output a fourth predetermined signal in each period (or half period) of Ref_clock in which the phase difference falls below 180 degrees, a fifth predetermined signal in each period (or half period) of Ref_clock in which the phase difference exceeds 180 degrees and a sixth predetermined signal in each period (or half period) of Ref_clock in which the phase difference deviates from 180 degrees by less than a predetermined threshold. When the first counter 942 is in its second mode the first counter 942 may increase the value of Rx_fine_start in response to receiving the first predetermined signal, decrease the value of Rx_fine_start in response to receiving the second predetermined signal and

maintain the value of Rx_fine_start in response to receiving the third predetermined signal. When the second counter 944 is in its second mode the second counter 944 may increase the value of Rx_fine_stop in response to receiving the fourth predetermined signal, decrease the value of Rx_fine_stop in response to receiving the fifth predetermined signal and maintain the value of Rx_fine_stop in response to receiving the sixth predetermined signal. Alternatively, the second counter 944 may be responsive to the first to third predetermined signals and the first counter 942 may be response to the fourth to sixth predetermined signals when in their respective second modes.

Similar to the CCB 846, the CCB 946 is arranged to, during the calibration mode, control the operations of the controller 920. More specifically the CCB 946 is arranged to control whether the counters 942 and 944 should update the values of Rx_fine_start or Rx_fine_stop, respectively. In the first operational state the CCB 946 may cause the first counter 942 to operate in its second mode and the second counter 944 to operate in its first mode. In the second operational state the CCB 946 may cause the first counter 942 to operate in its first mode and the second counter 944 to operate in its second mode.

The controller 920 further comprises the calculation unit 948 which corresponds to the calculation unit 848. However, the calculation unit 948 is further arranged to receive a signal from the counter 942 which signal represents the currently stored value of Rx_fine_start. The calculation unit 948 is further arranged to receive a signal from the second counter 944 which signal represents the currently stored value of Rx_fine_stop. In response to entering the first operational state of the controller 920, the calculation unit 948 is arranged to output a control signal Rx_fine corresponding to the current value of Rx_fine_start, thereby causing the switchable delay element of the delay line 922 to be set to the particular setting indicated by Rx_fine. During the first operational state the value of Rx_fine_start will increase and decrease until a desired phase relation between Ref_clock and Delay_ref has been achieved. An increase or decrease of Rx_fine_start will cause a corresponding change of the control signal Rx_fine wherein the setting of the switchable delay elements of the delay line 922 will change. In response to entering the second operational state of the controller 920, the calculation unit 948 is arranged to output a control signal Rx_fine corresponding to the current value of Rx_fine_stop. During the second operational state the value

of Rx_fine_stop will increase and decrease until a desired phase relation between Ref_clock and Delay_ref has been achieved. An increase or decrease of Rx_fine_stop will cause a corresponding change of the control signal Rx_fine wherein the setting of the switchable delay elements of the delay line 922 will change.

Similar to the controller 820 the controller 920 may implement lock detection for determining when the first and the second stages of the calibration are complete. When operating in the calibration mode for a first time (e.g. after turning on the power to the system), Rx_fine_start may be initialized to zero. Rx_fine_stop may be initialized to the maximum available value of Rx_fine. Alternatively, Rx_fine_stop may, following determination of Rx_fine_start, be initialized to be equal to Rx_fine_start and thereafter (i.e. during the second operational state) be increased until the desired phase difference between Ref_clock and Delay_ref has been achieved. If calibration is performed additional times, Rx_fine_start and Rx_fine_stop may start from their previously calibrated value. Preferably, calibration is implemented such that $Rx_fine_stop > Rx_fine_start$ upon completion thereof.

According to one embodiment the delay line 922 may be implemented in a same manner as the delay line 322. The delay line 922 may or may not include the varactors 380. Additionally, each variable capacitive load 370 may instead of a varactor include a capacitor having a fixed capacitance. In a first operational state, the controller 920 may disconnect a first number (preferably all) of the varactors of the variable capacitive loads 370 from the output of the associated inverter 360. The controller 920 may thereafter change (e.g. by increasing) the number of connected varactors of the delay line 922 until the total propagation delay of the delay line 922 corresponds to $I_1 * T_ref$ (or alternatively $I_1 * T_ref / 2$). The resulting setting of the delay line 922 forms the first setting. The controller 920 may then in a second operational state start from the first setting determined during the first operational state, and change (e.g. by increasing) the number of connected varactors of the variable capacitive loads 370 until the total propagation delay of the delay line 922 corresponds to $I_2 * T_ref$ (or $I_2 * T_ref / 2$).

In one embodiment the delay line 122 may be implemented as the delay line 422. The transistors 470a, 470b and 480a, 480b of each delay element may or may not have a tunable limiting current. The discussion in the preceding paragraph applies correspondingly to the present embodiment.

However, instead of varying a number of connected varactors, the number of connected transistors 470a, 470b may be varied.

According to one embodiment the controller (e.g. controller 120, 820, 920) may be arranged to estimate the $A \cdot \tau$ propagation delay of the delay line resulting for $Rx_fine = 0$ (e.g. in the analog calibration) or for $Rx_fine = Rx_fine_start$ (e.g. in the digital calibration). The propagation delay $A \cdot \tau$ may for example be estimated by setting the Tx_coarse to a number which gives a zero phase difference (alternatively 180° for $T_ref/2$) between Tx_trigg and Rx_trigg when Delay equals zero. The measurement may for example be performed after the calibration is complete. Knowledge of the value of the total propagation delay resulting for $Rx_fine = 0$ or $Rx_fine = Rx_fine_start$ may enable absolute distances to objects to be estimated. With reference to the previous discussion of the system 100 this embodiment may be used for example if the value of $A \cdot \tau$ is unknown or not known to an extent which allows for the calibrated value of $A \cdot \tau$ to be tied to the integer number I_1 of periods or half periods of Ref_clock .

According to a further embodiment, an analog calibration may be combined with a digital calibration. For example, a controller may be arranged to implement an analog calibration of the minimum total propagation delay of a delay line by controlling v_offset (e.g. using the voltage source 842 described in connection with Fig. 8) and implement a digital calibration of the maximum total propagation delay of the delay line by determining Rx_fine_stop (e.g. using the second counter 944 described in connection with Fig. 9). Conversely, the controller may be arranged to implement a digital calibration of the minimum total propagation delay of a delay line by determining Rx_fine_start (e.g. using the first counter 942 described in connection with Fig. 9) and implement an analog calibration of the maximum total propagation delay of the delay line by controlling v_slope (e.g. using the voltage source 842 described in connection with Fig. 8).

According to one embodiment illustrated in Fig. 10 (wherein elements 1018-1040 and 1048 corresponds to elements 818-840 and 848 in Fig. 8 and 918-940 and 948 in Fig. 9) the controller 1020 may be arranged to, for each correlation between a reference wavelet and a received wavelet, determine and record a phase difference between Ref_clock and $Delay_ref$. According to this embodiment, the delay line 1022 is preferably designed to present an adjustment range resulting in the above-described overlap in the digital-to-time transfer function of the timing circuitry 1018. The relevant values of

Rx_fine may then be determined during post processing by locating the zero crossing in the phase difference as a function of Rx_fine. As illustrated in Fig. 10 the controller 1020 may include an ADC 1050 arranged to digitize the output signal of the phase comparator 1040 which, as discussed in connection with Figs 8 and 9, may represents the determined phase difference. The ADC 1050 may be triggered by the trigger signal ADC_trigg. The digitized phase difference may be stored along with the set of correlations resulting from a plurality of correlations between received wavelets and reference wavelets. A range of Rx_fine may thereafter be determined by identifying Rx_fine values for which the phase difference assumes a minimum for one or more settings of Tx_coarse and Rx_coarse. This enables the set of correlation data corresponding to the determined range of Rx_fine to be determined, wherein the correlation data for Rx_fine values outside the determined range may be discarded. By counting the number of Rx_fine points between the two zero crossings, it is possible to estimate the Δt step size.

As may be understood by the skilled person, although in connection with the drawings, certain functions have been described in connection with, or as being performed by, schematic blocks or elements the present inventive concept is not limited to those specific arrangements of the blocks or elements. As understood by the person skilled in the art, unless explicitly stated otherwise, each of the above described circuit elements and components (e.g. the trigger circuits 124, 126, 824, 826, 924, 926, 1024, 1026, the controller 120, 820, 920, 1020 and the elements thereof such as the computation unit 848, 948, 1048, the phase comparator 840, 940, 1040, the calibration control unit 846, 946 etc.) may be implemented using electronic circuitry, one or more field programmable gate arrays (FPGAs), applications specified integrated circuits (ASICs), or the like, wherein the functions of the elements or components may be implemented using a hardware description language (HDL). It is further contemplated that at least some of the functions of the controller 120, 820, 920 and 1020 may be implemented in software instructions wherein a microprocessor or the like may control the operation of the controller by executing the software instructions. Such controllers may for example include digital-to-analog converters for converting values representing parameters such as Rx_fine, Rx_coarse, Tx_coarse etc into control signals which may be provided to the respective timing circuitries.

In the above the inventive concept has mainly been described with reference to a limited number of examples. However, as is readily appreciated by a person skilled in the art, other examples than the ones disclosed above are equally possible within the scope of the inventive
5 concept, as defined by the appended claims.

CLAIMS

1. A transmitter-receiver system comprising:
 - a transmitter arranged to transmit a wavelet;
 - a receiver arranged to receive a wavelet;
 - 5 a wavelet generator arranged to generate a reference wavelet;
 - timing circuitry arranged to receive a reference clock signal, output a first trigger signal for triggering transmission of a wavelet and output a second trigger signal for triggering generation of a reference wavelet, the timing circuitry comprising a delay line including at least one delay element and
 - 10 being arranged to receive a signal at an input of the delay line and transmit a delayed signal at an output of the delay line, wherein a state of each delay element of at least a subset of said at least one delay elements is switchable between at least a first state and a second state, wherein a delay element in said first state presents a first propagation delay, and a delay element in said
 - 15 second state present a second propagation delay which differs from the first propagation delay by a value which is smaller than a period of the reference clock signal, wherein a total propagation delay of the delay line is configurable by controlling the state of each delay element of said subset; and
 - a controller arranged to control a delay between the first trigger signal
 - 20 and the second trigger signal by controlling the total propagation delay of the delay line;
 - wherein the system is arranged to correlate the reference wavelet with a received wavelet for at least one setting of the total propagation delay.
- 25 2. A transmitter-receiver system according to claim 1, wherein each delay element comprises a logic circuit element, wherein each delay element of said subset is switchable between at least a first state and a second state by varying a capacitive load of the logic circuit element.
- 30 3. A transmitter-receiver system according to claim 1, wherein each delay element comprises a logic circuit element, wherein each delay element of said subset is switchable between at least a first state and a second state by varying a current supplied to the logic circuit element.
- 35 4. A transmitter-receiver system according to any one of claims 1-3, wherein the timing circuitry further comprises trigger circuitry arranged to

receive, at an input of the trigger circuitry, a clock signal and transmit, at an output of the trigger circuit, the second trigger signal in response to receiving a number of rising and/or falling edges of the clock signal, wherein the controller is arranged to control a delay between the output of the first trigger
5 signal and the second trigger signal by controlling the total propagation delay of the delay line and said number of rising and/or falling edges.

5. A transmitter-receiver system according to claim 4, wherein said clock signal received by the trigger circuitry is a delayed reference clock signal
10 transmitted by the delay line.

6. A transmitter-receiver system according to any one of claims 4-5, wherein the system is arranged to, for at least one setting of said number of rising and/or falling edges, correlate a reference wavelet with a received
15 wavelet for a set of different total propagation delays of the delay line.

7. A transmitter-receiver system according to any of the preceding claims, wherein the controller is further arranged to control each delay element of said subset of delay elements to said first state and tune the first propagation
20 delay of each delay element of said subset of delay elements such that the total propagation delay of the delay line corresponds to an integer number of periods of the reference clock signal or half periods of the reference clock signal.

25 8. A transmitter-receiver system according to any of claims 1-6, wherein the delay line includes an additional delay element having a propagation delay which is tunable, wherein the controller is arranged to control each delay element of said subset of delay elements to said first state and tune the propagation delay of said additional delay element such that the total
30 propagation delay of the delay line corresponds to an integer number of periods of the reference clock signal or half periods of the reference clock signal.

9. A transmitter-receiver system according to any of claims 7-8, wherein
35 the controller is further arranged to determine a phase difference between the reference clock signal and a delayed reference clock signal output from the

delay line, and wherein said tuning is based on the phase difference.

10. A transmitter-receiver system according to any of the preceding claims, wherein the controller is further arranged to control each delay element of
5 said subset of delay elements to said second state and tune the second propagation delay of each delay element of said subset of delay elements such that the total propagation delay of the delay line corresponds to an integer number of periods of the reference clock signal or half periods of the reference clock signal.
- 10 11. A transmitter-receiver system according to claim 10, wherein the controller is further arranged to determine a phase difference between the reference clock signal and a delayed reference clock signal output from the delay line and tune the second propagation delay of each delay element of
15 said subset of delay elements based on the phase difference.
12. A transmitter-receiver system according to any of claims 7-11, wherein the controller is arranged to tune the first and/or the second propagation delay of each delay element of said subset of delay elements using a control signal
20 which is common for the delay elements of said subset.
13. A transmitter-receiver system according to any of claims 1-6, wherein the controller is arranged to determine a setting of the states of the delay elements of said subset of delay elements, such that a total propagation delay
25 of the delay line corresponds to an integer number of periods of the reference clock signal or half periods of the reference clock signal.
14. A transmitter-receiver system according to any of claims 1-6, wherein the controller is arranged to:
30 determine a first setting of the states of the delay elements of said subset of delay elements, such that a total propagation delay of the delay line corresponds to a first integer number of periods of the reference clock signal or half periods of the reference clock signal, and
 determine a second setting of the states of the delay elements of said
35 subset of delay elements, such that a total propagation delay of the delay line corresponds to an integer number of periods of the reference clock signal or

half periods of the reference clock signal.

15. A transmitter-receiver system according to any of claims 13-14,
wherein the controller is further arranged to determine a phase difference
5 between the reference clock signal and a delayed reference clock signal
output from the delay line and determine said first and/or second settings by
repeatedly changing the states of one or more of the delay elements of said
subset of delay element based on the determined phase difference.