CLAIMS

1. A memory device comprising:

a first transistor; and

a memory element group comprising a plurality of memory elements, each of the plurality of memory elements comprising:

a first logic element comprising an input terminal and an output terminal; and

a second logic element comprising an input terminal and an output terminal,

wherein the input terminal of the first logic element is electrically connected to the output terminal of the second logic element,

wherein the input terminal of the second logic element is electrically connected to the output terminal of the first logic element,

wherein each of the plurality of memory elements is configured to be supplied with a first power supply potential and a second power supply potential,

wherein the first transistor is provided so that one of the first power supply potential and the second power supply potential is supplied to the first logic element and the second logic element in each of the plurality of memory elements through a source of the first transistor and a drain of the first transistor,

wherein each of the first logic element and the second logic element is an inverter or a clocked inverter,

wherein the first transistor comprises a channel formation region comprising an oxide semiconductor, and

wherein the first power supply potential is higher than the second power supply potential.

2. The memory device according to claim 1, wherein each of the first logic element and the second logic element is configured to be supplied with the first power supply potential and the second power supply potential.

3. The memory device according to claim 1,

wherein each of the plurality of memory elements comprises a second transistor comprising a first terminal, a second terminal, and a gate,

wherein the input terminal of the first logic element is electrically connected to the output terminal of the second logic element through the first terminal of the second transistor and the second terminal of the second transistor, and

wherein the second transistor comprises a channel formation region comprising an oxide semiconductor.

4. The memory device according to claim 1,

wherein each of the plurality of memory elements comprises:

a second transistor comprising a first terminal, a second terminal, and a gate;

a first capacitor comprising a first terminal and a second terminal; and

a third transistor comprising a first terminal, a second terminal, and a gate,

wherein the first terminal of the second transistor is electrically connected to the input terminal of the first logic element and the output terminal of the second logic element,

wherein the second terminal of the second transistor is electrically connected to the first terminal of the first capacitor,

wherein the first terminal of the third transistor is electrically connected to the input terminal of the first logic element, the output terminal of the second logic element, and the first terminal of the second transistor, and

wherein the second transistor comprises a channel formation region comprising an oxide semiconductor.

5. The memory device according to claim 4,

wherein each of the plurality of memory elements comprises:

a fourth transistor comprising a first terminal, a second terminal, and a gate; and

a second capacitor comprising a first terminal and a second terminal,

wherein the first terminal of the fourth transistor is electrically connected to the output terminal of the first logic element and the input terminal of the second logic element,

wherein the second terminal of the fourth transistor is electrically connected to the first terminal of the second capacitor, and

wherein the fourth transistor comprises a channel formation region comprising an oxide semiconductor.

6. The memory device according to claim 1,

wherein each of the plurality of memory elements comprises:

a second transistor comprising a first terminal, a second terminal, and a gate; and a capacitor comprising a first terminal and a second terminal,

wherein the first terminal of the second transistor is electrically connected to the output terminal of the second logic element,

wherein the second terminal of the second transistor is electrically connected to the first terminal of the capacitor and the input terminal of the first logic element, and

wherein the second transistor comprise a channel formation region comprising an oxide semiconductor.

7. The memory device according to claim 1,

wherein the first transistor comprises:

a first electrode over an insulating surface;

an oxide semiconductor film comprising the channel formation region over the

first electrode;

a second electrode over the oxide semiconductor film;

a gate insulating film covering the first electrode, the oxide semiconductor film, and the second electrode; and

a gate electrode over the gate insulating film,

wherein one of the first electrode and the second electrode is the source, and

wherein the other of the first electrode and the second electrode is the drain.

8. The memory device according to claim 1, wherein the plurality of memory elements are connected in series.

9. The memory device according to claim 1, wherein each of the plurality of memory elements is configured to be supplied with a potential of a signal.

10. The memory device according to claim 1, wherein the oxide semiconductor comprises indium, gallium, and zinc.

11. A CPU comprising:

a register comprising a memory device comprising:

a first transistor; and

a memory element group comprising a plurality of memory elements, each of

the plurality of memory elements comprising:

a first logic element comprising an input terminal and an output terminal; and

a second logic element comprising an input terminal and an output terminal,

wherein the input terminal of the first logic element is electrically connected to the output terminal of the second logic element,

wherein the input terminal of the second logic element is electrically connected to the output terminal of the first logic element,

wherein each of the plurality of memory elements is configured to be supplied with a first power supply potential and a second power supply potential,

wherein the first transistor is provided so that one of the first power supply potential and the second power supply potential is supplied to the first logic element and the second logic element in each of the plurality of memory elements through a source and a drain of the first transistor,

wherein each of the first logic element and the second logic element is an inverter or a clocked inverter,

wherein the first transistor comprises a channel formation region comprising an oxide semiconductor, and

wherein the first power supply potential is higher than the second power supply potential.

12. The CPU according to claim 11, wherein each of the first logic element and the second logic element is configured to be supplied with the first power supply potential and the second power supply potential.

13. The CPU according to claim 11,

wherein each of the plurality of memory elements comprises a second transistor comprising a first terminal, a second terminal, and a gate,

wherein the input terminal of the first logic element is electrically connected to the output terminal of the second logic element through the first terminal of the second transistor and the second terminal of the second transistor, and

wherein the second transistor comprises a channel formation region comprising an oxide semiconductor.

14. The CPU according to claim 11,

wherein each of the plurality of memory elements comprises:

a second transistor comprising a first terminal, a second terminal, and a gate; and

a first capacitor comprising a first terminal and a second terminal,

wherein the first terminal of the second transistor is electrically connected to the input terminal of the first logic element and the output terminal of the second logic element,

wherein the second terminal of the second transistor is electrically connected to the first terminal of the first capacitor, and

wherein the second transistor comprises a channel formation region comprising an oxide semiconductor.

15. The CPU according to claim 14,

wherein each of the plurality of memory elements comprises:

a third transistor comprising a first terminal, a second terminal, and a gate; and

a second capacitor comprising a first terminal and a second terminal,

wherein the first terminal of the third transistor is electrically connected to the output terminal of the first logic element and the input terminal of the second logic element,

wherein the second terminal of the third transistor is electrically connected to the first terminal of the second capacitor, and

wherein the third transistor comprises a channel formation region comprising an oxide semiconductor.

16. The CPU according to claim 11,

wherein each of the plurality of memory elements comprises:

a second transistor comprising a first terminal, a second terminal, and a gate; and

a capacitor comprising a first terminal and a second terminal,

wherein the first terminal of the second transistor is electrically connected to the output terminal of the second logic element,

wherein the second terminal of the second transistor is electrically connected to the first terminal of the capacitor and the input terminal of the first logic element, and

wherein the second transistor comprise a channel formation region comprising an oxide semiconductor.

17. The CPU according to claim 11,

wherein the first transistor comprises:

a first electrode over an insulating surface;

an oxide semiconductor film comprising the channel formation region over the first electrode;

a second electrode over the oxide semiconductor film;

a gate insulating film covering the first electrode, the oxide semiconductor film, and the second electrode; and

a gate electrode over the gate insulating film,

wherein one of the first electrode and the second electrode is the source, and

wherein the other of the first electrode and the second electrode is the drain.

18. The CPU according to claim 11, wherein the plurality of memory elements are connected in series.

19. The CPU according to claim 11, wherein each of the plurality of memory elements is configured to be supplied with a potential of a signal.

20. The CPU according to claim 11, wherein the oxide semiconductor comprises indium, gallium, and zinc.

21. A semiconductor device comprising:

a first transistor; and

a memory element comprising:

a first logic element comprising an input terminal and an output terminal;

a second logic element comprising an input terminal and an output terminal;

a second transistor comprising a first terminal, a second terminal, and a gate; and

a first capacitor comprising a first terminal and a second terminal,

wherein the input terminal of the first logic element is electrically connected to the output terminal of the second logic element,

wherein the input terminal of the second logic element is electrically connected to the output terminal of the first logic element,

wherein the first terminal of the second transistor is electrically connected to the input terminal of the first logic element and the output terminal of the second logic element,

wherein the second terminal of the second transistor is electrically connected to the first terminal of the first capacitor,

wherein the memory element is configured to be supplied with a first power supply potential and a second power supply potential,

wherein the first transistor is provided so that one of the first power supply potential and the second power supply potential is supplied to the first logic element and the second logic element in the memory element through a source of the first transistor and a drain of the first transistor,

wherein each of the first logic element and the second logic element is an inverter or a clocked inverter,

wherein the second transistor comprises a channel formation region comprising an oxide semiconductor, and

wherein the first power supply potential is higher than the second power supply potential.

22. The semiconductor device according to claim 21, wherein the first transistor comprises a channel formation region comprising an oxide semiconductor.

23. The semiconductor device according to claim 21, wherein each of the first logic element and the second logic element is configured to be supplied with the first power supply potential and the second power supply potential.

24. The semiconductor device according to claim 21,

wherein the memory element comprises a third transistor comprising a first terminal, a second terminal, and a gate,

wherein the input terminal of the first logic element is electrically connected to the output terminal of the second logic element through the first terminal of the third transistor and the second terminal of the third transistor, and

wherein the third transistor comprises a channel formation region comprising an oxide semiconductor.

25. The semiconductor device according to claim 21,

wherein the memory element comprises:

a third transistor comprising a first terminal, a second terminal, and a gate; and

a second capacitor comprising a first terminal and a second terminal,

wherein the first terminal of the third transistor is electrically connected to the output terminal of the first logic element and the input terminal of the second logic element,

wherein the second terminal of the third transistor is electrically connected to the first terminal of the second capacitor, and

wherein the third transistor comprises a channel formation region comprising an oxide semiconductor.

26. The semiconductor device according to claim 21,

wherein the first transistor comprises:

a first electrode over an insulating surface;

an oxide semiconductor film comprising the channel formation region over the

first electrode;

a second electrode over the oxide semiconductor film;

a gate insulating film covering the first electrode, the oxide semiconductor film, and the second electrode; and

a gate electrode over the gate insulating film,

wherein one of the first electrode and the second electrode is the source, and

wherein the other of the first electrode and the second electrode is the drain.

27. The semiconductor device according to claim 21, wherein the oxide semiconductor comprises indium, gallium, and zinc.