

[0005] For example, the insulation layers may be deposited to include silicon oxide or silicon nitride, and thus a silicon oxide layer and a silicon nitride layer may be formed.

[0006] When the insulation layers are etched to form patterns, a selective etching process with respect to a specific layer may be required. For example, a selective
5 etching process for the silicon nitride layer may be needed. In this case, an etchant composition for only etching the silicon nitride layer while sufficiently protecting the silicon oxide layer may be used.

[0007] Accordingly, an additional ingredient for protecting the silicon oxide layer may be added in an etchant composition. However, when the additional ingredient has a
10 poor compatibility with an acid that serves as an etching component, a uniform etching property may not be achieved due to aggregation or gelation during the etching process.

[0008] For example, Korean Registered Patent Publication No. 10-0823461 discloses a composition for etching both silicon oxide layer and silicon nitride layer, however, the selective etching process as described above may not be realized from the composition.

15

SUMMARY

[0009] According to an aspect of the present invention, there is provided an insulation layer etchant composition having improved etching selectivity and uniformity.

[0010] According to an aspect of the present invention, there is provided a method of
20 forming patterns using the insulation layer etchant composition.

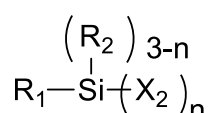
[0011] The above aspects of the present inventive concepts will be achieved by the following features or constructions:

[0012] (1) An insulation layer etchant composition, comprising: phosphoric acid; a silane compound including at least one of a mono-functional silane compound and a di-

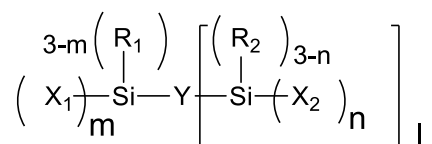
functional silane compound; and a remainder of water.

[0013] (2) The insulation layer etchant composition according to the above (1), wherein the silane compound includes a compound represented by General Formula 1 or 2 below:

5 **[0014]** [General Formula 1]



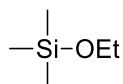
[0015] [General Formula 2]



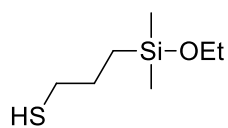
[0016] wherein, in the General Formulae 1 and 2, X_1 and X_2 are each independently
10 halogen, $-OR_3$ group or a phosphate group, R_3 is a C1 to C10 alkyl group, a C1 to C10 alkyl group including an ether bond or a C6 to C12 aryl group, R_1 and R_2 are each independently hydrogen, a C1 to C12 alkyl group or a C6 to C12 aryl group, Y is a divalent or trivalent organic group, and l , m and n are each an integer of 1 or 2.

[0017] (3) The insulation layer etchant composition according to the above (2),
15 wherein the silane compound includes at least one selected from a group consisting of compounds represented by Chemical Formulae 1 to 9 below:

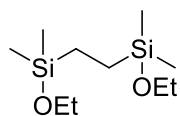
[0018] [Chemical Formula 1]



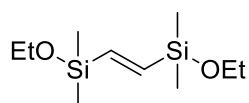
[0019] [Chemical Formula 2]



[0020] [Chemical Formula 3]

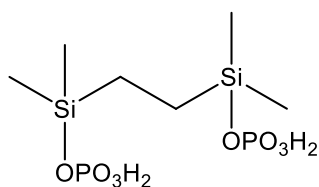


[0021] [Chemical Formula 4]

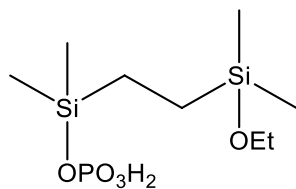


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[0022] [Chemical Formula 5]

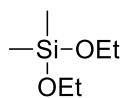


[0023] [Chemical Formula 6]

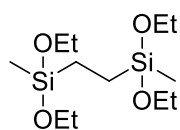


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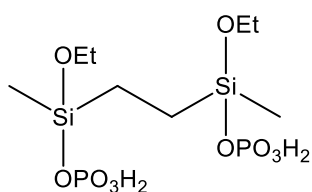
[0024] [Chemical Formula 7]



[0025] [Chemical Formula 8]



[0026] [Chemical Formula 9]



[0027] (4) The insulation layer etchant composition according to the above (1), wherein the silane compound includes halogen, an alkoxy group or a phosphate group as a functional group, and the silane compound does not include a tri-functional silane compound or a tetra-functional silane compound.

[0028] (5) The insulation layer etchant composition according to the above (1), wherein the silane compound includes a compound in which a plurality of mono-functional silane groups or di-functional silane groups are combined via a linker group.

[0029] (6) The insulation layer etchant composition according to the above (1), wherein a compound including a siloxane bond (-Si-O-Si-) is excluded from the composition.

[0030] (7) The insulation layer etchant composition according to the above (1), wherein an amount of the silane compound is in a range from 0.0001 wt% to 1 wt% based on a total weight of the composition.

[0031] (8) A method of forming patterns, comprising: forming an oxide layer and a nitride layer on a substrate; and selectively etching the nitride layer using the insulation layer etchant composition according to any one of the above (1) to (7).

[0032] (9) The method according to the above (8), wherein the oxide layer includes a silicon oxide layer and the nitride layer includes a silicon nitride layer.

[0033] According to exemplary embodiments as described above, the insulation layer etchant composition may include phosphoric acid, and at least one of a mono-functional silane compound or a di-functional silane compound. Accordingly, a gelation or

aggregation caused when a tri-functional or a tetra-functional silane compound is mixed with phosphoric acid may be reduced or avoided so that an etching stability may be improved while maintaining a proper passivation for an oxide layer.

[0034] According to exemplary embodiments, the insulation layer etchant composition may be effectively utilized in a selective etching process for a silicon nitride layer while preventing the silicon oxide layer from being etched.

BRIEF DESCRIPTION OF THE DRAWINGS

[0035] FIGS. 1 to 3 are schematic cross-sectional views illustrating a method of forming patterns in accordance with exemplary embodiments; and

[0036] FIGS. 4 to 6 are schematic cross-sectional views illustrating a method of forming patterns in accordance with exemplary embodiments.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0037] According to exemplary embodiments, an insulation layer etchant composition including phosphoric acid and at least one of a mono-functional silane compound or a di-functional silane compound, and having a high etching selectivity and etching stability is provided. A method of forming patterns using the insulation layer etchant composition is also provided.

[0038] Hereinafter, the present invention will be described in detail with reference to the accompanying drawings. However, those skilled in the art will appreciate that such embodiments described with reference to the accompanying drawings are provided to further understand the spirit of the present invention and do not limit subject matters to be protected as disclosed in the detailed description and appended claims.

[0039] <Insulation Layer Etchant Composition>

[0040] According to exemplary embodiments, an insulation layer etchant composition may include phosphoric acid, a mono-functional silane compound and/or a di-functional silane compound, and a remainder of water.

5 **[0041]** The insulation layer etchant composition may be provided on a structure including an oxide layer (e.g., a silicon oxide layer) and a nitride layer (e.g., a silicon nitride layer) to etch the nitride layer with a high etching selectivity without damaging the oxide layer.

[0042] For example, the insulation layer etchant composition may be used to
10 selectively etch the silicon nitride layer in a fabrication of a semiconductor device.

[0043] Phosphoric acid may be represented by a chemical formula H_3PO_4 , and may serve as a main etching ingredient for etching the nitride layer. In exemplary embodiments, an amount of phosphoric acid may be in a range from about 80 weight percent (wt%) to about 95 wt% based on a total weight of the insulation layer etchant
15 composition.

[0044] If the amount of phosphoric acid may be less than about 80 wt%, an overall etching rate may be degraded. If the amount of phosphoric acid may exceed about 95 wt%, an etching rate for the oxide layer or a conductive layer such as a metal layer may be also increased together with an etching rate for the nitride layer to reduce an etching
20 selectivity for the nitride layer.

[0045] Preferably, the amount of phosphoric acid may be controlled within a range from about 80 wt% to about 90 wt% in consideration of the etching rate and the etching selectivity.

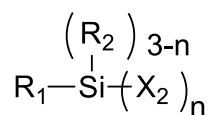
[0046] The etchant composition may include a silane compound for protecting the

oxide layer during etching the nitride layer. In exemplary embodiments, the etchant composition may include the mono-functional silane compound and/or the di-functional silane compound.

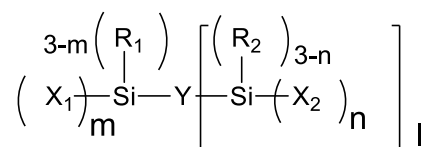
[0047] The term “functional” or “functional group” may indicate a passivation group for the oxide layer which is directly combined with a silicon (Si) atom included in the silane compound. For example, the functional group may indicate a group except for hydrogen or an alkyl group among groups or moieties that are directly combined with the silicon atom. In exemplary embodiments, the functional group may indicate halogen, an alkoxy group or a phosphate group.

[0048] In exemplary embodiments, the mono-functional silane compound or the di-functional silane compound may include a compound represented by General Formula 1 or General Formula 2 below.

[0049] [General Formula 1]



[0050] [General Formula 2]



[0051] In the General Formulae 1 and 2, X_1 and X_2 may each independently represent the functional group of the silane compound. In exemplary embodiments, X_1 and X_2 may each independently halogen, $-OR_3$ group or a phosphate group, and R_3 may represent a C1 to C10 alkyl group, a C1 to C10 alkyl group including an ether bond or a C6 to C12 aryl group. The alkyl group including the ether bond may indicate a group

in which at least one -CH₂- included in an alkyl chain is replaced with -O-.

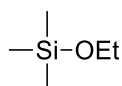
[0052] R₁ and R₂ may each independently represent a non-functional group of the silane compound. In exemplary embodiments, R₁ and R₂ may each independently represent hydrogen, a C1 to C12 alkyl group or a C6 to C12 aryl group. R₁ and R₂ may include a substitution group such as a hydroxyl group or a thiol group.

[0053] Y represents a linker group, and may be a divalent or trivalent organic group. In an embodiment, Y may be a C1 to C4 alkylene group or a C2 to C4 alkenylene group.

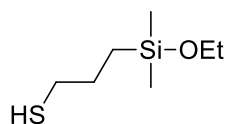
[0054] In the General Formulae 1 and 2, m, l and n may each be an integer of 1 or 2.

[0055] In some embodiments, the etchant composition may include at least one of mono-functional silane compounds represented by Chemical Formulae 1 to 6 below. In the Chemical Formulae below, “Et” represents an ethyl group.

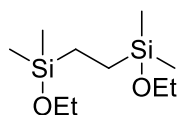
[0056] [Chemical Formula 1]



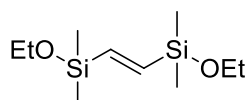
[0057] [Chemical Formula 2]



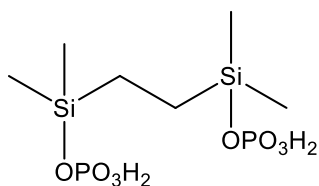
[0058] [Chemical Formula 3]



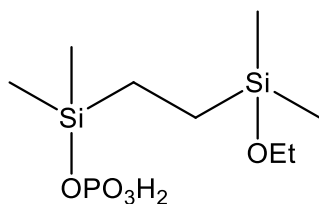
[0059] [Chemical Formula 4]



[0060] [Chemical Formula 5]



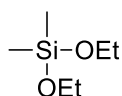
[0061] [Chemical Formula 6]



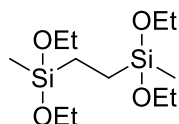
[0062] In some embodiments, the etchant composition may include at least one of di-

5 functional silane compounds represented by Chemical Formulae 7 to 9 below.

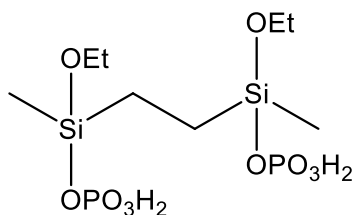
[0063] [Chemical Formula 7]



[0064] [Chemical Formula 8]



10 **[0065]** [Chemical Formula 9]



[0066] For example, the functional group of the silane compound such as halogen, the alkoxy group or the phosphate group may be adsorbed on or chemically interacted with a surface of the silicon oxide layer to serve as a passivation group forming a passivation

15 layer or an etchant barrier.

[0067] However, the silane compound may be an organic-based compound to result in a relatively low compatibility or solubility with phosphoric acid that may be the main etching ingredient. Further, phosphoric acid may be used as a phosphoric acid aqueous solution, and thus the functional group may be hydrolyzed before being dissolved in the phosphoric acid aqueous solution to cause an aggregation or a gelation.

[0068] Tri-functional or tetra-functional silane compounds may be reacted with each other by hydrolysis to be transformed into an oligomer or polymer to degrade etching uniformity and time-dependent stability of an etching process.

[0069] However, according to exemplary embodiments, the mono-functional silane compound and/or the di-functional silane compound may be used so that the number of sites capable of inducing hydrolysis may be reduced, and an oxide passivation may be provided while maintaining time-dependent stability.

[0070] In some embodiments, as represented by Chemical Formulae 3-6, 7 and 8, a silane compound in which a plurality of mono-functional or di-functional silane groups (e.g., two silane groups) are combined by a linker group may be used.

[0071] Accordingly, the oxide passivation may be promoted, and the silane groups may be separated or isolated by the linker group so that the aggregation or the gelation may be reduced or avoided.

[0072] In some embodiments, the silane compound may consist of the mono-functional silane compound and/or the di-functional silane compound, and the tri-functional or tetra-functional silane compound may be excluded from the etchant composition.

[0073] In some embodiments, a fluorine ion generating species (e.g., a fluoride or a fluorine ion salt such as ammonium fluoride) may be excluded from the insulation layer etchant composition. Accordingly, etching damages of the oxide layer by a fluorine

ion may be avoided.

[0074] In some embodiments, the insulation layer etchant composition may not include an ingredient that may generate etching residues on an object such as a siloxane-based compound (e.g., including -Si-O-Si- bond) or an oxime-based compound.

5 **[0075]** For example, the siloxane compound may have a structure similar to that of silicon oxide, and thus may be dissociated by phosphoric acid together with the silicon oxide layer. For example, the siloxane compound may be dissociated in an etching process at a high temperature of 150 °C or more, and thus an initial etching capability may not be constantly maintained.

10 **[0076]** However, according to exemplary embodiments, the mono-functional silane compound and/or the di-functional silane compound may be used as an ingredient for the oxide passivation so that improved etching uniformity and time-dependent stability may be achieved without causing the etching residues and the gelation.

[0077] In some embodiments, the insulation layer etchant composition may include the
15 mono-functional silane compound and/or the di-functional silane compound in an amount ranging from about 0.0001 wt% to about 1 wt% based on a total amount of the composition. If the amount of the silane compound is less than about 0.0001 wt%, an oxide layer passivation may not be substantially realized. If the amount of the silane compound exceeds about 1 wt%, an etching capability from phosphoric acid may be
20 deteriorated or time-dependent stability may be degraded.

[0078] Preferably, the amount of the silane compound may be controlled within a range from about 0.001 wt% to about 0.1 wt% based on the total amount of the composition in a consideration of the oxide layer passivation and the etching uniformity.

[0079] The insulation layer etchant composition may include a remainder of water (e.g.,

deionized water). For example, phosphoric acid may be provided as an aqueous solution (e.g., 85% phosphoric acid), and the silane compound may be included in the amount range as described above based on 100 parts by weight of the phosphoric acid aqueous solution.

5 **[0080]** In some embodiments, the insulation layer etchant composition may consist essentially of the phosphoric acid, the mono-functional silane compound and/or the di-functional silane compound, and a remainder of water. In some embodiments, the insulation layer etchant composition may further include an additive such as an etching enhancer without degrading the passivation effect and time-dependent stability of the
10 silane compound and the etchant composition.

[0081] <Method of Forming Pattern >

[0082] FIGS. 1 to 3 are schematic cross-sectional views illustrating a method of forming patterns in accordance with exemplary embodiments.

[0083] Referring to FIG. 1, an oxide layer 110 and a nitride layer 120 may be formed
15 on a substrate 100.

[0084] The substrate 100 may include a semiconductor material such as single crystalline silicon, single crystalline germanium, etc., or may include polysilicon.

[0085] In exemplary embodiments, the oxide layer 110 may be formed of silicon oxide. The oxide layer 110 may be formed by a chemical vapor deposition (CVD) process, a
20 sputtering process, a physical vapor deposition (PVD) process, an atomic layer deposition (ALD) process, etc.

[0086] The nitride layer 120 may be formed on the oxide layer 110. In exemplary embodiments, the nitride layer 120 may be formed of silicon nitride by a CVD process, a PVD process, a sputtering process, an ALD process, etc.

[0087] Referring to FIG. 2, a photoresist pattern 130 may be formed on the nitride layer 120. For example, a photoresist layer may be formed on the nitride layer 120, and a portion of the photoresist layer may be removed by a selective exposure process and a developing process.

5 **[0088]** Accordingly, the photoresist pattern 130 partially exposing a top surface of the nitride layer 120 may be formed.

[0089] Referring to FIG. 3, a wet etching process may be performed using the insulation layer etchant composition according to exemplary embodiments and using the photoresist pattern 130 as an etching mask.

10 **[0090]** Accordingly, an exposed portion of the nitride layer 120 may be removed to form a nitride pattern 125. As described above, the insulation layer etchant composition according to exemplary embodiments may provide remarkably improved oxide passivation stably for a long period by the silane compound. Thus, a surface of the oxide layer 110 may not be substantially etched or damaged, and the nitride layer
15 120 may be selectively etched.

[0091] For an etching efficiency, the insulation etchant composition may be heated to about 150 °C or more. The photoresist pattern 130 may be removed after the etching process by a strip process and/or an ashing process.

[0092] As illustrated in FIGS. 1 to 3, the nitride layer 120 may be partially removed.
20 Alternatively, the nitride layer 120 may be wholly removed using the etchant composition. In this case, a top surface of the oxide layer 110 may be entirely protected by the silane compound to be prevented from etching damages.

[0093] FIGS. 4 to 6 are schematic cross-sectional views illustrating a method of forming patterns in accordance with exemplary embodiments.

[0094] Referring to FIG. 4, a plurality of oxide layers 210 and nitride layers 220 may be alternately and repeatedly stacked on a substrate 200.

[0095] Referring to FIG. 5, a through pattern 230 penetrating the oxide layers 210 and the nitride layers 220 may be formed. For example, the oxide layers 210 and the nitride layers 220 may be commonly etched by a dry etching process to form an opening, and a filling material may be formed in the opening to form the through pattern 230. The through pattern 230 may be formed of a semiconductor material such as polysilicon, or a conductive material such as a metal.

[0096] Referring to FIG. 6, the nitride layers 220 may be selectively removed using the etchant composition according to exemplary embodiments as described above.

[0097] Accordingly, the oxide layers 210 may remain on a sidewall of the through pattern 230, and gaps 240 may be defined by spaces from which the nitride layers 220 are removed. A conductive layer such as a metal layer may be formed in the gaps 240. The oxide layers 210 may be protected by the silane compound during the etching process from etching damages.

[0098] The methods of forming patterns as described above are provided as exemplary implementations, and the insulation layer etchant composition may be also employed to form various insulation structure included in a semiconductor device or a display device (e.g., a gate insulation layer, a barrier layer, an isolation layer, etc.).

[0099] Hereinafter, preferred embodiments will be described to more concretely understand the present invention with reference to examples. However, it will be apparent to those skilled in the art that such embodiments are provided for illustrative purposes and various modifications and alterations may be possible without departing from the scope and spirit of the present invention, and such modifications and

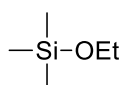
alterations are duly included in the present invention as defined by the appended claims.

[00100] Examples and Comparative Examples

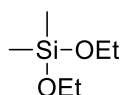
[00101] 0.1 part by weight of silane compounds as listed below was mixed in 100 parts by weight of 85% phosphoric acid aqueous solution to form etchant compositions

5 of Examples and Comparative Examples.

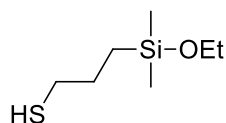
[00102] 1) Example 1



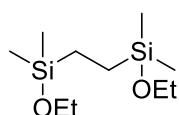
[00103] 2) Example 2



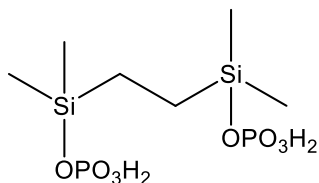
10 **[00104]** 3) Example 3



[00105] 4) Example 4

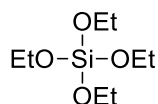


[00106] 5) Example 5

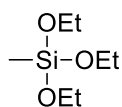


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[00107] 6) Comparative Example 1



[00108] 7) Comparative Example 2



[00109] Experimental Example

[00110] (1) Measuring etching rate (E/R) of silicon nitride (SiN) layer

5 **[00111]** A wafer including a silicon nitride (SiN) layer having a thickness of 5,000 Å thereon was cut to form a sample having a dimension 2*2cm². The sample was immersed in the compositions of Examples and Comparative Examples at 160 °C for 3 minutes. After the immersion, the sample was washed by a deionized water (DIW) and dried. After the drying, a thickness of the sample was measured using a scanning
10 electron microscope (SEM) to measure an etching rate (Å/min).

[00112] Further, the etchant compositions of Examples and Comparative Examples were left for 4 weeks at 60 °C, and then etching rates for the silicon nitride layer were measured by the same method as described above.

[00113] (2) Measuring etching rate of silicon oxide (SiO₂) layer

15 **[00114]** A wafer including a silicon oxide (SiO₂) layer having a thickness of 400 Å was cut to form a sample having a dimension 2*2cm². The sample was immersed in the compositions of Examples and Comparative Examples at 160 °C for 3 minutes. After the immersion, the sample was washed by a deionized water (DIW) and dried. After the drying, a thickness of the sample was measured using Ellipsometer to measure
20 an etching rate (Å/min).

[00115] Further, the etchant compositions of Examples and Comparative Examples were left for 4 weeks at 60 °C, and then etching rates for the silicon oxide layer were measured by the same method as described above.

[00116] The results are shown in Table 1 below.

[00117] [Table 1]

	SiN E/R (Å/min) (A)	SiO ₂ E/R (Å/min) (B)	Etching Selectivity (A/B)	SiN E/R after 4 weeks (Å/min) (C)	SiO ₂ E/R after 4 weeks (Å/min) (D)	Etching Selectivity after 4 weeks (C/D)
Example 1	112	4.2	27	114	4.9	23
Example 2	110	3.4	32	111	4.4	25
Example 3	111	3.8	29	109	3.6	30
Example 4	109	3.5	31	113	4.8	34
Example 5	110	3.6	31	112	4.4	25
Comparative Example 1	109	3.2	34	111	6.1	18
Comparative Example 2	112	3.1	36	113	7.3	15

[00118] Referring to Table 1, in Examples using the mono-functional or di-functional silane compounds, etching selectivities after 4 weeks were substantially the same as or similar to initial etching selectivities. In Comparative Examples, etching selectivities were explicitly decreased after 4 weeks.

What is claimed is:

1. An insulation layer etchant composition, comprising:

phosphoric acid;

5 a silane compound including at least one of a mono-functional silane compound, a di-functional silane compound and a compound in which a plurality of mono-functional silane groups or di-functional silane groups are combined via a linker group; and

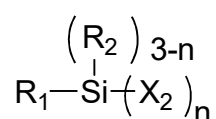
a remainder of water,

10 wherein a fluorine ion generating species is excluded from the insulation layer etchant composition.

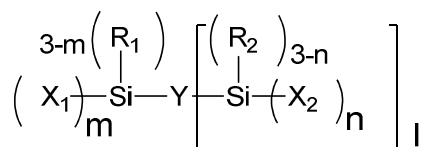
2. The insulation layer etchant composition according to claim 1, wherein the silane compound includes a compound represented by General Formula 1 or 2

15 below:

[General Formula 1]



[General Formula 2]



20 wherein, in the General Formulae 1 and 2, X₁ and X₂ are each independently halogen, -OR₃ group or a phosphate group,

R₃ is a C1 to C10 alkyl group, a C1 to C10 alkyl group including an ether bond or a C6 to C12 aryl group,

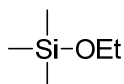
R₁ and R₂ are each independently hydrogen, a C1 to C12 alkyl group or a C6 to C12 aryl group,

5 Y is a divalent or trivalent organic group, and

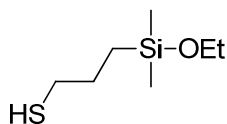
1, m and n are each an integer of 1 or 2.

3. The insulation layer etchant composition according to claim 2, wherein the silane compound includes at least one selected from a group consisting of
10 compounds represented by Chemical Formulae 1 to 9 below:

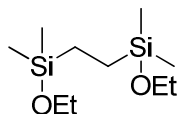
[Chemical Formula 1]



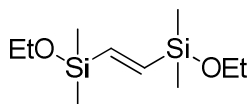
[Chemical Formula 2]



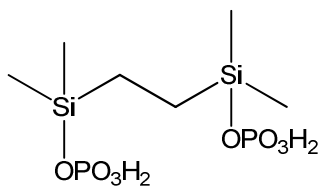
15 [Chemical Formula 3]



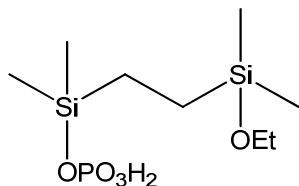
[Chemical Formula 4]



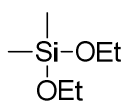
[Chemical Formula 5]



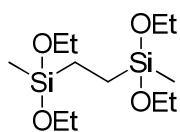
[Chemical Formula 6]



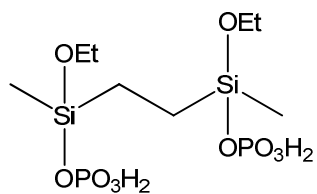
[Chemical Formula 7]



[Chemical Formula 8]



[Chemical Formula 9]



4. The insulation layer etchant composition according to claim 1, wherein the silane compound includes halogen, an alkoxy group or a phosphate group as a functional group, and the silane compound does not include a tri-functional silane compound or a tetra-functional silane compound.

5. The insulation layer etchant composition according to claim 1, wherein a compound including a siloxane bond (-Si-O-Si-) is excluded from the composition.

5 6. The insulation layer etchant composition according to claim 1, wherein an amount of the silane compound is in a range from 0.0001 wt% to 1 wt% based on a total weight of the composition.

7. A method of forming patterns, comprising:
10 forming an oxide layer and a nitride layer on a substrate; and
selectively etching the nitride layer using the insulation layer etchant composition according to any one of claims 1 to 6.

8. The method according to claim 7, wherein the oxide layer includes a
15 silicon oxide layer and the nitride layer includes a silicon nitride layer.