

SUMMARY

[0003a] According to a first aspect, a method of fabricating an emitter region of a solar cell is provided, the method comprising:

forming a silicon layer above a substrate;

implanting, through a stencil mask, dopant impurity atoms in the silicon layer to form

implanted regions of the silicon layer with adjacent non-implanted regions;

forming, through the stencil mask, a capping layer on and substantially in alignment with the
implanted regions of the silicon layer;

removing the non-implanted regions of the silicon layer, wherein the capping layer protects the
implanted regions of the silicon layer during the removing; and

annealing the implanted regions of the silicon layer to form doped polycrystalline silicon
emitter regions.

[0003b] According to a second aspect, a method of fabricating alternating N-type and P-type emitter regions of a solar cell is provided, the method comprising:

forming a polycrystalline silicon layer on a thin oxide layer disposed on a monocrystalline
silicon substrate;

implanting, through a first stencil mask, dopant impurity atoms of a first conductivity type in
the polycrystalline silicon layer to form first implanted regions of the polycrystalline
silicon layer adjacent to non-implanted regions;

forming, through the first stencil mask, a first capping layer on and substantially in alignment
with the first implanted regions of the polycrystalline silicon layer;

implanting, through a second stencil mask, dopant impurity atoms of a second, opposite,
conductivity type in portions of the non-implanted regions of the polycrystalline silicon
layer to form second implanted regions of the polycrystalline silicon layer and resulting in
remaining non-implanted regions;

forming, through the second stencil mask, a second capping layer on and substantially in
alignment with the second implanted regions of the polycrystalline silicon layer;

removing the remaining non-implanted regions of the polycrystalline silicon layer, wherein the
first and second capping layers protect the first implanted regions and the second
implanted regions, respectively, of the polycrystalline silicon layer during the removing;

and

annealing the first implanted regions and the second implanted regions of the polycrystalline
silicon layer to form doped polycrystalline silicon emitter regions.

[0003c] According to a third aspect, an in-line process apparatus for fabricating an emitter region of a solar cell is provided, the in-line process apparatus comprising: a first station configured to align a stencil mask with a substrate;

a second station configured to implant dopant impurity atoms above the substrate, through the
stencil mask; and

a third station configured to form a capping layer above the substrate, through the stencil
mask, wherein the stencil mask and the substrate are configured to move together through
the second and third stations.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] Figures 1A-1F illustrate cross-sectional views of various stages in the fabrication of a solar cell, in accordance with an embodiment of the present disclosure.

[0005] Figure 2 is a flowchart listing operations in a method of fabricating a solar cell as corresponding to Figures 1A-1F, in accordance with an embodiment of the present disclosure.

[0006] Figure 3 is a flowchart listing operations in another method of fabricating a solar cell, in accordance with an embodiment of the present disclosure.

[0007] Figure 4 illustrates a plan of a back surface of an aluminum metallization back contact solar cell, in accordance with an embodiment of the present disclosure.

[0008] Figure 5A schematically illustrates a cross-sectional view of an inline platform for patterned implant and capping, in accordance with an embodiment of the present disclosure.

[0009] Figure 5B illustrates an implant and capping sequence through silicon contact masks in the apparatus of Figure 5A, in accordance with an embodiment of the present disclosure.

[0010] Figure 6A schematically illustrates a cross-sectional view of an inline platform for patterned implant involving traveling wafer and stationary shadow mask, in accordance with an embodiment of the present disclosure.

[0011] Figure 6B illustrates an implant sequence through graphite proximity masks in the apparatus of Figure 6A, in accordance with an embodiment of the present disclosure.

[0012] Figure 7A illustrates a plan view of the back side of an interdigitated back contact (IBC) solar cell having an adjacent “Short Finger” multibusbar layout, in accordance with an embodiment of the present disclosure.

[0013] Figure 7B illustrates a plan view of the back side of an IBC solar cell having a metal foil backplane of copper (Cu) or aluminum (Al), in accordance with an embodiment of the present disclosure.