

WHAT IS CLAIMED IS:

1. A three-dimensional (3D) semiconductor memory device comprising:
 - a substrate;
 - an electrode structure on the substrate, the electrode structure including gate electrodes stacked in a first direction, the first direction perpendicular to a top surface of the substrate;
 - a vertical semiconductor pattern penetrating the electrode structure and connecting to the substrate; and
 - a data storage pattern between the electrode structure and the vertical semiconductor pattern,
- wherein the data storage pattern includes a first insulating pattern, a second insulating pattern, and a third insulating pattern, the first through third insulating patterns sequentially stacked,
- each of the first to third insulating patterns includes a horizontal portion extending in a second direction, the second direction parallel to the top surface of the substrate,
- the horizontal portion of the first insulating pattern, the horizontal portion of the second insulating pattern, and the horizontal portion of the third insulating pattern are sequentially stacked in the first direction, and
- in the second direction, each of the horizontal portion of the first insulating pattern and the horizontal portion of the third insulating pattern protrudes beyond a sidewall of the horizontal portion of the second insulating pattern.

2. The 3D semiconductor memory device of claim 1, wherein in the first direction, each of the first to third insulating patterns includes a vertical portion extending from the horizontal portion, and

the vertical portion of the second insulating pattern is between the vertical portion of the first insulating pattern and the vertical portion of the third insulating pattern.

3. The 3D semiconductor memory device of claim 2, wherein the vertical portion of the first insulating pattern is between the electrode structure and the vertical portion of the second insulating pattern, and

the vertical portion of the third insulating pattern is disposed between the vertical semiconductor pattern and the vertical portion of the second insulating pattern.

4. The 3D semiconductor memory device of claim 2 and claim 3, wherein the vertical semiconductor pattern comprises:

a lower semiconductor pattern penetrating a lower portion of the electrode structure and connected to the substrate; and

an upper semiconductor pattern penetrating an upper portion of the electrode structure and connected to the lower semiconductor pattern,

wherein in the first direction, the horizontal portion of the first insulating pattern, the horizontal portion of the second insulating pattern, and the horizontal portion of the third insulating pattern are sequentially stacked on a top surface of the lower semiconductor pattern.

5. The 3D semiconductor memory device of claim 4, wherein the horizontal portion of the first insulating pattern is adjacent to the lower semiconductor pattern,

wherein the horizontal portion of the third insulating pattern is spaced apart from the lower semiconductor pattern with the horizontal portion of the first insulating pattern between the lower semiconductor pattern and the horizontal portion of the third insulating pattern, and

the horizontal portion of the second insulating pattern is between the horizontal portion of the first insulating pattern and the horizontal portion of the third insulating pattern.

6. The 3D semiconductor memory device of claim 4 or claim 5, wherein the upper semiconductor pattern contacts sidewalls of the horizontal portions of the first to third insulating patterns.

7. The 3D semiconductor memory device of claim 5 or claim 6, wherein the upper semiconductor pattern extends between the horizontal portion of the first insulating pattern and the horizontal portion of the third insulating pattern and contacts the sidewall of the horizontal portion of the second insulating pattern.

8. The 3D semiconductor memory device of claim 1, wherein the horizontal portion of the second insulating pattern is disposed between the horizontal portion of the first insulating pattern and the horizontal portion of the third insulating pattern, and

the vertical semiconductor pattern extends between the horizontal portion of the first insulating pattern and the horizontal portion of the third insulating pattern and contacts the sidewall of the horizontal portion of the second insulating pattern.

9. The 3D semiconductor memory device of any one of claims 1 to 8, wherein the sidewall of the horizontal portion of the second insulating pattern includes a concave surface having a recess toward an inside of the second insulating pattern.

10. The 3D semiconductor memory device of claim 9, wherein the horizontal portion of the first insulating pattern includes a convex sidewall protruding toward an outside of the first insulating pattern, and

in the second direction a lower edge of the sidewall of the horizontal portion of the first insulating pattern protrudes beyond an upper edge of the sidewall of the horizontal portion of the first insulating pattern.

11. The 3D semiconductor memory device of any one of the claims 1 to 10, wherein the sidewall of the horizontal portion of the second insulating pattern includes an inclined surface.

12. The 3D semiconductor memory device of claim 1, wherein among the horizontal portion of the first insulating pattern and the horizontal portion of the third insulating pattern, the horizontal portion of the first insulating pattern is closer to the top surface of the substrate,

wherein a sidewall of the horizontal portion of the first insulating pattern includes a first inclined surface,

the sidewall of the horizontal portion of the second insulating pattern includes a second inclined surface, and

from a normal line perpendicular to the top surface of the substrate, the first inclined surface and the second inclined surface are inclined in opposite directions to each other.

13. The 3D semiconductor memory device of claim 12, wherein a sidewall of the horizontal portion of the third insulating pattern includes a third inclined surface, and

the third inclined surface and the second inclined surface are inclined in the same direction from the normal line.

14. The 3D semiconductor memory device of claim 13, wherein the second inclined surface and the third inclined surface are inclined in the second direction from the normal line, and

wherein the first inclined surface is inclined in an opposite direction to the second direction from the normal line.

15. The 3D semiconductor memory device of claim 13 or claim 14, wherein the second inclined surface is aligned with the third inclined surface.

16. The 3D semiconductor memory device of claim 1, wherein, among the horizontal portion of the first insulating pattern and the horizontal portion of the third insulating pattern, the horizontal portion of the first insulating pattern is closer to the top surface of the substrate,

the horizontal portion of the second insulating pattern is between the horizontal portion of the first insulating pattern and the horizontal portion of the third insulating pattern, and

the horizontal portion of the first insulating pattern protrudes more than the horizontal portion of the third insulating pattern.

17. The 3D semiconductor memory device of claim 1, wherein
a sidewall of the horizontal portion of the first insulating pattern includes an inclined surface, and
from a normal line perpendicular to the top surface of the substrate the inclined surface is inclined in an opposite direction to the second direction.

18. The 3D semiconductor memory device of any one of claims 1 to 17, wherein the second insulating pattern includes a material having an etch selectivity with respect to the first and third insulating patterns.

19. A three-dimensional (3D) semiconductor memory device comprising:
a substrate;
an electrode structure on the substrate, the electrode structure including gate electrodes stacked in a first direction perpendicular to a top surface of the substrate;
a vertical semiconductor pattern penetrating the electrode structure and connecting to the substrate;
a first insulating pattern extending in the first direction, the first insulating pattern between the electrode structure and the vertical semiconductor pattern; and
a second insulating pattern extending in the first direction, the second insulating pattern between the first insulating pattern and the vertical semiconductor pattern,
wherein each of the first and second insulating patterns includes a horizontal portion extending in a second direction, the second direction parallel to the top surface of the substrate,
the horizontal portion of the first insulating pattern is between the substrate and the horizontal portion of the second insulating pattern, and

the horizontal portion of the first insulating pattern protrudes beyond a sidewall of the horizontal portion of the second insulating pattern in the second direction.

20. The 3D semiconductor memory device of claim 19, wherein the second insulating pattern includes a material having an etch selectivity with respect to the first insulating pattern.