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The present invention relates to a semiconductor memory device. The device may be e.g. a dynamic random access memory (hereinafter referred to as dynamic RAM).

5 A dynamic RAM has one or more memory arrays consisting of a plurality of memory cells, and address decoder circuits for selecting appropriate memory cells from the memory arrays, on the basis of address signals.

In a dynamic RAM, each memory cell consists of
10 an insulated gate field effect transistor (hereinafter referred to as MOSFET) and a capacitor. Since each memory cell has a relatively small number of elements, it is relatively easy to form many memory cells on a semiconductor chip, and to thereby fabricate a memory
15 having a large storage capacity.

However, an increase in the number of memory cells formed on the semiconductor chip results in an increase in the number of elements making up the address decoder circuit which selects the appropriate memory
20 cells of the memory array. In other words, the area occupied by the address decoder circuit increases. The increase in the area occupied by the address decoder circuit imposes a limitation in memory size when a memory having a large storage capacity is to be formed
25 on a relatively small semiconductor chip.

Fig. 8 of the accompanying drawings is a diagram of an address decoder circuit that has already been

developed by the inventors of the present invention. The address decoder circuit of Fig. 8 is used for the X system in a dynamic RAM having a storage capacity of, for example, about 256 K (262144) bits.

5 That dynamic RAM of 256 kilobits has four memory arrays each having a storage capacity of 64 K (65536) bits. Each of these memory arrays has 65536 memory cells arranged in the form of a matrix, with data lines being provided for each of the memory cell rows,
10 and word lines being provided for each of the memory cell columns. In this case, each of the memory arrays has, for example, 256 data lines and 256 word lines W_0 to W_{255} .

 In the address decoder circuit of Fig. 8, word
15 lines are selected by address signals from the 256 word lines, and select signals are supplied only to the selected word lines. Therefore, select signals are supplied from the address decoder circuit to the memory cells that are to be selected.

20 The address decoder circuit is used in common for the two memory arrays. Therefore, the above-mentioned dynamic RAM of 256 kilobits is provided with two address decoder circuits shown in Fig. 8. The address decoder circuit has a first address decoder circuit DEC_1
25 and a second address decoder circuit DEC_2 .

 The first address decoder circuit DEC_1 consists of four unit address decoder circuits DEC_{10} to DEC_{13} ,

receives complementary address signals $\underline{ax0}$, $\underline{ax1}$ and decodes them. Therefore, a MOSFET designated by the complementary address signals $\underline{ax0}$, $\underline{ax1}$ is selected from the MOSFETs Q_{100} to Q_{103} , and a select timing signal is selectively formed from the four select timing signals ϕ_{x00} to ϕ_{x11} . In this way 64 word lines are selected from the 256 word lines. A word line is selected by the second address decoder circuit DEC_2 from the above-selected 64 word lines. The second address decoder circuit DEC_2 decodes complementary address signals $\underline{ax2}$ to $\underline{ax7}$, receives through an input terminal a select timing signal corresponding to the decoded signal, and produces an output from its output terminal which turns on a MOSFET that is coupled to the word line which is to be selected. Therefore, the select timing signal is transmitted only to the word line that is to be selected. The second address decoder circuit DEC_2 consists of 64 unit address decoder circuits DEC_{200} to DEC_{263} which each select a corresponding one of the 64 word lines. Since a large number of unit address decoder circuits are required, a relatively large amount of electric power is consumed.

The above-mentioned complementary address signal $\underline{an}$ consists of a pair of internal address signals, i.e. consists of an internal address signal $\underline{an}$ which is substantially in phase with an external address signal An supplied from an external unit, and an internal address signal $\overline{an}$ which is substantially inverted in phase relative to the external address signal An . Therefore,

the complementary address signal ax0 consists of an internal complementary address signal ax0 and an internal address signal ax0 which is inverted in phase relative thereto. In the following description, therefore, the
5 address signals are expressed in the above-mentioned manner.

The internal complementary address signals ax0 to ax7 are formed by an address buffer circuit (not shown). The internal complementary address signals ax2
10 to ax7 are supplied to a relatively large number of unit address decoder circuits as mentioned above. Therefore, the load of address buffer circuit increases. Consequently, the address buffer circuit requires a relatively extended period of time to form internal
15 complementary address signals, and the speed of operation of the dynamic RAM increases.

The present invention seeks to provide a semiconductor memory device in which the circuit structure is simplified relative to the prior art arrangements.
20 It achieves this by providing three select means which are interconnected so that a first select means transmits a signal to the second select means, the second select means transmits a signal to the third select means, and all three receive signals from a control means. The
25 selection of a particular memory cell of a memory array may then be made on the basis of the outputs of the three select means.

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This construction makes it possible to reduce the number of unit decoder circuits. The present invention also makes possible a memory device which consumes less electric power than prior art devices and
5 which may operate at higher speeds.

Embodiments of the present invention will now be described, by way of example, with reference to the accompanying drawings, in which:

Fig. 1 is a block diagram showing a dynamic
10 RAM being a first embodiment of the present invention;

Fig. 2A is a block diagram showing a part of the dynamic RAM of Fig. 1;

Fig. 2B is a circuit diagram showing a memory cell;

15 Fig. 3 is a circuit diagram showing an address decoder circuit X-DEC₂, gate circuits GCU, GCD, and word drivers WDU, WDD;

Fig. 4 is a circuit diagram showing an address decoder circuit X-DEC₁, and a ϕ_x driver ϕ_x -DRV;

20 Fig. 5 is a circuit diagram showing an address decoder circuit X-DEC₃;

Fig. 6 is a circuit diagram of a dynamic RAM being a second embodiment of the present invention;

25 Fig. 7 is a circuit diagram showing an address buffer circuit X-ADB;

Fig. 8 is a circuit diagram showing an address decoder circuit that was developed by the inventors of

the present invention prior to the present invention and has already been discussed; and

Fig. 9 is a plan view showing a layout of a dynamic RAM being a third embodiment of the present invention.

In the description of Fig. 8 above it was assumed that the MOSFETs Q_{100} to Q_{119} were all of the n-channel enhancement type. Similarly, in the subsequent description of embodiments of the present invention it will also be assumed that the MOSFETs are of the n-channel enhancement type, unless otherwise stated. However, the present invention is not limited to the use of such MOSFETs.

In Fig. 1, the circuit blocks surrounded by a dot-dash line are formed on a semiconductor substrate by a known technique for fabricating a semiconductor integrated circuit. In Fig. 1, furthermore, the main circuit blocks are described in the way that they would, in practice, be formed on the semiconductor substrate.

In Fig. 1, $M-ARY_1$ to $M-ARY_4$ denote memory arrays each having 65536 memory cells, although it is not essential for them to have that number of cells. With this number of cells, however, the dynamic RAM has a storage capacity of about 256 kilobits. As will be described later in detail with reference to Fig. 2B, a memory cell has a select terminal, an input/output terminal, a MOSFET for selection, and a capacitor for

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storing data. A control electrode (gate electrode) of the MOSFET is coupled to the select terminal, one electrode of the MOSFET is coupled to the input/output terminal, and the other electrode is coupled to the capacitor for storing data.

In each memory array, e.g. the memory array M-ARY₁, the memory cells are arranged in the form of a matrix of rows and columns of memory cells. As will be discussed later in detail with reference to Fig. 2A, word lines are formed for the memory cell columns, and complementary data lines are formed for the memory cell rows. The select terminals of a plurality of memory cells in the same memory cell column are coupled to a word line that is provided for the memory cell column. Terminals on one side of the word lines are coupled to output terminals of a word driver WDU.

In the memory array, select terminals of the memory cells to be selected receive a select signal from the word driver WDU via word lines. Therefore, one of the memory cell columns in the memory array is selected. The data stored in the selected memory cells are transmitted to the corresponding complementary data lines.

A sense amplifier is provided for each memory cell row. The sense amplifier amplifies the signal on the complementary data line of the memory cell row. Therefore, the data transmitted from the selected memory

cell to the corresponding complementary data line, is amplified by the corresponding sense amplifier. In Fig. 1, a plurality of sense amplifiers provided for a memory array are represented by a circuit block SA. It is preferable that the operation of the sense amplifiers is controlled by a timing signal ϕ_{pa} .

The data amplified by the sense amplifier SA of the memory cell array M-ARY, are transmitted to a column switch C-SW₁ which selects data from the amplified data in response to signals from a column switch driver CSDL. The selected data are transmitted to an input & output circuit via a complementary common data line.

Although the above description has dealt only with the memory array M-ARY₁, the other three memory arrays M-ARY₂ to M-ARY₄ are also constructed in the same manner as the memory array M-ARY₁. Therefore, the input & output circuit receives data from each of the memory arrays, i.e., receives four sets of data. The input & output circuit has a decoder circuit for decoding the complementary address signals $\underline{ax8}$, $\underline{ay8}$. In a reading operation, one of the four sets of data is selected by the complementary address signals $\underline{ax8}$, $\underline{ay8}$, and is transmitted via an input/output terminal D_{IN}/D_{OUT}.

In a writing operation, the data supplied to the input & output circuit via the input/output terminal D_{IN}/D_{OUT}, is transmitted to a complementary common data line designated by the complementary address signals $\underline{ax8}$, $\underline{ay8}$. Therefore, the data is transmitted to one of

the four memory arrays in response to the complementary address signals $ax8$, $ay8$. The data transmitted to the memory array is transmitted to a complementary data line designated by the column switch driver CSD, and then to
5 a memory cell selected by a select signal from the word driver WD, and is written therein.

The input & output circuit transmits the data from the complementary common data line to the input/output terminal D_{IN}/D_{OUT} or transmits the data from the
10 input/output terminal D_{IN}/D_{OUT} to the complementary common data line in dependence on the potential of timing signal ϕ_{RW} .

Fig. 1 shows an X-address buffer circuit X-ADB and a Y-address buffer circuit Y-ADB. External address
15 signals A_0 to A_8 are transmitted to the X-address buffer circuit X-ADB and to the Y-address buffer circuit Y-ADB via external terminals A_0 to A_8 . The X-address buffer circuit X-ADB introduces the external address signals A_0 to A_8 in synchronism with a timing signal ϕ_{ay} to form
20 complementary address signals $\underline{ax}0$ to $\underline{ax}8$ of the system. Similarly, the Y-address buffer circuit Y-ADB introduces the external address signals A_0 to A_8 in synchronism with a timing signal ϕ_{ay} to form complementary address signals $\underline{ay}0$ to $\underline{ay}8$ of the Y system. The Y-address buffer circuit
25 Y-ADB introduces external address signals at a time lagging behind the X-address buffer circuit X-ADB. Therefore, the dynamic RAM of this embodiment uses an address multiplex system.

It is desirable that the complementary address signals ax0, ax1 of the signals ax0 to ax8 are supplied to first X-address decoder circuits and select timing signal drivers X-DEC₁ and ϕ_x -DRV respectively, the
5 complementary address signals ax2 to ax6 are supplied to second X-address decoder circuits X-DEC₂, and the complementary address signal ax7 is supplied to third X-address decoder circuits X-DEC₃. The remaining
10 complementary address signal ax8 is supplied to the input & output circuit as mentioned earlier.

As will be discussed later in detail with reference to Fig. 4, the first X-address decoder circuits and select timing signal drivers X-DEC₁ and ϕ_x -DRV receive a word line select timing signal ϕ_x and
15 the complementary address signals ax0, ax1, and selectively form a select timing signal.

The second X-address decoder circuit X-DEC₂ can be regarded as made up of a plurality of unit decoder circuits as will be mentioned later with
20 reference to Fig. 3. In this embodiment, one unit decoder circuit is provided for eight word lines. In the embodiment, therefore, the second X-address decoder circuit X-DEC₂ has 32 unit decoder circuits. The second X-address decoder circuits X-DEC₂ decode the
25 complementary address signals ax2 to ax6, and supply output signals (decoded signals) to the gate circuits GCU and GUD.

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Each of the gate circuits GCU and GUD can be regarded as a plurality of unit gate circuits, as will be described later in detail with reference to Fig. 3. In this embodiment, one unit gate circuit is provided
5 for eight word lines. Therefore, each of the gate circuits has 32 unit gate circuits, in a similar way to the second X-address decoder circuits X-DEC₂.

The individual decoder circuits of the second X-address decoder circuits X-DEC₂ supply output signals
10 to their corresponding unit gate circuits in the gate circuit GCU, and to their corresponding unit gate circuits in the gate circuit GCD. One unit decoder circuit can be regarded as being provided for substantially 16 word lines.

15 The 32 unit decoder circuits decode the complementary address signals ax₂ to ax₆; i.e., a select signal is formed by one unit decoder circuit which is selected by the complementary address signals from the 32 unit decoder circuits. Therefore, only the
20 two unit gate circuits to which the select signal is supplied are selected from the 64 unit gate circuits.

The two unit gate circuits selected produce select signals that select four of the eight word lines on the basis of output signals of the third X-
25 address decoder circuits X-DEC₃.

Each of the word drivers WDU, WDC can be regarded as a plurality of unit word drivers. In this

embodiment, one unit word driver is provided for eight word lines. Therefore, as with the unit decoder circuits, each of the word drivers has 32 unit word drivers. One unit word driver is provided for each
5 unit gate circuit in the ratio of 1 to 1.

Each unit word driver receives output signals from a corresponding unit gate circuit, and with output signals from the first X-address decoder circuit and select timing signal driver $Y-DEC_1$ and ϕ_x-DRV . A unit
10 word driver receives select signals from the unit gate circuit so as to select four word lines, and selects one of the four word lines on the basis of the complementary address signals $\underline{ax}0$, $\underline{ax}1$, and supplies a select signal thereto.

15 As mentioned above, one of the 256 word lines of the memory array $M-ARY_1$ is designated by the complementary address signals $\underline{ax}0$ to $\underline{ax}7$ and is selected by the address decoder circuits $X-DEC_1$ to $X-DEC_3$, select timing signal driver ϕ_x-DRV , gate
20 circuit GCU and word driver WDU, that are shown on the left side of Fig. 1. In this case, one of the 256 word lines constituting the memory array $M-ARY_3$ designated by the complementary address signals $\underline{ax}0$ to $\underline{ax}7$ is also selected by the address decoder circuits $X-DEC_1$ to $X-DEC_3$,
25 select timing signal driver ϕ_x-DRV , gate circuit GCD and word driver WDD, that are shown on the left side of Fig. 1. At substantially the same time, a word line designated

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by the complementary address signals $\underline{ax}0$ to $\underline{ax}7$ is selected from each of the memory arrays $M-ARY_2$ and $M-ARY_4$ by the address decoder circuits $X-DEC_1$ to $X-DEC_3$, select timing signal driver $\emptyset_x-DRV$, gate circuits GCU, 5 GCD, and word drivers WDU, WDD, that are shown on the right side of Fig. 1.

The complementary address signals $\underline{ay}0$ and $\underline{ay}1$ of the signals $\underline{ay}0$ to $\underline{ay}8$ formed by the Y-address buffer Y-ADB are supplied to the first Y-address decoder circuit & 10 select timing signal driver Y-DEC & $\emptyset_y-DRV$, the complementary address signals $\underline{ay}2$ to $\underline{ay}6$ are supplied to the second Y-address decoder circuit $Y-DEC_2$, and the complementary address signal $\underline{ay}7$ is supplied to the third Y-address decoder circuit $Y-DEC_3$. The remaining 15 address signal $\underline{ay}8$ is supplied to the input & output circuit as mentioned earlier.

It is preferable that the first Y-address decoder circuit and the select timing signal driver $Y-DEC_1$ and $\emptyset_y-DRV$ are constructed in the same manner as 20 the first X-address decoder circuit and select timing signal driver $X-DEC_1$, and $\emptyset_x-DRV$, the second Y-address decoder circuit $Y-DEC_2$ is constructed in the same manner as the second X-address decoder circuit $X-DEC_2$ is constructed in the same manner as the third X-address 25 decoder circuit $X-DEC_3$. Also, the gate circuits GCL, GCR are constructed in the same manner as the gate circuits GCU, GCD, and the column switch drivers CSDL,

SCDR are constructed in the same manner as the word drivers WDU, WDD.

The second Y-address decoder circuit $Y-DEC_2$ may be considered to be a plurality of unit decoder
5 circuits. In this embodiment, it is preferable that one unit decoder circuit is provided for 16 pairs of complementary data lines. Therefore, the second Y-address decoder circuit has 64 unit decoder circuits.

Each of the gate circuits GCL, GCR may be
10 considered to be a plurality of unit gate circuits. Again, it is preferable that one unit gate circuit is provided for eight pairs of complementary data lines. Therefore, each of the gate circuits has 64 unit gate circuits.

15 The unit decoder circuits of the second Y-address decoder $Y-DEC_2$ correspond to the unit gate circuits constituting the gate circuit GCL in a ratio of 1 to 1, and further correspond to the unit gate circuits constituting the gate circuit GCR at a ratio of
20 1 to 1. Thus the output signals of the unit decoder circuits are supplied to the corresponding unit gate circuits in the gate circuit GCL, and to the corresponding unit gate circuits in the gate circuit GCR.

Each of the column switch drivers CSDL, CSDR
25 can also be regarded as a plurality of unit column switch drivers. In this embodiment, one unit column switch driver is provided for eight pairs of

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complementary data lines. Therefore, each of the column switch drivers consists of 64 unit column switch drivers. The unit column switch drivers are provided for the unit gate circuits on a rate of 1 to 1, and hence output
5 signals of the unit gate circuits are supplied to the corresponding unit column switch drivers.

32 of the 64 unit decoder circuits of the second Y-address decoder circuits $Y-DEC_2$ are used for the memory arrays $M-ARY_1$, $M-ARY_2$. Therefore, 32 unit
10 gate circuits in the gate circuit GCL corresponding to the above 32 unit decoder circuits, and 32 unit gate circuits in the gate circuit GCR corresponding to the above 32 unit decoder circuits, are also used for the memory arrays $M-ARY_1$, $M-ARY_2$. Also, 32 unit column
15 switch drivers in the column switch driver CSDL corresponding to 32 unit gate circuits in the gate circuit GCL, and 32 unit column switch drivers in the column switch driver CSDR corresponding to 32 unit gate circuits in the gate circuit GCR, are used for the
20 memory arrays $M-ARY_1$, $M-ARY_2$.

The remaining unit decoder circuits, remaining gate circuits and remaining unit column switch drivers, are used for the other memory arrays $M-ARY_3$, $M-ARY_4$.

For ease of explanation, the following
25 description deals with the parts of the circuit used for the memory arrays $M-ARY_1$, $M-ARY_2$. The parts used for the memory arrays $M-ARY_3$, $M-ARY_4$ are the same as

those used for the memory arrays $M-ARY_1$, $M-ARY_2$.

The 32 unit decoder circuits of the second Y-address decoder $Y-DEC_2$ decode the complementary address signals $\underline{ay}2$ to $\underline{ay}6$, and only one of the 32 unit decoder circuit designated by the complementary address signals forms a select signal. The second Y-address decoder $Y-DEC$ thus forms select signals to select eight pairs of complementary data lines of the memory arrays $M-ARY_1$ and $M-ARY_2$.

10 These select signals are supplied to unit gate circuits in the gate circuit GCL corresponding to the unit decoder circuits that have formed the select signals, and are supplied to the unit gate circuits in the gate circuit GCR that also correspond thereto.

15 The individual gate circuits receiving the select signals form select signals which select four of the eight pairs of complementary data lines on the basis of the output signals of the second Y-address decoder circuit $Y-DEC_2$. Thus, the individual unit gate circuits

20 produce select signals to select four of the eight pairs of complementary data lines on the basis of the complementary address signal $\underline{ay}7$.

 Select signals produced by the unit gate circuits in the gate circuit GCL are supplied to the

25 corresponding unit column switch drivers in the column switch driver CSDL. Similarly, select signals produced by the unit gate circuits in the gate circuit

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GCR are supplied to the corresponding unit column switch driver in the column switch driver CSDR. The individual unit column switch drivers receive signals from the first Y-address decoder circuit Y-DEC₁. The
5 unit column switch drivers receiving the select signals produce select signals which couple only one pair of complementary data lines designated by the output signals of the first Y-address decoder circuit Y-DEC₁ to a pair of complementary common data lines. Thus, of the four
10 pairs of complementary data lines designated by select signals from the unit gate circuits, only one pair of complementary data lines designated by the complementary address signals ay0, ay1 are coupled to a pair of complementary common data lines.

15 The various timing signals mentioned above, and other timing signals required for the operation of the device, are generated by a timing signal generator TG. The timing signal generator TG forms the timing signals using an address strobe signal $\overline{\text{RAS}}$ of the X
20 system supplied via an external terminal $\overline{\text{RAS}}$, an address strobe signal $\overline{\text{CAS}}$ of the Y system supplied via an external terminal $\overline{\text{CAS}}$, and a write enable signal $\overline{\text{WE}}$ supplied via an external terminal $\overline{\text{WE}}$.

Fig. 2A is a block diagram illustrating in
25 detail the memory array M-ARY₁ and its peripheral circuits.

As described with reference to Fig. 1, each

of the second Y-address decoder circuit $Y-DEC_2$, gate circuits GCL, GCR, and column switch drivers CSDL, CSDR corresponding to the memory arrays $M-ARY_1$, $M-ARY_2$, has 32 unit circuits. Of these unit circuits, Fig. 2 shows only two unit decoder circuits $UY-DEC_{200}$, $UY-DEC_{231}$, four unit gate circuits $UGCL_0$, $UGCR_0$, $UGCL_{31}$, $UGCR_{31}$ corresponding to the two unit decoder circuits $UY-DEC_{200}$, $UY-DEC_{231}$, and four unit column switch drivers $UCDL_0$, $UCDR_0$, $UCDL_{31}$, $UCDR_{31}$ corresponding to these unit gate circuits.

As mentioned earlier, the memory array $M-ARY_1$ has 65536 memory cells M that are arranged in the form of a matrix of 256 rows and 256 columns. A pair of complementary data lines D , $\bar{D}$ are formed for each row, and a word line is formed for each column. Therefore, the memory array $M-ARY_1$ is provided with 256 pairs of complementary data lines D_0 , $\bar{D}_0$, to D_{255} , $\bar{D}_{255}$ and with 256 word lines W_{U0} to W_{U255} .

Of the 256 pairs of complementary data lines mentioned above, Fig. 2A shows two pairs of complementary data lines D_0 , $\bar{D}_0$, D_7 , $\bar{D}_7$ that are to be selected by select signals produced by the unit column switch driver $UCDL_0$, and two pairs of complementary data lines D_{248} , $\bar{D}_{248}$, D_{255} , $\bar{D}_{255}$ that are to be selected by select signals produced by the unit column switch driver $UCDL_{31}$.

Of the 256 word lines, Fig. 2A shows only 16

word lines W_{U0} to W_{U7} , and W_{U240} to W_{U247} that will be selected by select signals produced by unit word drivers $UWDU_0$, $UWDU_{30}$ which will be described later with reference to Fig. 3.

5 Fig. 2B illustrates an embodiment of the memory cell M which consists of a select terminal coupled to a word line W, an input/output terminal that is to be connected to either one of the pair of complementary data lines D , $\bar{D}$, a MOSFET Q_{25} , and a capacitor C_M . The gate
10 electrode of the MOSFET Q_M is coupled to the select terminal, one input/output electrode of the MOSFET Q_{25} is coupled to the input/output terminal, and the other input/output electrode of the MOSFET Q_{25} is coupled to the capacitor C_M .

 In the dynamic RAM of this embodiment, it is
15 preferable that the memory array has a folded bit line arrangement.

 In such an arrangement, a pair of complementary data lines (e.g. D_0 and $\bar{D}_0$) are arranged in parallel with each other. As shown in Fig. 2A, the input/output terminals of a plurality of memory cells M are coupled to
20 either one of the pair of complementary data lines D_0 , $\bar{D}_0$ according to a predetermined rule. A pair of input/output terminals of a sense amplifier is coupled to the pair of complementary data lines D_0 , $\bar{D}_0$. The sense amplifier
25 preferably consists of a pair of input/output terminals and MOSFETs Q_{17} to Q_{19} . The gate of MOSFET Q_{17} and the drain of MOSFET Q_{18} are coupled to one of the pair of input/output terminals and the drain of MOSFET Q_{17} and the gate of MOSFET

Q_{18} are coupled to the other input/output terminal. The source of MOSFET Q_{17} and the source of MOSFET Q_{18} are connected in common, and are coupled to the earth potential of the circuit via a MOSFET Q_{19} that is controlled by a
5 timing signal ϕ_{pa} .

Precharging MOSFETs Q_1, Q_2 which are provided between a power-source voltage V_{CC} and the data lines $D_0, \bar{D}_0$ and their switching operation is controlled by a timing signal ϕ_p (precharging signal). MOSFETs Q_3, Q_4 acting as
10 column switches are provided between the pair of complementary common data lines $D_0, \bar{D}_0$ and the pair of complementary common data lines $CD_1, \bar{CD}_1$. The gates of the MOSFETs acting as column switches receive a signal C_{L0} from the unit column switch driver $UCDL_0$.

15 As for the pair of complementary data lines $D_0, \bar{D}_0$, the other pairs of complementary data lines $D_1, \bar{D}_1$ to $D_{255}, \bar{D}_{255}$ are also provided with memory cells, a sense amplifier, precharging MOSFETs, and MOSFETs acting as column switches.

20 In the memory array, the select terminals of a plurality of memory cells of a memory cell column are coupled to the same word line (e.g., W_{U0}). Therefore, the memory cells of a memory cell column receive a select signal from a unit word driver via the word line
25 W_{U0} . The other memory cell columns have also been constructed in the same manner as the memory cell column discussed above.

Though not shown in Fig. 2A, a dummy cell is

coupled to each of the data lines. As is well known, the dummy cell applies a reference potential to the sense amplifier during the reading operation. Therefore, when a memory cell is selected with its input/output
5 terminal being connected to one of the pair of complementary data lines, a dummy cell connected to the other data line is selected. Accordingly, the sense amplifier receives a potential corresponding to data stored in the selected memory cell, and the reference
10 potential from the dummy cell.

In the dynamic RAM of this embodiment, the second X-address decoder circuit $X-DEC_2$ selects one of the 32 unit gate circuits $UGCU_0$ to $UGCU_{31}$ which constitute the gate circuit GCU , and selects one of
15 the 32 unit gate circuits $UGCD_0$ to $UGCD_{31}$ which constitute the gate circuit GCD .

Fig. 3 illustrates the second X-address decoder circuit $X-DEC_2$, gate circuits GCU , GCD , and word drivers WDU , WDD according to an embodiment of the
20 present invention.

Only two of the 32 unit decoder circuits $UX-DEC_{200}$ to $UX-DEC_{231}$ of the second X-address decoder circuit $X-DEC_2$ are shown in Fig. 3, being unit decoder circuits $UX-DEC_{230}$ and $UX-DEC_{231}$. The unit decoder
25 circuit $UX-DEC_{230}$ consists of a five-input NOR gate circuit made up of five drive MOSFETs Q_{44} to Q_{48} connected between the output lines l_2 and earth

potential V_{SS} of the circuit, and a precharging MOSFET Q_{49} which is provided between the output line ℓ_2 and the power-source voltage V_{CC} . The switching operation of the precharging MOSFET Q_{49} is controlled by a timing signal (precharging signal) ϕ_p . Other unit decoder circuits are also constructed in the same manner as the unit decoder circuit UX-DEC₂₃₀. However, it should be noted that different combinations of internal address signals are supplied to the unit decoder circuits.

Therefore, only that unit decoder circuit which is designated by the complementary address signals $\bar{a}_2$ to $\bar{a}_6$ forms a select signal of the high level and the other unit decoder circuits form non-select signals of the low level. Accordingly, a select signal is supplied to only one of the 32 unit gate circuits UGCU₀ to UGCU₃₁ of the gate circuit GCU, and a select signal is also supplied to only one of the 32 unit gate circuits UGCD₀ to UGCD₃₁ of the gate circuit GCD.

For example, when the internal address signals $\bar{a}_2$, $\bar{a}_3$, $\bar{a}_4$, $\bar{a}_5$ and $\bar{a}_6$ are at a low level, only the unit decoder circuit UX-DEC₂₃₀ produces a select signal at a high level. Therefore, the select signal is supplied to two unit gate circuits UGCU₃₀ and UGCD₃₀ that correspond to the unit decoder circuit UX-DEC₂₃₀.

The unit gate circuit UGCU₃₀ consists of transfer gate MOSFETs Q_{28} to Q_{35} which selectively supply decoded signals produced by the corresponding

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unit decoder circuit UX-DEC₂₃₀ to the corresponding unit word driver UWDU₃₀, and resetting MOSFETs Q₃₆ to Q₄₃ provided between each of the output terminals N₁ to N₈ of the unit gate circuit UGCU₃₀ and the earth potential of the circuit. The eight transfer gate MOSFETs Q₂₈ to Q₃₅ can be divided into two groups, i.e., divided into four transfer gate MOSFETs Q₂₈ to Q₃₁ and four transfer gate MOSFETs Q₃₂ to Q₃₅. The switching operation of the four transfer gate MOSFETs Q₂₈ to Q₃₁ and another group of four transfer gate MOSFETs Q₃₂ to Q₃₅ are controlled in a complementary manner by the output signals ϕ_{x7} , $\bar{\phi}_{x7}$ from the third X-address decoder circuit X-DEC₃. The eight resetting MOSFETs can also be divided substantially into two groups; four resetting MOSFETs Q₄₀ to Q₄₃, of which the switching operation is controlled by the signal $\bar{a}x7$ produced by the third X-address decoder circuit X-DEC₃, and four resetting MOSFETs Q₃₆ to Q₃₉ of which the switching operation is controlled by the signal $\bar{a}x7$. The switching operation of the resetting MOSFETs of these two groups is controlled in a complementary manner. The switching operation of the transfer gate MOSFETs Q₂₈ to Q₃₁ (or MOSFETs Q₃₂ to Q₃₅) and the resetting MOSFETs Q₃₆ to Q₃₉ (or Q₄₀ to Q₄₃) is controlled in a complementary manner.

For instance, when the transfer gate MOSFETs Q₂₈ to Q₃₁ (or Q₃₂ to Q₃₅) are turned on, the transfer

gate MOSFETs Q_{32} to Q_{35} (or Q_{28} to Q_{31}) are turned off. In this case, the resetting MOSFETs Q_{36} to Q_{39} (or Q_{40} to Q_{43}) are turned off, and the resetting MOSFETs Q_{40} to Q_{43} (or Q_{36} to Q_{39}) are turned on.

5 Other unit gate circuits are also constructed in the same manner as the unit gate circuit $UGCU_{30}$ discussed above.

When a select signal at a high level is produced from the unit decoder circuit $UX-DEC_{230}$, the unit gate
10 circuits $UGCU_{30}$ and $UGCD_{30}$ transmit the select signals to four of the eight output terminals N_1 to N_8 , on the basis of output signals of the third X-address decoder circuit $X-DEC_3$. The potential of the four output
terminals to which the select signal has not been
15 transmitted is changed to a low level by the resetting MOSFETs.

Fig. 5 shows an example of the third X-address decoder circuit $X-DEC_3$ which consists of two unit decoder
circuits $UX-DEC_{30}$ and $UX-DEC_{31}$. The unit decoder circuit
20 $UX-DEC_{30}$ consists of MOSFETs Q_{59} , Q_{60} , which substantially form a push-pull inverter, and a precharging MOSFET Q_{58} which is provided between the output line $_3$ and the
power-source voltage V_{CC} and of which the switching
operation is controlled by the timing signal ϕ_p . The
25 other unit decoder circuit $UX-DEC_{31}$ is constructed in the same manner as the unit decoder circuit $UX-DEC_{30}$.
As shown in Fig. 5, however, different internal address

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signals are supplied to the MOSFETs that constitute the push-pull inverter.

Therefore, when the internal address signal $ax7$ (or $\bar{ax}7$) changes to a high level, the unit decoder circuit UX-DEC₃₁ produces a select signal ϕ_{x7} at a high level (or UX-DEC₃₀ produces a select signal $\bar{\phi}_{x7}$ at a high level), and the unit decoder circuit UX-DEC₃₀ produces a non-select signal $\bar{\phi}_{x7}$ at a low level (or UX-DEC₃₁ produces a non-select signal ϕ_{x7} at a low level).

Therefore, the unit gate circuits which receive output signals from the third X-address decoder circuit X-DEC₃ select four of the eight word lines on the basis of the complementary address signal $ax7$, i.e., the unit gate circuits UGCU₃₀ and UGCD₃₀ transmit select signals to four of the eight output terminals N_1 to N_8 on the basis of the complementary address signal $ax7$.

Output signals produced by the unit gate circuits are supplied to the corresponding unit word drivers. The unit word driver UWDU₃₀ corresponding to the unit gate circuit UGCU₃₀ consists of eight transfer gate MOSFETs Q_{20} to Q_{27} as shown in Fig. 3. The gate of the transfer gate MOSFET Q_{20} is connected to the output terminal N_1 of the corresponding unit gate circuit UGCU₃₀ and to the output line l_2 of the corresponding unit decoder circuit UX-DEC₂₃₀ via a transfer gate MOSFET Q_{28} . Similarly, the gate of the transfer gate MOSFET

Q₂₁ is connected to the output terminal N₂ and to the output line ℓ_2 via MOSFET Q₂₉, the gate of the transfer gate MOSFET Q₂₂ is connected to the output terminal N₃ and to the output line ℓ_2 via MOSFET Q₃₀, and so for
5 MOSFETs Q₂₃ to Q₂₆, and the gate of the transfer gate MOSFET Q₂₇ is connected to the output terminal N₈ and to the output line ℓ_2 via MOSFET Q₃₅. The select timing signal $\emptyset_{x00}$ of the first X-address decoder circuit and the select timing signal driver X-DEC and $\emptyset_x$ -DRV is
10 supplied to one electrode of each of the transfer gate MOSFETs Q₂₃ and Q₂₇, the select timing signal $\emptyset_{x01}$ is supplied to one electrode of each of the transfer gate MOSFETs Q₂₂ and Q₂₆, the select timing signal $\emptyset_{x10}$ is supplied to one electrode of each of the transfer gate
15 MOSFETs Q₂₁ and Q₂₅, and the select timing signal $\emptyset_{x11}$ is supplied to one electrode of each of the transfer gate MOSFETs Q₂₀ and Q₂₄.

The corresponding word lines W_{U240} to W_{U248} are connected to the other electrode of each of the
20 transfer gate MOSFETs Q₂₀ to Q₂₇. The other unit word drivers are also constructed in the same manner as the above unit word driver UWDU₃₀.

When a select signal is produced from the unit decoder circuit UX-DEC₂₃₀, and an internal address
25 signal $\bar{a}x7$ at a low level is supplied to the third X-address decoder circuit X-DEC₃, select signals are produced from each of the output terminals N₁ to N₄ of

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the unit gate circuits $UGCU_{30}$, $UGCD_{30}$, and the potential of other output terminals N_5 to N_8 falls to a low level. Therefore, of the eight transfer gate MOSFETs constituting the unit word drivers $UWDU_{30}$ and $UWDD_{30}$,
5 the transfer gate MOSFETs Q_{24} to Q_{27} are turned off, and the transfer gate MOSFETs Q_{20} to Q_{23} are turned on. Accordingly, the word lines W_{U243} and W_{D243} receive the select timing signal ϕ_{x00} via the transfer gate MOSFET Q_{23} , the word lines W_{U242} and W_{D242} receive the select
10 timing signal ϕ_{x01} via the transfer gate MOSFET Q_{22} , the word lines W_{U241} and W_{D241} receive the select timing signal ϕ_{x10} via the transfer gate MOSFET Q_{21} , and the word lines W_{U240} and W_{D240} receive the select timing signal ϕ_{x11} via the transfer gate MOSFET Q_{20} .

15 As will be described later in detail with reference to Fig. 4, of the four select timing signals ϕ_{x00} to ϕ_{x11} , only one select timing signal designated by the complementary address signals $\underline{ax0}$, $\underline{ax1}$ is changed to the high level by the first X-address decoder circuit
20 and select timing signal driver $X-DEC_1$ and ϕ_x-DRV . For instance, when the select timing signal ϕ_{x00} is at a high level, a select timing signal at a high level is transmitted only to the word lines W_{U243} , W_{D243} . In other words, the select timing signal of the high level
25 is supplied to only those word lines W_{U243} , W_{D243} of the memory array which are designated by the complementary address signals $\underline{ax0}$ to $\underline{ax7}$. Therefore, the word lines

W_{U243} , W_{D243} are selected.

When a select timing signal at a high level is supplied to the word line W_{U243} , memory cells are selected whose select terminals are coupled to that word line. The potential of the data line coupled to the input/output terminals of the selected memory cells varies in dependence upon the data stored in the memory cells. In this case, a dummy cell is coupled to the other data line which forms a pair with the first data line, and a reference potential is applied to the other data line. Then, the sense amplifier coupled to the pair of data lines operates, and the potential difference between the pair of data lines is amplified. As mentioned above, the complementary data lines $D_0, \bar{D}_0$ to $D_{256}, \bar{D}_{256}$, assume a pair of complementary data lines designated by the complementary address signals $\underline{ay}0$ to $\underline{ay}7$ is selected by the first Y-address decoder circuit and select timing signal driver $Y-DEC_1$ and $\emptyset_Y-DRV$, second and third Y-address decoder circuits $Y-DEC_2$, $Y-DEC_3$, column switch C-SW, column switch driver CSD, and gate circuit GC. Consequently, the input & output circuit receives the data stored in the memory cells designated by the complementary address signals $\underline{ax}0$ to $\underline{ax}7$, $\underline{ay}0$ to $\underline{ay}7$ from the four memory arrays $M-ARY_1$ to $M-ARY_4$ via complementary common data lines $CD_1, \bar{CD}_1$ to $CD_4, \bar{CD}_4$.

Upon receipt of complementary address signals

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$\underline{ax}0$, $\underline{ax}1$ and a select timing signal ϕ_x formed by the timing signal generator TG (refer to Fig. 1), the first X-address decoder circuit and select timing signal driver X-DEC₁ and ϕ_x -DRV produces four select timing signals ϕ_{x00} to ϕ_{x11} . These select timing signals ϕ_{x00} to ϕ_{x11} are supplied to the unit word drivers UWDU₀ to UWDU₃₁ and UWDD₀ to UWDD₃₁. Fig. 4 illustrates an embodiment of the first X-address decoder circuit & select timing signal driver X-DEC₁ & ϕ_x -DRV.

10 The first X-address decoder circuit and select timing signal driver X-DEC₁ and ϕ_x -DRV consists of the first X-address decoder circuit X-DEC₁ which decodes the complementary address signals $\underline{ax}0$, $\underline{ax}1$, and the select timing signal driver ϕ_x -DRV which
15 receives output signals of the first X-address decoder circuit X-DEC₁ and the select timing signal ϕ_x and which produces the select timing signals ϕ_{x00} to ϕ_{x11} .

 The first X-address decoder circuit X-DEC₁ consists of four unit decoder circuits UX-DEC₁₀ to
20 UX-DEC₁₃. Fig. 4 illustrates in detail one unit decoder circuit UX-DEC₁₀ of the four unit decoder circuits. The unit decoder circuit UX-DEC₁₀ consists of a two-input NOR gate circuit which has two drive MOSFETs Q₅₂, Q₅₃ coupled between the output line $\hat{L}_1$
25 and earth potential V_{SS} of the circuit, a precharging MOSFET Q₅₀ which is coupled between the output line $\hat{L}_1$ and the power-source voltage V_{CC} and the switching

operation of which is controlled by a timing signal (precharge signal) ϕ_p , and a cut MOSFET Q_{51} of which one electrode is connected to the output line ϕ_1 and the gate electrode is coupled to the power-source voltage V_{CC} . The other unit decoder circuits UX-DEC₁₁ to UX-DEC₁₃ are also constructed in the same manner as the unit decoder circuit UX-DEC₁₀. It should be noted that internal address signals of different combinations are supplied to each of the unit decoder circuits. Therefore, of the four unit decoder circuits, only one unit decoder circuit designated by the complementary address signals $\underline{ax0}$, $\underline{ax1}$ produce a select signal at a high level, and the other unit decoder circuits produce non-select signals at a low level.

The select timing signal driver ϕ_x -DRV consists of four transfer gate MOSFETs Q_{54} to Q_{57} . The select timing signal ϕ_x is supplied to one electrode of each of the transfer gate MOSFETs Q_{54} to Q_{57} . The select timing signals ϕ_{x00} to ϕ_{x11} are produced from the other electrode of each of the transfer gate MOSFETs Q_{54} to Q_{57} . The switching operations of the transfer gate MOSFETs are controlled by the corresponding unit decoder circuits. Thus the switching operation of the transfer gate MOSFET Q_{54} is controlled by a signal produced by the unit decoder circuit UX-DEC₁₀, the transfer gate MOSFET Q_{55} is controlled for its

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switching operation by a signal produced by the unit decoder circuit UX-DEC₁₁, the switching operation of the transfer gate MOSFET Q₅₆ is controlled by a signal produced by the unit decoder circuit UX-DEC₁₂, and
5 the transfer gate MOSFET Q₅₇ is controlled for its switching operation by a signal produced by the unit decoder circuit UX-DEC₁₃. Therefore, of the four transfer gate MOSFETs, only one transfer gate MOSFET designated by the complementary address signals ax0,
10 ax1 is turned on. Therefore, a select timing signal ϕ_x is produced which is at a high level while the select operation is being carried out for the word lines. Therefore, while the selection of word lines is being carried out, any one of the select timing
15 signals ϕ_{x00} to ϕ_{x11} is at a high level.

For instance, if the internal address signals ax0, ax1 is at a low level, the unit decoder circuit UX-DEC₁₀ produces a select signal which causes only the MOSFET Q₅₄ to be turned on. Therefore, the select
20 timing signal ϕ_x is produced as a select timing signal at a high level ϕ_{x00} via the MOSFET Q₅₄.

As mentioned above, the unit decoder circuit is provided with the cut MOSFET Q₅₁. Therefore, owing to the self-bootstrap function of the transfer gate
25 MOSFET, the high-level value of the select timing signal ϕ_{x00} can be brought substantially equal to the high-level value of the select timing signal ϕ_x . When

a signal at a high level is applied to the gate electrode of the transfer gate MOSFET Q_{54} via the cut MOSFET Q_{51} , an inverted layer is formed under the gate electrode of the transfer gate MOSFET Q_{54} . Therefore, a capacitor is formed between the gate electrode and the inverted layer, and is electrically charged. If the select timing signal ϕ_x is changed from a low to a high level to select a word line, the potential of gate electrode of the transfer gate MOSFET Q_{54} is raised due to the action of the capacitor which is electrically charged. Accordingly, the potential of select timing signal ϕ_{x00} becomes approximately equal to the potential of select timing signal ϕ_x . In other words, the level loss caused by the threshold voltage of the transfer gate MOSFET can be reduced. Since the potential of the gate electrode of the transfer gate MOSFET Q_{54} rises, the cut MOSFET Q_{51} is turned off. This makes it possible to prevent the discharge of electric charge from the capacitor.

Described below is the operation for selecting word lines in the dynamic RAM of the first embodiment of the present invention, in conjunction with Figs. 3 to 5.

When the address strobe signal $\overline{RAS}$ rises to a high level, the timing signal generator TG produces a timing signal ϕ_p at a high level. Due to this timing signal ϕ_p , a parasitic capacity is precharged.

As the precharge signal ϕ_p rises to a high level, the precharging MOSFET Q_{50} is turned on during the precharging period. Therefore, signals at a high level are produced from the unit decoder circuits UX-DEC₁₀ to UX-DEC₁₃ of the first X-address decoder circuit X-DEC₁. All the transfer gate MOSFETs Q_{54} to Q_{57} of the select timing signal driver ϕ_x -DRV are turned on. Also, since the precharging MOSFETs Q_{49} , Q_{49}' are turned on by a precharge signal ϕ_p at a high level, signals at a high level are produced from the unit decoder circuits UX-DEC₂₀₀ to UX-DEC₂₃₁ of the second X-address decoder circuit X-DEC₂. Therefore, the unit gate circuits receive signals at a high level from the corresponding unit decoder circuits UX-DEC_{2n} ($n=00$ to 31). Since the precharging MOSFETs Q_{58} , Q_{61} have been turned on by a precharging signal ϕ_p at a high level, signals ϕ_{x7} , $\bar{\phi}_{x7}$ at a high level are produced from the unit decoder circuits UX-DEC₃₀, UX-DEC₃₁ of the third X-address decoder circuit X-DEC₃. The transfer gate MOSFETs Q_{28} to Q_{35} (Q_{28} , to Q_{35} ,) of the unit gate circuits are turned on, and signals at a high level formed by the unit decoder circuits UX-DEC_{2n} are transmitted to the gate electrodes of the transfer gate MOSFETs Q_{20} to Q_{27} (Q_{20} , to Q_{27} ,) of the unit word drivers. Therefore, the transfer gate MOSFETs Q_{20} to Q_{27} (Q_{20} , to Q_{27} ,) are turned on. At this moment, the timing signal generator TG forms

a select timing signal ϕ_x at a low level. Hence, select timing signals at a low level are supplied to the word lines.

Next, as the address strobe signal $\overline{RAS}$ is
5 changed from a high level to a low level, the timing signal generator TG produces a precharge signal ϕ_p at a low level and a timing signal ϕ_{ax} at a high level. In response to the timing signal ϕ_{ax} , the X-address buffer X-ADB introduces external address
10 signals A0 to A8, and produces complementary address signals $\underline{ax}0$ to $\underline{ax}8$ that correspond to the introduced external address signals A0 to A8.

Description will now be given of the operation when the X-address buffer X-ADB has formed internal
15 address signals $\bar{ax}0$, $\bar{ax}1$, $ax2$, $\bar{ax}3$ to $\bar{ax}8$ at a high level (and, the internal address signals $ax0$, $ax1$, $\bar{ax}2$, $ax3$ to $ax8$ are at a low level).

Since the internal address signals $ax0$, $ax1$ are at a low level, only the unit decoder circuit
20 UX-DEC₁₀ of the four unit decoder circuits UX-DEC₁₀ to UX-DEC₁₃ continues to produce a select signal at a high level. On the other hand, the other unit decoder circuits UX-DEC₁₁ to UX-DEC₁₃ produce non-select signal at a low level, because the internal
25 address signals $\bar{ax}0$, $\bar{ax}1$ are at a high level. Therefore, only the transfer gate MOSFET Q₅₄ of the MOSFETs Q₅₄ to Q₅₇ is turned on and the other three MOSFETs

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Q_{55} to Q_{57} are turned off.

Since the internal address signals $\bar{a}x_2$, ax_3 , to ax_6 are at a low level, only the unit decoder circuit UX-DEC₂₃₀ of the 32 address decoder circuits of the second X-address decoder circuit X-DEC receiving a combination of internal address signals $\bar{a}x_2$, ax_3 , to ax_6 continues to produce a select signal at a high level, and the other unit decoder circuits form non-select signals at a low level. Therefore, a signal (select signal) at a high level continues to be supplied to the unit gate circuits UGCU₃₀ and UGCD₃₀ from the unit decoder circuit UX-DEC₂₃₀. On the other hand, signals (non-select signals) at a low level are kept supplied to the other unit gate circuits from the corresponding unit decoder circuits UX-DEC_{2n} ($n=00$ to $29, 31$).

Since the internal address signal $\bar{a}x_7$ is at a high level, the unit decoder circuit UX-DEC₃₀ continues to produce a signal (select signal) $\bar{\phi}_{x7}$ at a high level between two unit decoder circuits constituting the third X-address decoder circuit X-DEC₃. On the other hand, the unit decoder circuit UX-DEC₃₁ produces a signal (non-select signal) ϕ_{x7} at a low level.

Therefore, the transfer gate MOSFETs Q_{32} to Q_{35} of the eight transfer gate MOSFETs in the unit gate circuits UGCU₃₀, UGCD₃₀ are maintained conductive and other transfer gate MOSFETs Q_{28} to Q_{31} are rendered

nonconductive. Also, of the eight resetting MOSFETs in the unit gate circuits $UGCU_{30}$, $UGCD_{30}$, the resetting MOSFETs Q_{36} to Q_{39} receiving the internal address signal $\bar{a}x7$ at a high level are turned on, and the resetting MOSFETs Q_{40} to Q_{43} receiving the internal address signal $ax7$ are turned off. As the resetting MOSFETs Q_{40} to Q_{43} are turned on, the potentials of the output terminals N_1 to N_4 fall to the earth potential, thereby turning off the transfer gate MOSFETs Q_{20} to Q_{23} , of the eight transfer gate MOSFETs in the unit word drivers $WUDU_{30}$, $WUDD_{30}$.

Then, a select timing signal ϕ_x which rises to a high level is produced from the timing signal generator TG; i.e., the select timing signal ϕ_x is produced as a select timing signal ϕ_{x00} from the select timing signal driver ϕ_x -DRV via the transfer gate MOSFET Q_{54} which has been turned on. In this way the first X-address decoder circuit $X-DEC_1$ makes only the select timing signal ϕ_{x00} be at a high level of the four select timing signals ϕ_{x00} to ϕ_{x11} . Therefore, only the word lines WU_{247} , WD_{247} are selected, and their potentials rise to a high level in response to a selected timing signal ϕ_x . When the level of the select timing signal ϕ_x is raised by the bootstrap circuit, level loss caused by the threshold voltage of the MOSFET may be reduced by the self bootstrap function of the transfer gate MOSFETs

Q_{54} , Q_{27} , and the level of the select timing signal ϕ_x is transmitted to the word lines WU_{247} , WD_{247} . Here, the MOSFET Q_{35} works as a cut MOSFET which, when the gate voltage of the MOSFET Q_{27} is raised by the self bootstrap function, prevents the gate voltage from being delivered to the unit decoder circuit UX-DEC₂₃₀.

Although the transfer gate MOSFETs Q_{24} to Q_{26} have been turned on, the word lines WU_{244} to WU_{246} , and WD_{244} to WD_{246} receive non-select signals at a low level and are not selected, because the select timing signals ϕ_{x01} to ϕ_{x11} are at a low level.

Fig. 7 illustrates an embodiment of the address buffer circuit X-ADB, i.e., shows a circuit diagram of a part of the device which forms the complementary address signal $\bar{a}_2$ upon receipt of the external address signal A_2 .

In Fig. 7, an amplifier 1 receives the address signal A_2 and a reference voltage V_{ref} produced by a reference voltage generator circuit (not shown), and produces an address signal a_2 in phase with the external address signal A_2 and an address signal $\bar{a}_2$ of phase inverted relative to the external address signal A_2 . The address signals a_2 , $\bar{a}_2$ are supplied to an output circuit that will be discussed below.

The output circuit consists of MOSFETs Q_{84} , Q_{85} , drive MOSFETs Q_{86} , Q_{87} of which the operation is controlled by address signals a_2 , $\bar{a}_2$ supplied via the

MOSFETs Q_{84} , Q_{85} , and a pair of MOSFETs Q_{88} , Q_{89} of which the drains and gates are connected together in a crossed manner.

When the external address signal A_2 is at a high level, the amplifier 1 produces an address signal a_2 at a high level and an address signal $\bar{a}_2$ at a low level. Therefore, the MOSFET Q_{86} is turned on, and the MOSFET Q_{87} is turned off. A timing signal ϕ_{ax} at a high level, which is produced by the timing signal generator circuit TG to introduce the address signal, is transmitted to the gate of the MOSFET Q_{89} . Therefore, the MOSFET Q_{89} is turned on, and the MOSFET Q_{88} is turned off. Hence, an internal address signal ax_2 at a high level and an internal address signal $\bar{ax}_2$ at a low level are produced from the output circuit. Here, the MOSFETs Q_{84} , Q_{85} are cut MOSFETs that are provided such that the MOSFET Q_{86} or Q_{87} will produce the self bootstrap function.

Other complementary address signals are formed by circuits that are constructed in the same manner as the circuit described above.

According to this embodiment, the consumption of electric power may be reduced since the number of unit decoder circuits is small.

Since the number of MOSFETs served with the internal address signals is small, the load for the output circuit may be reduced. Accordingly, it is

possible for the output circuit to form complementary address signals having predetermined potentials within short periods of time. Accordingly, the dynamic RAM may operate at high speeds.

5 Fig. 9 is a plan view of the second X-address decoder circuit $X-DEC_2$, gate circuit GCU and word driver WDU, which correspond to the unit decoder circuits DEC_{230} , DEC_{231} , unit gate circuits $UGCU_{30}$, $UGCU_{31}$, and unit word drivers $UWDU_{30}$, $UWDU_{31}$ that are
10 shown in Fig. 3. In Fig. 9, the parts corresponding to the circuit elements of Fig. 3 are denoted by the same symbols.

 In Fig. 9, a region Sub surrounded by a two-dot dash line represents a p-type semiconductor substrate,
15 and regions surrounded by broken lines represent n-type semiconductor regions formed on the p-type semiconductor substrate Sub. The n-type semiconductor regions form a source region, a drain region and a wiring layer for the MOSFET. Regions surrounded by
20 a dot-dash line represent electrically conductive polycrystalline silicon layers formed on the semiconductor substrate Sub via a field insulating film or a gate insulating film. The gate electrode or wiring layer of the MOSFET is formed by the electrically
25 conductive polycrystalline silicon layer. In Fig. 9, regions surrounded by solid lines denote aluminium layers that form wiring layers. An intermediate

insulating film is formed between the aluminium layer and the electrically conductive polycrystalline silicon layer. Contact holes C_1 are formed in the intermediate insulating film that is formed between the aluminium layer and the electrically conductive polycrystalline silicon layer, so that the aluminium layer and the electrically conductive polycrystalline silicon layer are coupled together via the contact holes.

The aluminium layer and the semiconductor region are electrically connected together through contact holes C_3 in the insulating film that is formed therebetween. Similarly, when the electrically conductive polycrystalline silicon layer and the semiconductor region are to be electrically coupled together, contact holes C_2 are formed in an insulating film that is formed therebetween, so that the electrically conductive polycrystalline silicon layer and the semiconductor region are coupled together via the contact holes. Although a plurality of contact holes are formed, Fig. 9 shows only representative contact holes shown at C_1 , C_2 and C_3 to simplify the drawing.

It is preferable that a semiconductor region V_{SS} for supplying the earth potential V_{SS} of the circuit to the resetting MOSFETs Q_{36} to Q_{38} is coupled to an aluminium layer V_{SS} which supplies the earth potential V_{SS} of the circuit via an electrically

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conductive polycrystalline silicon layer (not shown).
Also a semiconductor region V_{SS} which supplies the
earth potential V_{SS} of the circuit to the resetting
MOSFETs Q_{40} to Q_{43} is preferably coupled to a semi-
5 conductor region V_{SS} which supplies the earth potential
 V_{SS} of the circuit to the resetting MOSFETs Q_{36} to Q_{38}
via an aluminium layer (not shown).

The memory cell shown in Fig. 2B is formed
between a word line (e.g., WU_{246}) and a neighbouring
10 word line (e.g., WU_{243}), and the select terminal of the
memory cell is coupled to the word line WU_{246} or WU_{243} .

As will be obvious from comparison of Fig. 9
with Fig. 3, the order of word lines is different. In
Fig. 3, the word lines are numbered from the left to
15 right to simplify the drawing. When the gate circuits,
word drivers etc. are formed in practice, the word
lines of Fig. 3 will be formed as shown in Fig. 9. Thus
by forming the unit gate circuits and unit word drivers
as shown in Fig. 9, a select timing signal may be
20 supplied at one place for both unit decoder circuits,
and the area occupied may be reduced.

The gate electrode of a drive MOSFET (e.g.,
a MOSFET Q_{45}) in a unit decoder circuit is coupled to
an aluminium layer $ax3$ which transmits an internal
25 address signal $ax3$ or to an aluminium layer $\bar{ax}3$ which
transmits an internal address signal $\bar{ax}3$, depending
upon an internal address signal that is supplied



thereto.

In this embodiment, the first Y-address decoder circuit and select timing signal driver $Y-DEC_1$ and $\emptyset_Y-DRV$ (refer to Fig. 2A) is constructed in the same manner as the first X-address decoder circuit and select timing signal driver $X-DEC_1$ and $\emptyset_X-DRV$ that is shown in Fig. 4. In this case, complementary address signals $\underline{ay}0$, $\underline{ay}1$ are supplied instead of the complementary address signals $\underline{ax}0$, $\underline{ax}1$, and a select timing signal $\emptyset_Y$ is supplied instead of the select timing signal $\emptyset_X$. Therefore, the first Y-address decoder circuit and select timing signal driver $Y-DEC_1$ and $\emptyset_Y-DRV$ produces select timing signals $\emptyset_{y00}$ to $\emptyset_{y11}$ instead of the select timing signals $\emptyset_{x00}$ to $\emptyset_{x11}$.

The third Y-address decoder circuit $Y-DEC_3$ (refer to Fig. 2A) is constructed in the same manner as the third X-address decoder circuit $X-DEC_3$ that is shown in Fig. 5. In this case, the third Y-address decoder circuit $Y-DEC_3$ receives a complementary address signal $\underline{ay}7$ instead of the complementary address signal $\underline{ax}7$. Therefore, the third Y-address decoder circuit $Y-DEC_3$ produces signals $\emptyset_{y7}$, $\bar{\emptyset}_{y7}$ instead of signals $\emptyset_{x7}$, $\bar{\emptyset}_{x7}$, and also produces signals $\underline{ay}7$, $\bar{\underline{ay}}7$ instead of signals $\underline{ax}7$, $\bar{\underline{ax}}7$.

Each of 32 unit decoder circuits $UY-DEC_{200}$ to $UY-DEC_{231}$ (refer to Fig. 2A) of the second Y-address

decoder circuit $Y-DEC_2$ is constructed in the same manner as the unit decoder circuit $UX-DEC_{230}$ shown in Fig. 3. In this case, the unit decoder circuits $UY-DEC_{200}$ to $UY-DEC_{231}$ receive complementary address signals $\underline{ay}_2$ to $\underline{ay}_6$ instead of complementary address signals $\underline{ax}_2$ to $\underline{ax}_6$.

Each of 32 unit gate circuits $UGCL_0$ to $UGCL_{31}$ ($UGCR_0$ to $UGCR_{31}$) of the gate circuit GCL (GCR) is constructed in the same manner as the unit gate circuit $UGCU_{30}$ shown in Fig. 3. However, the unit gate circuits $UGCL_0$ to $UGCL_{31}$ receive signals $\emptyset_{y7}$, $\bar{\emptyset}_{y7}$, $\underline{ay}_7$, $\bar{\underline{ay}}_7$ formed by the third Y-address decoder circuit $Y-DEC_3$ instead of signals $\emptyset_{x7}$, $\bar{\emptyset}_{x7}$, $\underline{ax}_7$, $\bar{\underline{ax}}_7$.

Moreover, each of 32 unit column switch drivers $UCDL_0$ to $UCDL_{31}$ ($UCDR_0$ to $UCDR_{31}$) (refer to Fig. 2A) of the column switch driver CSDL (CSDR) is constructed in the same manner as the unit word driver $WUDU_{30}$ shown in Fig. 3. In this case, however, the unit column switch drivers $UCDL_0$ to $UCDL_{31}$ ($UCDR_0$ to $UCDR_{31}$) receive select timing signals $\emptyset_{y00}$ to $\emptyset_{y11}$ formed by the first Y-address decoder circuit and select timing signal driver $Y-DEC_1$ and $\emptyset_{Y-DRV}$ instead of select timing signals $\emptyset_{x00}$ to $\emptyset_{x11}$.

The first, second and third Y-address decoder circuits $Y-DEC_1$, $Y-DEC_2$ and $Y-DEC_3$ operate in the same manner as the first, second and third X-address decoder circuits $X-DEC_1$, $X-DEC_2$ and $X-DEC_3$. The select timing

signal driver ϕ_Y -DRV, gate circuit GCL (GCR) and column switch driver CSDL (CSDR) operate in the same manner as the select timing signal driver ϕ_X -DRV, gate circuit GCU (GCD) and word driver WDU (WDD).

5 Fig. 6 shows another dynamic RAM in which the present invention is embodied.

 In Fig. 6, parts which operate in the same manner as those of Figs. 3 to 5 are denoted by the same symbols. In this embodiment, the third X-address
10 decoder circuit X-DEC₃ and the gate circuit GCU (GCD) are different from the third X-address decoder circuit X-DEC₃ and the gate circuit GCU (GCD) that are shown in Figs. 5 and 3.

 In particular the third X-address decoder
15 circuit X-DEC₃ consists of two unit decoder circuits UX-DEC₃₀ and UX-DEC₃₁. The unit decoder circuit UX-DEC₃₀ (UX-DEC₃₁) consists of a ratioless inverter circuit which is made up of MOSFETs Q₈₀, Q₈₁ (Q₈₂, Q₈₃). The MOSFET Q₈₀ (Q₈₂) receives a precharge
20 signal ϕ_p , and the drive MOSFET Q₈₁ (Q₈₂) receives the internal address signal ax7 ($\bar{a}x7$). Signals ϕ_{x7} , $\bar{\phi}_{x7}$ produced by the ratioless inverter circuit are supplied to the gate circuits GCU, GCD.

 Each of the gate circuits GCU, GCD consists of
25 32 unit gate circuits UGCU₀ to UGCU₃₁ (UGCD₀ to UGCD₃₁) as in the embodiment of Fig. 1. Of these unit gate circuits, only one unit gate circuit UGCU₃₁ is shown

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in Fig. 6. Other unit gate circuits are constructed in the same manner as the unit gate circuit $UGCU_{31}$.

The unit gate circuit $UGCU_{31}$ consists of transfer gate MOSFETs Q_{64} to Q_{67} controlled by the signal ϕ_{x7} ,
5 transfer gate MOSFETs Q_{68} to Q_{71} controlled by the signal $\bar{\phi}_{x7}$, resetting MOSFETs Q_{76} to Q_{79} controlled by the signal ϕ_{x7} , and resetting MOSFETs Q_{72} to Q_{75} controlled by the signal $\bar{\phi}_{x7}$.

The level of signal ϕ_{x7} and the level of signal
10 $\bar{\phi}_{x7}$ have complementary values according to complementary address signals $\underline{ax7}$. For instance, when the internal address signal $ax7$ (or $\bar{ax7}$) is at a high level, the signal ϕ_{x7} (or $\bar{\phi}_{x7}$) is also at a high level, and the signal $\bar{\phi}_{x7}$ (or ϕ_{x7}) is at a low level. Therefore,
15 the transfer gate MOSFETs Q_{64} to Q_{67} (or Q_{68} to Q_{71}) are turned on, and the transfer gate MOSFETs Q_{68} to Q_{71} (or Q_{64} to Q_{67}) are turned off. Accordingly, a signal (decoded signal) produced by the unit decoder circuit $UX-DEC_{231}$ is supplied to the unit word driver $UWCU_{31}$
20 via transfer gate MOSFETs Q_{64} to Q_{67} (or Q_{68} to Q_{71}) that have been turned on, and via output terminals N_1 to N_4 (or N_5 to N_8). In this case, the potentials of the output terminals N_5 to N_8 (or N_1 to N_4) to which the transfer gate MOSFETs Q_{68} to Q_{71} (or Q_{64} to Q_{67})
25 of the off condition have been coupled, are set to the earth potential of the circuit via resetting MOSFETs Q_{76} to Q_{79} (or Q_{72} to Q_{75}) that are turned on, and via

the drive MOSFET Q_{81} (or Q_{83}).

Therefore, when the signal produced by the unit decoder circuit UX-DEC₂₃₁ is a select signal, this select signal is supplied to a word line that is
5 designated by complementary address signals $\underline{ax}0$ to $\underline{ax}7$ as in the first embodiment.

According to the embodiment of Fig. 6, no wiring is required to transmit the signals $\underline{ax}7$, $\bar{\underline{ax}}7$ to the unit gate circuits. Therefore, the size of the
10 dynamic RAM can be reduced by an area that would have been occupied by such wiring.

Below are listed some principal effects which may be obtained by the present invention.

(1) The address decoder circuit is divided into
15 three stages to decrease the number of unit address decoder circuits which constitute the address decoder circuit. For instance, 256 word lines (the same also holds true for the data lines) can be selected requiring a total of 38 unit address decoder circuits, i.e.,
20 requiring four first address decoder circuits, 32 second address decoder circuits, and two third address decoder circuits. This is one-half the number of address decoder circuits shown in Fig. 8.

(2) Cut MOSFETs are used as transfer gate MOSFETs
25 that select addresses. Therefore, the number of unit address decoders can be greatly reduced as described in (1) above, without substantially increasing the number of MOSFETs.

(24)

(3) As the number of unit address decoder circuits may be reduced, the chip size of the semiconductor memory device may also be reduced.

(4) Since the number of unit address decoder
5 circuits may be halved, the consumption of electric current may be reduced, and the consumption of electric power of the semiconductor memory device may also be reduced.

(5) The load of the address buffer circuit decreases
10 with a decrease in the number of unit address decoder circuits. Therefore, the address buffer circuit may form complementary address signals having predetermined levels within short periods of time and hence the semiconductor memory device may operate at high speeds.

15 The present invention is not limited to the embodiments described above, but may be modified in a variety of ways. For instance, when the third address decoder circuit X-DEC₃ has a decoder circuit which decodes complementary address signals of two bits, as
20 for the first address decoder circuit X-DEC₁, the number of unit decoder circuits constituting the second address decoder circuit X-DEC₂ may be halved.

Thus, the bits of address signals for the three address decoder circuits can be distributed in
25 a variety of ways. This fact can also be adapted to the address decoder circuits of the Y-system that select data lines.

(65)

Also the address decoder circuits may be constituted by complementary MOS circuits made up of p-channel MOSFFETs and n-channel MOSFETs.

5 Although the foregoing description has dealt with the case in which the present invention was adapted to a dynamic RAM, the invention can also be adapted in the same manner to static RAMs or read-only memories (ROMs) including programmable ROMs.

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Claims:

1. A semiconductor memory device comprising:
a plurality of memory cells;
a control means adapted to generate first,
second, and third select signals, and also at least one
5 timing signal;
first select means which receives the first
select signals and generates fourth select signals for
selecting a first predetermined number of the memory
cells;
10 second select means which receives the second
and fourth signals and generates fifth select signals
for selecting a second predetermined number of memory
cells from the memory cells selected by the first
select means, the second predetermined number being
15 less than the first predetermined number; and
third select means which receives the third
and fifth select signals, and the at least one timing
signal and produces sixth select signals for selecting a pre-
determined number of the memory cells selected by the
20 second select means.
2. A memory device according to claim 1, wherein
the second select means includes a first decoder circuit
and first switching elements, the first decoder circuit
decoding the second select signals and generating
25 signals for controlling the first switching elements,



* C L N S *

(67)

the first switching elements also receiving at their input terminals the fourth switching signals and producing at their output terminals the fifth select signals.

5 3. A memory according to claim 2, wherein the second select means has reference means connected to the output terminals of the first switching elements, which reference means are adapted to supply a predetermined potential to the output terminals in the
10 absence of the fifth select signals.

4. A memory device according to claim 3, wherein the reference means comprises an insulated gate field effect transistor between the output terminals of each of the first switching elements and a point at the
15 predetermined potential.

5. A memory device according to any one of claims 2 to 4, wherein each of the first switching elements comprises an insulated gate field effect transistor.

6. A memory device according to any one of the
20 preceding claims, wherein the third select means includes second switching elements and a select circuit, the second switching elements being controlled by the fifth select signals, the select circuit receiving the third select signals and the at least one timing signal and
25 generating seventh select signals which are fed to input terminals of the second switching elements.

7. A memory device according to claim 6, wherein



the second switching elements include insulated gate field effect transistors.

8. A memory device according to claim 6 or claim 7, wherein the select circuit has a second decoder
5 circuit which decodes the third select signals and generates signals fed to a driver, the driver also receiving the at least one timing signal and generating the seventh select signals.

9. A memory device according to claim 8, wherein
10 the driver has a plurality of third switching elements, the third switching elements receiving the at least one timing signal at their input terminals and being controlled by signals generated by the second decoder circuit.

10. A memory device according to claim 9, wherein
15 the third switching elements include insulated gate field effect transistors.

11. A memory device according to any one of the preceding claims, wherein each memory cell includes an insulated gate field effect transistor and a
20 capacitor for data storage.

12. A semiconductor memory device substantially as herein described with reference to and as illustrated in Figs. 1 to 5 or Figs. 6 and 7, or Fig. 9 of the accompanying drawings.

