## CLAIMS

**1**. A method for designing an integrated circuit, comprising:

folding a two-dimensional (2D) block that has one or more circuit components into a three-dimensional (3D) block having multiple tiers, wherein the one or more circuit components in the folded 2D block are distributed among the multiple tiers in the 3D block;

duplicating one or more input/output (I/O) pin locations across the multiple tiers in the 3D block; and

connecting the one or more duplicated I/O pin locations using one or more intra-block through-silicon-vias (TSVs) placed inside the 3D block.

**2**. The method recited in claim **1**, further comprising:

connecting one or more other blocks in the integrated circuit to one of the duplicated I/O pin locations according to tier locations associated with the one or more other blocks.

**3**. The method recited in claim **2**, further comprising:

performing 3D floorplanning to pack the 3D block and the one or more other blocks into a full-chip design associated with the integrated circuit.

**4**. The method recited in claim **3**, further comprising:

choosing the one or more I/O pin locations to duplicate across the multiple tiers in the 3D block to minimize a total wirelength and a footprint area in the full-chip design.

**5**. The method recited in claim **1**, wherein the one or more intra-block TSVs provide a vertical connection between the one or more duplicated I/O pin locations.

**6**. The method recited in claim **1**, wherein the 2D block and the 3D block comprise intellectual property (IP) blocks.

**7**. The method recited in claim **1**, wherein folding the 2D block into the 3D block further comprises:

partitioning the 2D block into the multiple tiers; and

re-implementing placement and routing associated with the one or more circuit components in the 2D block to distribute the one or more circuit components in the folded 2D block among the multiple tiers in the 3D block and to interconnect the one or more circuit components distributed among the multiple tiers in the 3D block.

**8**. The method recited in claim **7**, further comprising:

determining shared space available across the multiple tiers in the 3D block according to the re-implemented placement and the re-implemented routing; and

placing the one or more duplicated I/O pin locations according to the shared space available across the multiple tiers in the 3D block.

**9**. A three-dimensional (3D) intellectual property block, comprising:

multiple tiers;

one or more circuit components distributed across the multiple tiers; and

one or more input/output (I/O) pin locations that are duplicated across the multiple tiers.

**10**. The 3D intellectual property block recited in claim **9**, further comprising:

one or more through-silicon-vias placed inside the 3D intellectual property block, wherein the one or more

through-silicon-vias connect the one or more I/O pin locations that are duplicated across the multiple tiers.

**11**. The 3D intellectual property block recited in claim **10**, wherein the one or more through-silicon-vias provide a vertical connection between the one or more duplicated I/O pin locations.

**12**. The 3D intellectual property block recited in claim **9**, wherein the one or more I/O pin locations that are duplicated across the multiple tiers are chosen to minimize a total wirelength and a footprint area in a 3D integrated circuit that includes the 3D intellectual property block.

**13**. The 3D intellectual property block recited in claim **9**, wherein the 3D intellectual property block comprises a two-dimensional (2D) intellectual property block that has been folded into the multiple tiers and re-implemented to distribute and interconnect the one or more circuit components among the multiple tiers in the 3D intellectual property block.

**14**. The 3D intellectual property block recited in claim **9**, wherein the one or more duplicated I/O pin locations are placed in the 3D intellectual property block according to shared space available across the multiple tiers.

**15**. A three-dimensional (3D) integrated circuit, comprising:

at least one 3D block having one or more circuit components distributed across multiple tiers and one or more input/output (I/O) pin locations that are duplicated across the multiple tiers; and

at least one additional block located on one of the multiple tiers, wherein the at least one additional block is

connected to one of the duplicated I/O pin locations in the at least one 3D block according to the one of the multiple tiers on which the at least one additional block is located.

**16**. The 3D integrated circuit recited in claim **15**, wherein the at least one 3D block further comprises one or more intra-block through-silicon-vias that connect the one or more I/O pin locations that are duplicated across the multiple tiers in the at least one 3D block.

**17**. The 3D integrated circuit recited in claim **15**, wherein the one or more I/O pin locations that are duplicated across the multiple tiers in the at least one 3D block are chosen to minimize a total wirelength and a footprint area associated with the 3D integrated circuit.

**18**. The 3D integrated circuit recited in claim **15**, wherein the at least one 3D block comprises a two-dimensional (2D) block that has been folded into the multiple tiers and re-implemented to distribute and interconnect the one or more circuit components among the multiple tiers.

**19**. The 3D integrated circuit recited in claim **15**, wherein the one or more duplicated I/O pin locations are placed in the at least one 3D block according to shared space available across the multiple tiers.

**20**. The 3D integrated circuit recited in claim **15**, wherein at least one of the 3D block or the at least one additional block comprises an intellectual property (IP) block.

**21**. The 3D integrated circuit recited in claim **15**, wherein the at least one additional block comprises one or more of a two-dimensional (2D) block or a second 3D block.