

Method and Apparatus for Testing a Device-Under-Test

Description

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The present invention relates to testing of integrated circuits (ICs) and semiconductor devices by means of automated test equipment (ATE).

10 During a typical semiconductor manufacturing processes, ICs are tested to ensure their proper operation. The ATEs perform necessary tests to ensure functionality and quality, with the ICs being devices under test (DUT). In general, a test to be performed on a DUT consists of a set of digital pattern vectors that translate to stimulus voltage levels to be applied to input signal pins of the DUT according to a pre-specified timing. Signals
15 captured from output signal pins of the DUT are translated into corresponding response vectors that may be analyzed to determine whether the DUT is operating according to its specification. The ATE generally provides a number of signal generating resources that may generate configurable signal levels with configurable timing. The tester also provides signal processing resources capable of converting signals generated by the DUT (e.g. in
20 analog form) into a format (e.g. in digital form) readable by the tester. The signal processing resources may also be configurable. The ATE may be configured, e.g., by way of a set of relays, to electrically connect any tester resource to any tester interface pin.

A typical automated tester for integrated circuits includes a set of so-called test channels,
25 each connected to separate pin of an IC or DUT. This is schematically depicted in Fig. 1a.

Fig. 1a schematically shows an ATE 100 for testing a DUT 130. The ATE 100 comprises a plurality of test channels 110-1, 110-2 to 110-n. Each of the test channels 110 is coupled to a central test control unit 120, such as, a computer or microcontroller. On the DUT-end,
30 each of the test channels 110-1, 110-2 to 110-n is dedicated to a different input and/or output (I/O) pin of the DUT 130. Each test channel 110-1, 110-2 to 110-n may be divided into a digital and an analog signal processing part. Within the digital part, each test channel 110-1, 110-2 to 110-n comprises a channel-specific channel control block 111 coupled to the central test control unit 120, wherein the channel control block 111 again controls
35 further digital test channel blocks, such as a digital test pattern generator 112 for generating digital pattern vectors, a test pattern comparator 113 for analyzing response vectors and a time formatting block 114 to generate pre-specified timings. Together, the blocks 111, 112, 113 and 114 make up a so-called digital test channel. The channel control

block 111 traditionally also controls analog signal processing blocks or hardware resources 115, 116 coupled in between an I/O pin of the DUT 130 and the digital test channel, wherein the hardware resources 115, 116 are adapted to connect the digital test channel to the DUT 130, or wherein the hardware resources 115, 116 are adapted to convert a signal or a test pattern to/from the DUT 130 to a signal suited for the DUT-pin / the digital test channel. Hence, the hardware resources 115, 116 e.g. comprise switches, relays, signal level drivers, threshold comparators, analog-to-digital converters (ADCs) and/or digital-to-analog converters (DACs), etc..

Conventionally, the digital test channels are arranged in a separate digital test channel IC, while the hardware resources 115, 116 are kept external to the digital test channel IC in order to ease their substitution, respectively. Such a setup is exemplarily shown in Fig. 1b.

As has been explained above, each of the test channels 110-1, 110-2 to 110-n is divided into a digital test channel part 140-1, 140-2,..., 140-n, and an analog test channel part 150-1, 150-2, ..., 150-n, respectively. Thereby, the digital test channel parts 140-1, 140-2,..., 140-n of the test channels 110-1, 110-2,..., 110-n, i.e., the blocks 111, 112, 113 and 114, respectively, are placed into a dedicated test pattern processing IC 140. The analog test channel parts 150-1, 150-2, ..., 150-n, i.e., the parts comprising the hardware resources 115, 116, respectively, are located externally from the test pattern processing IC 140 in between the DUT 130 and the pattern processing IC 140.

As has been explained with reference to Fig. 1a, the dedicated pattern processing IC 140 is responsible for generating digital patterns that translate, via the hardware resources 150, to stimulus voltage levels to be applied to a plurality of input signal pins of the DUT 130 according to a pre-specified timing. Signals captured from a plurality of output signal pins of the DUT 130 via the hardware resources 150 are translated into corresponding response vectors that may again be analyzed by the dedicated pattern processing IC 140. For this reason, such a chip 140 typically has a plurality of digital test channels 140-1, 140-2,..., 140-n. In addition, external hardware components or resources 150-1, 150-2, ..., 150-n are needed, e.g., relays 116, or signal drivers 115, that can drive various voltages. Also, ADCs, DACs and many more hardware resources may be applied.

Traditionally, each digital test channel part 140-1, 140-2,..., 140-n in the pattern processing or test channel IC 140 controls its associated analog hardware resources 150-1, 150-2, ..., 150-n, respectively. Such a setup may create great difficulties when the external resources 150-1, 150-2, ..., 150-n are replaced for any reason with other components or resources that behave differently. Normally, the test channel IC 140 has to be adapted in

this case. However, modifying the test channel IC 140 is an expensive and time consuming process. Also, the test software running on the central test control unit 120 would have to be adapted in case of such modifications.

- 5 Hence, it is an object of the present invention to avoid these disadvantages and, hence, to provide an improved concept for automated testing of DUTs.

This object is solved by an apparatus for testing a DUT according to claim 1 and a method for testing a DUT according to claim 9.

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Some embodiments of the present invention also provide a computer program for carrying out steps of the inventive method.

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Embodiments of the present invention provide an apparatus for testing a DUT, the apparatus comprising a test channel integrated circuit adapted to communicate with an input or output pin of the device-under-test by means of a hardware resource. Further, the apparatus comprises a resource control means coupled to the test channel integrated circuit for receiving a logical control command describing a desired operation of the hardware resource, wherein the resource control means is adapted to convert the logical control command into a dedicated control command for the hardware resource, wherein the dedicated control command is adapted to a physical implementation of the hardware resource. Thereby, the logical control command received from the test channel integrated circuit is adapted to the hardware resource genus or species, however, it is kept independent from an actual physical implementation of the hardware resource.

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According to embodiments of the present invention, the apparatus comprises a plurality of test channel integrated circuits, wherein the resource control means is shared by the plurality of test channel integrated circuits and is adapted to multiplex different logical control commands from different test channel integrated circuits to a single control data port, which may be coupled to a multi-channel port of a multi-channel hardware resource. According to the present invention, the plurality of test channel integrated circuits corresponds to the digital test channel parts 140-1, 140-2,..., 140-n in the pattern processing or test channel IC 140 explained with reference to Fig. 1b.

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- 35 Hence, embodiments of the present invention allow high integration of modern hardware resources for more than one channel, i.e. so-called multi-channel hardware resources, with only a single control port or channel, while saving control signals, space, power and cost.

According to further embodiments of the present invention, the apparatus comprises a plurality of test channel integrated circuits, wherein the shared resource control means is adapted to temporally schedule different logical control commands from different test channel integrated circuits, such that the different test channel integrated circuits may subsequently access a single hardware resource in a multiplexing scheme, such as, e.g., time division multiplexing (TDM).

Hence, embodiments of the present invention allow using one single general hardware resource for a plurality of test channels. Virtually this hardware resource exists for each test channel. However, physically there is only one instance of the hardware resource. This enables test system flexibility and reduced system and component costs.

Also, according to some embodiments, the (shared) resource control means is re-configurable, e.g. by programming, for adapting the resource control means to a varying or changing physical implementation of actually connected hardware resources. I.e., the (shared) resource control means may be reconfigured to at least one new external resource when the at least one external resource is replaced for any reason with other components or resources that behave differently.

Embodiments of the present invention allow an emulation of hardware resource control protocols while keeping logical channel control commands for controlling the hardware resources uniformed to a respective hardware resource genus (species), but independent of the actual physical implementation of the connected hardware resource. This means, e.g., if an ADC resource is replaced by another ADC resource, the logical channel control commands delivered from the test channel integrated circuit to the resource control means are still valid for the new, replaced ADC resource. Hence, channel resources may be changed without changing a channel control algorithm running on the central test control unit 120 and/or the channel-specific channel control block 111. When changing a channel hardware resource only the respective "translation-scheme" from the logical control command to the dedicated control command has to be adapted to the new channel resource.

Embodiments of the present invention will be described in more detail with respect to the accompanying drawings, in which:

Fig. 1a shows a schematic block diagram of a prior art automated test system (ATE);

- Fig. 1b shows a separation of the ATE according to Fig. 1a into digital test channel integrated circuits and external analog hardware resources;
- 5 Fig. 2 shows an apparatus for testing a device-under-test (DUT), according to an embodiment of the present invention;
- Fig. 3a shows a conventional control of a relay as a hardware resource by a digital test channel;
- 10 Fig. 3b schematically depicts an impact of a change of the hardware resource according to Fig. 3a in a conventional test concept;
- Fig. 3c shows a test channel integrated circuit coupled to a resource control means for a translation of logical channel control commands to dedicated channel control commands, according to an embodiment of the present invention;
- 15 Fig. 4a shows a conventional configuration of test channel ICs communicating with dedicated hardware resources via channel specific communication ports;
- 20 Fig. 4b schematically shows the usage of a shared resource control means communicating with a multi-channel hardware resource via a single communication port;
- Fig. 5a schematically shows a conventional setup of various tests channels using dedicated hardware resources, respectively;
- 25 Fig. 5b shows a concept of a shared resource control means communicating with a single hardware resource used for a plurality of test channels in a multiplex scheme, according to an embodiment of the present invention;
- 30 Fig. 6 schematically shows a block diagram of an ATE using the inventive concept; and
- Fig. 7 shows connections of a shared resource control means according to an embodiment of the present invention.
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The following description sets forth specific details such as particular embodiments, procedures, techniques, etc. for purposes of explanation and not limitation. It will be

appreciated by those skilled in the art that other embodiments may be employed apart from these specific details. For example, although the following description is facilitated using non-limiting example applications, the technology may be employed to any type of ATE. In some instances, detailed descriptions of well-known methods, interfaces, circuits and devices are omitted so as to not obscure the description with unnecessary detail. Moreover, individual blocks are shown in some of the figures. Those skilled in the art will appreciate that the functions of those blocks may be implemented using individual hardware circuits, using software programs and data, in conjunction with a suitably programmed digital micro processor or general purpose computer, using application-specific integrated circuitry (ASIC) and/or using one or more digital signal processors (DSPs).

Fig. 2 schematically shows a block diagram of an apparatus 200 for testing a device-under-test according to an embodiment of the present invention.

The apparatus 200, which may be comprised of an ATE, comprises a digital pattern processing or test channel IC 240-n ($n=1,2,\dots,N$) adapted to communicate with an I/O pin of the DUT 130 by means of a (analog) hardware resource 150-n ($n=1,2,\dots,N$). The test channel IC 240-n ($n=1,2,\dots,N$) is coupled to a resource control means 260. The resource control means 260 receives from the test channel IC 240-n ($n=1,2,\dots,N$) a logical control command U-CTRL describing a desired operation of the hardware resource 150-n ($n=1,2,\dots,N$), wherein the resource control means 260 is adapted to convert the logical control command U-CTRL into a dedicated control command D-CTRL for the hardware resource 150-n ($n=1,2,\dots,N$), wherein the dedicated control command D-CTRL is adapted to an actual physical implementation of the hardware resource 150-n ($n=1,2,\dots,N$).

The logical control command U-CTRL from the test channel IC 240-n ($n=1,2,\dots,N$) is dependent on the genus or species of the hardware resource 150-n ($n=1,2,\dots,N$), i.e., whether the hardware resource 150-n ($n=1,2,\dots,N$) is, e.g., of the genus/species ADC, DAC, switch, voltage/current level driver, etc. On the other hand, the logical control command U-CTRL received from the test channel IC 240-n ($n=1,2,\dots,N$) is independent from the actual physical implementation of the hardware resource 150-n ($n=1,2,\dots,N$), i.e., independent from whether the hardware resource 150-n ($n=1,2,\dots,N$) is, e.g., an ADC-x or an ADC-y. This means, that the logical control command U-CTRL is uniform for a certain genus of hardware resource and describes the desired operation of the hardware resource 150-n ($n=1,2,\dots,N$) abstractly. E.g., for the hardware resource genus "switch", the logical control command U-CTRL may e.g. be of the binary form "open" (switch) or "close" (switch). For other hardware resource species, the respective logical control commands U-

CTRL may similarly describe abstract hardware resource operations, like, e.g., “sample” for the species ADC.

- The resource control means 260 then translates the abstract logical control command U-CTRL into hardware-resource-specific dedicated control commands D-CTRL which specifically address, control or program the external hardware resource 150-n ($n=1,2,\dots,N$) in a manner appropriate to its specific physical implementation. This will be explained with reference to the hardware-resource genus “switch” and referring to the Figs. 3a-3c.
- Fig. 3a shows a conventional connection of a relay, which is an electrically operated switch, as hardware resource 150-n ($n=1,2,\dots,N$) connected between a test channel IC 140-n ($n=1,2,\dots,N$) and a DUT 130. The test channel IC 140-n ($n=1,2,\dots,N$) comprises a data line 310 for transmitting and/or receiving a test pattern to or from the DUT. Additionally, the test channel IC 140-n ($n=1,2,\dots,N$) comprises a dedicated control signal line 320 for transmitting dedicated, hardware-specific control commands D-CTRL from the test channel IC 140-n ($n=1,2,\dots,N$) to the relay 150-n ($n=1,2,\dots,N$). For the relay 150-n ($n=1,2,\dots,N$) the hardware-specific control commands D-CTRL are simply “On”/“Off”, which may be coded using only one single bit (“1”/“0”).
- An economic alternative to the relay 150-n ($n=1,2,\dots,N$) would be an electronic switch 350-n ($n=1,2,\dots,N$) that is integrated as a part of a pin electronic chip and can perform other measurement functions as well, see Fig. 3b. Due to a silicon implementation of the switch 350-n ($n=1,2,\dots,N$), special care is required during the switching process. E.g., in order to prevent spikes while switching, there is a need for a sequence of events (or dedicated hardware-specific control commands D-CTRL) that should be followed when using the electronic switch 350-n ($n=1,2,\dots,N$) instead of the relay 150-n ($n=1,2,\dots,N$). I.e., the simple control command “On”/“Off” for the relay 150-n ($n=1,2,\dots,N$), which can also be regarded as a logical control command for the relay/switch, has to be translated into a sequence of dedicated control commands D-CTRL applicable for the electronic switch 350-n ($n=1,2,\dots,N$), like, e.g., “turn on the voltage clamping”, “turn on the switch”, then “release the clamping”. While in a traditional ATE according to the principle of Fig. 3a, the test channel IC 140-n ($n=1,2,\dots,N$) has to send a single bit, “0”, “1” corresponding to “Off”/“On”, the test channel IC 340-n ($n=1,2,\dots,N$) needs to adapt to the protocol that is required by the pin electronics, e. g. SPI (Serial Peripheral Interface Bus). Moreover, the channel IC 340-n ($n=1,2,\dots,N$) has to follow a sequence of events for a safe switching that is required by the pin electronics chip 350-n ($n=1,2,\dots,N$). Therefore, a dedicated pin electronic solution would have to be built within the channel IC 140-n ($n=1,2,\dots,N$). However, modifying the test channel IC 140-n ($n=1,2,\dots,N$), or, more specifically, the

channel-specific channel control block 111 thereof, is an expensive and time consuming process. Also, the test software running on the central test control unit 120 would have to be adapted.

- 5 The example of Figs. 3a and 3b shows, that each time external hardware resources are changed and, consequently, a different handling thereof is required, the test channel IC 140-n ($n=1,2,\dots,N$) would have to be adapted again. This can be avoided by applying the inventive concept, which will be detailed with reference to Fig. 3c.
- 10 According to embodiments of the present invention, it is separated between the logical control commands U-CTRL, e. g. "1"/"0" ("On"/"Off"), and the dedicated control commands D-CTRL including the sequence of control events that are required by the new external resource 350-n ($n=1,2,\dots,N$). As can be seen from Fig. 3c, the conversion from the logical control commands U-CTRL to the dedicated control commands D-CTRL is
- 15 handled by the inventive resource control means 260, while the test channel IC 240-n ($n=1,2,\dots,N$) always keeps a uniform control interface with uniform logical control commands U-CTRL, even when the external resources are replaced and, hence, require a different handling. The resource control means 260 is, according to an embodiment of the present invention, adapted to translate the uniform logical control commands U-CTRL that
- 20 come from the test pattern processing or test channel IC 240-n ($n=1,2,\dots,N$) into the dedicated control commands D-CTRL, communication protocols and/or sequence of events that are required due to the physical implementation of the associated external hardware resource. This allows saving costs because the test channel IC 240-n ($n=1,2,\dots,N$) does not have to be adapted each time when changing associated hardware
- 25 resources for communicating with DUTs. Hence, development time may be saved.

A further embodiment of the present invention shall now be explained with reference to Figs. 4a and 4b.

- 30 Fig. 4a schematically shows a traditional ATE-setup, wherein each test channel IC 140-n ($n=1,2,3$) comprises its own control line 320-n ($n=1,2,3$) and its own transceiver 420-n ($n=1,2,3$) to external resources 350-n ($n=1,2,3$). E.g., the dedicated control communication may be implemented according to a synchronous serial data link standard such as, e. g., the serial peripheral interface bus (SPI).

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For some test scenarios, the individual channel-specific hardware resources 350-n ($n=1,2,3$) could be replaced by a hardware resource having a so-called multi-channel port.

An example could be a two-channel driver as a single chip and with only a single control port according to SPI. A similar scenario is exemplarily illustrated in Fig. 4b.

Fig. 4b shows an external multi-channel hardware resource chip 450 comprising a plurality of test pattern data ports for the plurality of test pattern data lines 310-n ($n=1,2,3$) from the plurality of specific test channel ICs 240-n ($n=1,2,3$). However, the multi-channel hardware resource 450 only comprises a single control port 460 for receiving dedicated control commands D-CTRL from the test channel IC 240 (comprising the individual test channel ICs 240-n ($n=1,2,3$)). According to the embodiment depicted in Fig. 4b, the resource control means 260 is shared by the plurality of the individual test channel ICs 240-n ($n=1,2,3$) and is adapted to multiplex different logical control commands U-CTRL-n ($n=1,2,3$) from the different individual test channel integrated circuits 240-n ($n=1,2,3$) to a single control data port 470 of the shared resource control means 260, which may be coupled to the multi-channel control port 460 of the multi-channel hardware resource 450. I.e., the resource control means 260, which is a shared resource control means between the different test channel ICs 240-n ($n=1,2,3$), receives individual logical control commands U-CTRL-n ($n=1,2,3$) from the individual test channel IC's 240-n ($n=1,2,3$), respectively, and converts the received individual logical control commands into multiplexed dedicated control commands D-CTRL. The multiplexing may be done on the test channel IC 240 such that the multiplexed dedicated control commands are communicated via the single control data port 470 to the external multi-channel hardware resource 450. This may save I/O pins on both ends and does not require multiple transceivers (SPI master/slave), like shown in Fig. 4a.

A third embodiment of the present invention will now be described with reference to Figs. 5a and 5b.

Fig. 5a shows a conventional ATE setup including a pattern processing test channel IC 140 with a plurality of individual test channel ICs 140-n ($n=1,2,3$) in communication with external hardware resources 350-n, 550-n ($n=1,2,3$), respectively. For the communication with both external hardware resources 350-n, 550-n ($n=1,2,3$), the individual test channel ICs 140-n ($n=1,2,3$) transmit dedicated control commands D-CTRL to both the external hardware resources 350-n, 550-n ($n=1,2,3$), respectively. In the example shown in Fig. 5a, each individual conventional test channel IC 140-n ($n=1,2,3$) configures its own DAC 550-n ($n=1,2,3$).

In case the different test channel ICs 140-n ($n=1,2,3$) do not need to access their associated DACs 550-n ($n=1,2,3$) temporally in parallel, the setup of Fig. 5a may be heavily

simplified with respect to communication port and hardware resource count by applying embodiments of the present invention. In case the individual test channel ICs 140-n ($n=1,2,3$) subsequently access the individual DACs 550-n ($n=1,2,3$), the embodiment schematically shown in Fig. 5b allows a significant reduction of external hardware resources.

According to Fig. 5b only one common general hardware resource 550 (for example a DAC) is used for the plurality of individual test channel ICs 240-n ($n=1,2,3$). The common general resource 550 is not a physical part of the individual test channels, however, it is virtually seen by each test channel as a dedicated hardware resource although physically only a single or only a few instances of it exist. This shared hardware resource 550 is controlled by the shared resources control means 260, which can prioritize the usage control between the individual test channels or test channel ICs 240-n ($n=1,2,3$). For this reason, the shared resource control means 260 is, according to an embodiment, adapted to temporally schedule different logical control commands U-CTRL-n ($n=1,2,3$) from the different test channel ICs 240-n ($n=1,2,3$), such that the different channel test channel ICs 240-n ($n=1,2,3$) may subsequently access the single external hardware resource 550 according to multiplexing scheme, such as, e. g., a time division multiple access (TDMA) scheme. In this case the shared resources control means 260 receives the logical control commands U-CTRL-n ($n=1,2,3$) from the plurality of test channel ICs 240-n ($n=1,2,3$) and schedules their conversion to dedicated control commands D-CTRL for the common hardware resource 550. If, e. g., test channel IC 240-1 wants to access the hardware resource (e.g. DAC) 550 temporarily before the test channel IC 240-2, the shared resources control means 260 schedules the respective translated dedicated control commands D-CTRL accordingly. I.e., first, dedicated control commands D-CTRL-1 corresponding to logical control commands U-CTRL-1 of test channel IC 240-1 are communicated to the DAC 550 together with a MUX-control signal for controlling a multiplexer 560, such that the DAC 550 operates according to the needs of test channel 1. Subsequently, dedicated control commands D-CTRL-2 corresponding to logical control commands U-CTRL-1 of test channel IC 240-2 are communicated to the common DAC 550 together with the MUX-control signal for controlling the multiplexer 560.

According to the embodiment of Fig. 5b virtually every test channel n ($n=1,2,3$) sees the common DAC 550 and may configure it exactly like in the situation corresponding to Fig. 5a. Also, test software that already exists may be kept. In fact, there is only a single DAC 550 that may be shared between the different test channels n ($n=1,2,3$). The shared resources control block 260 reacts to each channel-specific logical DAC control command, and decides on which channel to physically connect to the common DAC 550 by means of

the external multiplexer 560. For certain tests, the shared resources control block 260 allows each channel to access the DAC 550 in a time sharing manner. For other tests, however, sometimes there is only one DAC 550 required in the setup and the shared resources control means 260 allows connecting it to that test channel in an automatic way without doing anything specific for that test channel.

The ATE-setup according to Fig. 5b can save external resources, costs, electrical power and space on printed circuit boards (PCBs). The external resource 550 is no longer dedicated to a single test channel. In this example only one single DAC serves multiple test channels, while the shared resources control means 260 schedules and multiplexes it to the appropriate test channel.

An overview of an ATE 600 according to an embodiment of the present invention with a shared resources control block 260 is shown in Fig. 6.

The shared resources control means 260 is coupled to the channel control instance 611 of each individual test channel IC 140-n ($n=1,2,\dots,N$). I.e., the common shared resources control means 260 is fed from each individual test channel IC 140-n ($n=1,2,\dots,N$) and is seen by each test channel as a dedicated channel resource block. The shared resources control means 260 is adapted to receive uniformed channel commands U-CTRL from the respective channel specific control blocks 611-n ($n=1,2,\dots,N$) and to generate appropriate signals, communication protocols and sequences of control events that are required by the external channel resources 615, 616.

Some of the external hardware resources may have multi-channel ports, such as, e. g., two channel drivers as a single chip and with a single control port (e. g. SPI). In this case the shared resources control means 260 can multiplex logical control commands U-CTRL from a plurality of test channel ICs 140-n ($n=1,2,\dots,N$) and translate them to a single required resource communication protocol as has been explained with reference to Fig. 4b.

Common general resources 650 that are not part of a test channel are virtually seen by each test channel IC 140-n ($n=1,2,\dots,N$) as a dedicated resource. However, physically only a single or a few instances of it exists. This common general resource 650 is controlled by the shared resources control means 260 which can prioritize the usage control between the different test channels. E.g., a plurality of test channels may have access to a single A/D or D/A converter, as has been described with reference to Fig. 5b.

Referring now to Fig. 7, the (shared) resource control means 260 may be realized in the form of a microprocessor, which may be located within a housing of a main test channel IC 240 comprising the individual test channel ICs 240-n ($n=1,2,\dots,N$). However, the resource control means 260 may also be located physically outside the housing of the test channel IC 240. It may be implemented as software running on the microprocessor. Another method of implementation is dedicated hardware, such as an ASIC or a software state machine.

As illustrated, the (shared) resource control means 260 comprises various connections or interfaces, such as a configuration channel 710, connections 720 to external general purpose I/O pins which can interface to various external hardware resources, and connections 730 to the individual test channel ICs 240-n ($n=1,2,\dots,N$) using a unified protocol, i.e. the logical control commands (U-CTRL).

Although some aspects of the present invention have been described in the context of an apparatus, it is clear that these aspects also represent a description of the corresponding method, where a block or device corresponds to a method step or a feature of a method step. Analogously, aspects described in the context of a method step also represent a description of a corresponding block or item or feature of a corresponding apparatus.

Depending on the circumstances, the inventive concept may be implemented in hardware or software. The implementation may be done on a digital storage medium, particularly a disk, CD or DVD with electronically readable control signals, which may cooperate with a programmable computer system such that the method for testing a DUT is executed. In general, the invention thus also consists of a computer program product with a program code stored on a machine-readable carrier for performing the inventive method when the computer program product runs on a computer. In other words, the invention may thus be realized as a computer program with a program code for performing the method for testing a DUT when the computer program runs on a computer or a digital signal processor.

While this invention has been described in terms of several preferred embodiment, there are alterations, permutations and equivalents, which fall within the scope of this invention. It should also be noted that there are many alternative ways of implementing the methods and compositions of the present invention. It is therefore intended that the following appended claims be interpreted as included all such alterations, permutations and equivalents as falling within the true spirit and scope of the present invention.

Claims

1. An apparatus (200; 600) for testing a device-under-test (130), the apparatus comprising:
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a test channel integrated circuit (240) adapted to communicate with an input or output pin of the device-under-test (130) by means of a hardware resource (150; 350; 450; 550; 615; 616; 650); and
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a resource control means (260) coupled to the test channel integrated circuit (240) to receive a logical control command (U-CTRL) describing a desired operation of the hardware resource (150; 350; 450; 550; 615; 616; 650), wherein the resource control means (260) is adapted to convert the logical control command (U-CTRL) into a dedicated control command (D-CTRL) for the hardware resource, wherein
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the dedicated control command (D-CTRL) is adapted to a physical implementation of the hardware resource (150; 350; 450; 550; 615; 616; 650).
2. The apparatus according to claim 1, wherein the logical control command (U-CTRL) received from the test channel integrated circuit (240) is independent from
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the physical implementation of the hardware resource (150; 350; 450; 550; 615; 616; 650).
3. The apparatus according to claim 1 or 2, wherein the test channel integrated circuit (240) comprises, for communicating with the input or output pin of the device-under-test (130), a digital test pattern generator (112) for generating a digital test pattern and a time formatter (114) for associating a timing to binary values of the
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digital test pattern.
4. The apparatus according to one of the preceding claims, wherein the test channel integrated circuit (240) comprises, for communicating with the input or output pin of the device-under-test (130), a digital test pattern comparator (113) for comparing a test pattern received from the pin with an expected digital test pattern.
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5. The apparatus according to one of the preceding claims, wherein the hardware resource (150; 350; 450; 550; 615; 616; 650) is arranged externally to the test channel integrated circuit (240), and wherein the hardware resource (150; 350; 450; 550; 615; 616; 650) is adapted to connect the test channel integrated circuit (240) to the device-under-test (130) or adapted to convert a signal of a test pattern to or
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from the device-under-test (130) to a signal suited for the pin or the digital test channel integrated circuit (240).

5 6. The apparatus according to one of the preceding claims, comprising a plurality of test channel integrated circuits (240-n), wherein the resource control means (260) is shared by the plurality of test channel integrated circuits (240-n) and is adapted to multiplex different logical control commands (U-CTRL-n) from different test channel integrated circuits (240-n) to a single control data port (470) which may be coupled to a multi-channel port of a multi-channel hardware resource (450).

10 7. The apparatus according to one of the preceding claims, comprising a plurality of test channel integrated circuits (240-n), wherein the shared resource control means (260) is adapted to temporally schedule different logical control commands (U-CTRL-n) from different test channel integrated circuits (240-n), such that the
15 different test channel integrated circuits (240-n) may subsequently access a single hardware resource (550) in a time division multiplexing scheme.

20 8. The apparatus according to one of the preceding claims, wherein the shared resource control means (260) is re-configurable for adapting the shared resource control means to a physical implementation of an actually connected hardware resource (150; 350; 450; 550; 615; 616; 650).

25 9. A method for testing a device-under-test (130), the method comprising:

receiving, from a test channel integrated circuit (240) dedicated to communicate with an input or output pin of the device-under-test (130) by means of a hardware resource (150; 350; 450; 550; 615; 616; 650), a logical control command (U-CTRL) describing a desired operation of the hardware resource (150; 350; 450; 550; 615; 616; 650); and

30 converting the logical control command (U-CTRL) into a dedicated control command (D-CTRL) for the hardware resource, wherein the dedicated control command (D-CTRL) is adapted to a physical implementation of the hardware resource (150; 350; 450; 550; 615; 616; 650).

35 10. A computer-program for performing the method according to claim 9, when the computer-program is running on a computer or micro-controller.