

Description

Title of the invention: Piezoelectric-on-insulator (POI) substrate and process for producing a piezoelectric-on-insulator (POI) substrate.

[0001] The invention relates to a piezoelectric-on-insulator (POI) substrate and to a process for producing such a piezoelectric-on-insulator (POI) substrate.

[0002] A piezoelectric-on-insulator (POI) substrate comprises a thin layer of piezoelectric material on a support substrate joined together by a dielectric layer of silicon oxide that provides good adhesion between the layer of piezoelectric material and the support substrate.

[0003] Such substrates are used for acoustic wave devices such as sensors or filters. These devices have good performance by virtue of quality values Q and electromechanical coupling coefficients k^2 that are higher by comparison with other substrates of the prior art.

[0004] However, the support substrate material being silicon-based means there is a significant difference between the acoustic impedance of the support substrate and that of the dielectric layer of silicon oxide. This difference in acoustic impedance in the structure of the piezoelectric substrate gives rise to a loss of performance of the acoustic wave device produced on the POI substrate. This is because the difference in acoustic impedance between the support substrate and the dielectric layer of silicon oxide can create parasitic modes in the frequency bands used in acoustic wave devices (SAWs).

[0005] An aim of the invention is to overcome the abovementioned drawbacks and in particular to design a piezoelectric-on-insulator (POI) substrate having better characteristics for use in acoustic wave devices (SAWs).

[0006] The object of the invention is achieved by a piezoelectric-on-insulator (POI) substrate comprising a support substrate having a first acoustic impedance, a piezoelectric layer, especially a layer of lithium tantalate (LTO), lithium niobate (LNO), aluminium nitride (AlN), lead zirconate titanate (PZT), langasite or langatate, a dielectric layer having a second acoustic impedance and sandwiched between the piezoelectric layer and the support substrate, an intermediate layer positioned between the support substrate and the dielectric layer, characterized in that the intermediate layer is a layer having a variable composition, more particularly along its thickness, such that the acoustic impedance of the intermediate layer varies, especially in a gradual manner, between the values of the first and the second acoustic impedance. Thus, the variation

in the acoustic impedance of the intermediate layer makes it possible to gradually reduce the difference in acoustic impedance between the dielectric layer and the support substrate in a piezoelectric-on-insulator (POI) substrate and thus to reduce the losses in performance.

[0007] According to one embodiment, the support substrate may be a silicon-based substrate, the dielectric layer is a layer of silicon oxide and the intermediate layer is a layer of silicon oxynitride SiO_xN_y having a variable oxygen composition and/or a variable nitrogen composition. The use of a nitrogen-based intermediate layer situated between the piezoelectric layer and the support substrate makes it possible to reduce the diffusion of lithium or hydrogen into the support substrate while at the same time achieving an intermediate layer having a variable composition.

[0008] According to one embodiment, the variation in the oxygen composition and/or in the nitrogen composition of the intermediate layer is a gradual linear or a stepwise variation. The variation of the quantity q_t of the silicon oxynitride layer makes it possible to gradually vary the acoustic impedance of the intermediate layer. According to one embodiment, the variable composition of the intermediate silicon oxynitride SiO_xN_y layer is defined by the quantity $q_t = y/(y+x)$ and may vary along its thickness, more particularly where q_t is 0 at the interface with the dielectric layer and q_t is at least 0.4 at the interface with the support substrate. The variation of the quantity q_t along the thickness of the silicon oxynitride layer makes it possible to gradually reduce the difference in acoustic impedance between the dielectric layer and the support substrate.

[0009] According to one embodiment concerned with longitudinal waves, the quantity q_t at the interface with the support substrate may be equal to about $q_t = 0.5$ since the acoustic impedance Z is equal to $19.4 \cdot 10^6 \text{ Pa} \cdot \text{s/m}$ for a support substrate of the Si (100) type, the quantity x may be equal to about $q_t = 0.68$ since $Z = 21.1 \cdot 10^6 \text{ Pa} \cdot \text{s/m}$ for a support substrate of the Si (110) type, and the quantity q_t may be equal to about $q_t = 0.7$ since $Z = 21.6 \cdot 10^6 \text{ Pa} \cdot \text{s/m}$ for a support substrate of the Si (111) type. The variation of the quantity q_t at the interface with the support substrate makes it possible to adjust the acoustic impedance to the acoustic impedance of the support substrate according to its crystal orientation.

[0010] Depending on the mode of propagation of relevance to the acoustic device, that is to say either a longitudinal propagation wave or a slow or fast shear wave, other optimized values may be determined.

[0011] According to one embodiment, the quantity qt of the silicon oxynitride SiO_xN_y layer may vary in an increasing manner between the interface with the dielectric layer of the piezoelectric layer and the interface with the support substrate, especially in a stepwise or linear increasing manner. In this way, it is again possible to further reduce the negative effect of differences in acoustic impedance.

[0012] According to one embodiment, the piezoelectric-on-insulator (POI) substrate may further comprise a trapping layer on the solid support substrate, especially a polycrystalline silicon-based layer. The presence of a trapping layer on the support substrate makes it possible to improve the piezoelectric-on-insulator substrate while reducing energy loss in the support substrate. The trapping layer being silicon-based, like the support substrate, it is therefore possible to use the intermediate layer in contact with the trapping layer and to reduce the difference in acoustic impedance in the same way as described above.

[0013] The object of the invention is also achieved by a process for producing a piezoelectric-on-insulator (POI) substrate comprising the steps of providing a support substrate having a first acoustic impedance, especially a silicon-based substrate, providing a piezoelectric substrate, especially a lithium tantalate (LTO), lithium niobate (LNO), aluminium nitride (AlN), lead zirconate titanate (PZT), langasite or langatate substrate, forming a dielectric layer having a second acoustic impedance on the piezoelectric substrate, especially a layer of silicon oxide, forming an intermediate layer on a free surface of the support substrate, especially a layer based on silicon oxynitride SiO_xN_y , the intermediate layer having a variable composition, more particularly along its thickness, such that the acoustic impedance of the intermediate layer varies, especially in a gradual manner, between the values of the first and the second acoustic impedance, and joining the piezoelectric substrate with the dielectric layer with the support substrate with the intermediate layer. Thus, the variation in the acoustic impedance of the intermediate layer makes it possible to gradually reduce the difference in acoustic impedance between the dielectric layer and the support substrate in the piezoelectric-on-insulator substrate and thus to reduce the losses in performance in the piezoelectric-on-insulator (POI) substrate.

[0014] According to one embodiment, the joining between the piezoelectric substrate and the support substrate may be achieved between the intermediate layer and the dielectric layer. The intermediate layer being SiO_xN_y -based, the joining interface results in the formation of bonds of oxide-oxide type, which are known for being stable.

[0015] According to one embodiment, the process may further comprise a step of forming of a dielectric layer on the intermediate layer of the support substrate before the joining step, such that the joining is then achieved between the dielectric layer of the support substrate and the dielectric layer of the piezoelectric substrate. The joining interface of the support substrate with the piezoelectric layer is created at the interface between two dielectric layers and has bonds of the oxide-oxide type, more particularly a bond of the silicon oxide-silicon oxide type, which is a stable bond.

[0016] According to one embodiment, the step of forming of the intermediate layer on the support substrate may comprise the formation of a layer based on silicon oxynitride SiO_xN_y in which the variable composition qt of the silicon oxynitride SiO_xN_y layer defined by the quantity $qt_1 = y/(y+x)$ varies along its thickness, more particularly where qt_1 is 0 at the interface with the dielectric layer and qt_1 is at least 0.4 at the interface with the support substrate. Given that the impedance of the intermediate layer varies between a value close to the impedance value of the dielectric layer at the interface with the dielectric layer and a value close to the impedance value of the support substrate, the intermediate layer makes it possible to adjust the acoustic impedances of the different piezoelectric-on-insulator (POI) substrate materials obtained by the process so as to reduce the difference in acoustic impedance of the piezoelectric-on-insulator substrate. The piezoelectric-on-insulator (POI) substrate obtained thus has an acoustic impedance that is better adapted to the use of the substrate in acoustic wave devices, since this results in a reduction in parasitic effects in the frequency bands used in acoustic wave devices.

[0017] According to one embodiment, the step of forming of the intermediate layer on the support substrate may comprise the formation of a layer based on silicon oxynitride SiO_xN_y in which the quantity qt_2 of the silicon oxynitride SiO_xN_y layer defined by $qt_2 = y/(y+x)$ varies along its thickness, more particularly where qt_2 is at least 0.4 at the interface with the support substrate, and the process may further include a step of forming of a SiO_xN_y layer on the dielectric layer of the piezoelectric substrate before the joining step, said SiO_xN_y layer having a quantity qt_3 for the silicon oxynitride SiO_xN_y layer defined by $qt_3 = y/(y+x)$ that varies along its thickness, more particularly $qt_3 = 0$ at the interface with the dielectric layer of the piezoelectric substrate, such that joining is then achieved between the SiO_xN_y layer of the support substrate and the SiO_xN_y layer of the piezoelectric substrate, where qt_2 is equal to qt_3 at the interface between the SiO_xN_y layers of the piezoelectric substrate and the support substrate.

[0018] The joining interface of the support substrate with the piezoelectric layer is created at the interface between two intermediate layers based on silicon oxynitride SiO_xN_y and has bonds of the oxide-oxide type, which permit a stable bond.

[0019] According to one embodiment, the process may further comprise a step of forming of a trapping layer on the support substrate, especially a polycrystalline silicon-based layer. The presence of a trapping layer on the support substrate makes it possible to improve the piezoelectric-on-insulator substrate while reducing energy loss in the support substrate. The trapping layer being silicon-based, like the support substrate, it is therefore possible to use the intermediate layer in contact with the trapping layer and to reduce the difference in acoustic impedance in the same way as described above.

[0020] According to one embodiment, the step of forming of the intermediate layer may be carried out by radiofrequency sputtering in a mixed oxygen and nitrogen atmosphere.

[0021] The object of the invention is also achieved by an acoustic wave device (SAW) comprising a piezoelectric-on-insulator substrate as described above. Such a SAW device exhibits a reduction in parasitic effects in the frequency bands at which the device is operated through the adjustment of the acoustic impedance between the support substrate and the dielectric layer of the piezoelectric-on-insulator (POI) substrate.

[0022] The invention and its advantages will be explained in more detail below by means of preferred embodiments and supported in particular by the accompanying figures that follow, in which the reference numbers identify characteristics of the invention.

[0023] [Figure 1] is a schematic representation of a piezoelectric-on-insulator (POI) substrate according to a first embodiment of the invention.

[0024] [Figure 2] shows the variation in the velocity of sound in the intermediate layer as a function of the quantity q_t of the composition of the intermediate layer for q_t values corresponding to $q_t = 0$, $q_t = 0.33$, $q_t = 0.50$, $q_t = 0.68$ and $q_t = 1$, according to the first embodiment of the invention.

[0025] [Figure 3] depicts the variation in acoustic impedance of the intermediate layer as a function of the quantity q_t of the intermediate layer according to the first embodiment of the invention.

[0026] [Figure 4] is a schematic representation of a piezoelectric-on-insulator (POI) substrate according to a first variant of the first embodiment of the invention.

[0027] [Figure 5a] is a schematic representation of a process for producing a piezoelectric-on-insulator (POI) substrate according to a second embodiment of the invention.

[0028] [Figure 5b] is a schematic representation of a process for producing a piezoelectric-on-insulator (POI) substrate according to a first variant of the second embodiment of the invention.

[0029] [Figure 5c] is a schematic representation of a process for producing a piezoelectric-on-insulator (POI) substrate according to a second variant of the second embodiment of the invention.

[0030] The invention will be described in more detail using advantageous embodiments in an exemplary manner and with reference to the drawings. The embodiments described are simply possible configurations and it should be kept in mind that the individual characteristics as described above can be provided independently of one another or can be omitted entirely in the implementation of the present invention.

[0031] [Figure 1] is a schematic representation of a piezoelectric-on-insulator (POI) substrate according to a first embodiment of the invention.

[0032] The piezoelectric-on-insulator (POI) substrate 100 comprises a support substrate 102 joined to a piezoelectric layer 104 via an intermediate layer 106 positioned on the support substrate 102 that is in direct contact with the support substrate 102 at the interface 108 and with a dielectric layer 110 at the interface 112. The dielectric layer 110 is in direct contact with the piezoelectric layer 104 at the interface 114.

[0033] The support substrate 102 may be a silicon-based substrate, especially a silicon-based solid substrate. The support substrate 102 may be a crystalline or polycrystalline substrate. The support substrate 102 based on crystalline silicon may have an orientation (111), an orientation (100) or else an orientation (110). The silicon (100) has an acoustic impedance Z equal to $19.4 \cdot 10^6 \text{ Pa} \cdot \text{s/m}$, the silicon (111) has an acoustic impedance of $Z = 21.6 \cdot 10^6 \text{ Pa} \cdot \text{s/m}$, the silicon (110) has an acoustic impedance of $Z = 21.1 \cdot 10^6 \text{ Pa} \cdot \text{s/m}$.

[0034] According to the invention, the dielectric layer 110 is a silicon oxide-based layer having a thickness between 100 and 900 nm, more particularly between 200 and 700 nm. The dielectric layer 110 has a second acoustic impedance that is different from the first acoustic impedance of the support substrate 102, since the silicon oxide has an acoustic impedance of between $11.5 \cdot 10^6 \text{ Pa} \cdot \text{s/m}$ and $14 \cdot 10^6 \text{ Pa} \cdot \text{s/m}$, more particularly

about $13.7 \cdot 10^6$ Pa·s/m. In one variant, the dielectric layer 110 may also be a silicon nitride-based layer or a layer comprising a combination of silicon nitride and silicon oxide SiO_xN_y in which the amount of nitride in the layer is constant.

[0035] The piezoelectric layer 104 is a layer based on a piezoelectric material having a thickness of between 200 nm and 700 nm. The piezoelectric material may for example be lithium tantalate (LTO), lithium niobate (LNO), aluminium nitride (AlN), lead zirconate titanate (PZT), langasite or langatate.

[0036] The intermediate layer 106 is a layer having a variable composition, more particularly along its thickness e_I . The variation in the composition of the intermediate layer 106 is such that the acoustic impedance of the intermediate layer 106 varies between the values of the first and the second acoustic impedance of the support substrate 102 and of the dielectric layer 110 respectively. The variable acoustic impedance of the intermediate layer 106 makes it possible to limit the influence of the difference in acoustic impedance between the dielectric layer 110 and the support substrate 102 of the POI substrate 100 when gradually passing from the first impedance value to the second impedance value.

[0037] According to one embodiment of the invention, the intermediate layer 106 is a layer based on silicon oxynitride SiO_xN_y . The thickness e_I of the intermediate layer 106 is between 100 nm and 1000 nm, more particularly between 200 nm and 1000 nm.

[0038] The intermediate layer 106 of silicon oxynitride SiO_xN_y according to the invention has a stoichiometry that varies as a function of its thickness e_I so as to adjust its acoustic impedance. This is because the acoustic impedance of the layer depends on the variation in the amount of oxygen and/or the variation in the amount of nitrogen in the layer.

[0039] The values for x and y are set such that a desired or predetermined variation in the acoustic impedance is observed. The amount of oxygen and nitrogen in the intermediate layer 106 depends on the production process used to deposit the layer of SiO_xN_y .

[0040] According to one embodiment, the intermediate layer is produced as described in Grahn et al.: "Elastic properties of silicon oxynitride films determined by picosecond acoustics", Applied Physics Letters 53, 2281, 1988 so as to obtain a stoichiometry in the intermediate silicon oxynitride SiO_xN_y layer 106 that varies according to $qt_1(e_I) = y/(y+x)$. The SiO_xN_y layer is produced by radiofrequency sputtering (RF sputtering) in a mixed oxygen and nitrogen atmosphere. The composition of the SiO_xN_y layer is thus controlled

by varying the ratio $y/(y+x)$, which corresponds to the amount of nitrogen and the amount of nitrogen and oxygen in the atmosphere during deposition.

- [0041] The variation in the quantity qt of the silicon oxynitride SiO_xN_y layer 106 is a variation in the thickness e_l of the layer 106 between the two surfaces of the intermediate layer 106. In this first embodiment, the variation in the quantity qt_l of the silicon oxynitride SiO_xN_y layer 106 is an increasing variation between the interface 112 with the dielectric layer 110 and the interface 108 with the support substrate 102. The variation is for example a stepwise increase or is a linear increase.
- [0042] Figure 2 shows the variation in the velocity of the longitudinal acoustic wave V_{longi} in the intermediate layer 106 as a function of the quantity qt of nitrogen (N) in the intermediate layer 106 for values for the quantity qt in the intermediate layer 106 of 0, 0.33, 0.50, 0.68 and 1. This figure has been published by Grahn et al. "Elastic properties of silicon oxynitride films determined by picosecond acoustics", Applied Physics Letters 53, 2281, 1988.
- [0043] A linear increase in the velocity of the longitudinal acoustic wave as a function of an increase in the quantity qt of the intermediate layer 106 can also be seen. The line representing the linear variation is an adjustment by the least-squares method at the data points.
- [0044] Starting from the data in Figure 2, the acoustic impedance is obtained by calculating the acoustic impedance Z where $Z = V_{\text{longi}} \cdot \text{density}$, V_{longi} being the velocity of the longitudinal acoustic wave, according to Grahn et al.: "Elastic properties of silicon oxynitride films determined by picosecond acoustics", Applied Physics Letters 53, 2281 (1988).
- [0045] The variation in the acoustic impedance of the SiO_xN_y layer as a function of the quantity qt is illustrated in Figure 3. For a quantity qt equal to 0, the value for the acoustic impedance Z is equal to the value for the acoustic impedance Z of a layer of silicon oxide, this being of the order of $13.7 \cdot 10^6 \text{ Pa}\cdot\text{s/m}$. As the quantity qt increases, the acoustic impedance of the intermediate layer 106 increases continuously. For a value for quantity qt of between 0.5 and 0.7, the acoustic impedance Z becomes comparable to the acoustic impedance Z of silicon, which is between $19.4 \cdot 10^6 \text{ Pa}\cdot\text{s/m}$ and $21.8 \cdot 10^6 \text{ Pa}\cdot\text{s/m}$, depending on the crystalline orientation of the silicon. For $qt = 1$, the obtained acoustic impedance Z is that of Si_3N_4 , which is of the order of $25.5 \cdot 10^6 \text{ Pa}\cdot\text{s/m}$. However, this value for the acoustic impedance Z depends on the deposition techniques employed.

[0046] Thus, by varying the quantity qt_1 of the intermediate layer 106, a variation in the acoustic impedance value of the layer 106 can be obtained, a value that can vary between the acoustic impedance value of a layer of Si_3N_4 and that of a layer of silicon oxide. Starting from the values shown in Figure 3, it is possible to set the value for the quantity qt as a function of the position in the thickness e_1 of the SiO_xN_y layer.

[0047] On the basis of what is shown in Figure 3, $qt_1(e_1)$ is set at 0 in the intermediate layer 106 at the interface 112 with the dielectric layer 110. Thereafter, qt_1 increases as a function of the thickness e_1 until reaching a quantity $qt_1(e_1 = 0) \geq 0.4$, more particularly $qt_1(e_1 = 0) = 0.7$ at the interface with the support substrate. The acoustic impedance of the intermediate layer 106 at the interface 108 with the support substrate 102 ($e_1 = 0$) is thus of the order of the first acoustic impedance of the support substrate 102.

[0048] The intermediate layer 106 thus makes it possible to reduce the difference in acoustic impedance between the support substrate 102 and the dielectric layer of silicon oxide 110 by its acoustic impedance, which is between the impedance of the support substrate 102 and that of the dielectric layer 110.

[0049] In addition, the interface 112 between the dielectric layer 110 and the intermediate layer 106 is an interface that is free of nitrogen (N) and that comprises silicon oxide-silicon oxide bonds, which are known for being stable bonds that improve adhesion.

[0050] In addition, given that the intermediate layer 106 is a SiO_xN_y -based layer, the presence of nitrogen in the intermediate layer 106 makes it possible to reduce the diffusion of lithium or hydrogen into the support substrate 102.

[0051] The piezoelectric-on-insulator (POI) substrate 100 according to the invention thus exhibits improved stability and also improved characteristics for the use thereof in surface wave devices (SAWs) such as sensors, filters or the like. Reducing the difference in acoustic impedance in the piezoelectric-on-insulator (POI) substrate 100 results in a reduction in undesirable modes in the desired frequency ranges for the operation of surface wave devices (SAWs).

[0052] Figure 4 shows a variant of the first embodiment of the invention. The sole difference between the POI substrate 100 and the POI substrate 200 of the variant is the presence of a trapping layer 116 between the support substrate 102 and the intermediate layer 106. All other characteristics of the POI substrate are the same as those described in Figure 1. None of the characteristics common to the first embodiment

employing the same reference number as above will be described again, but reference is made to their detailed description above.

[0053] The trapping layer 116 is in contact with the support substrate 102 at the interface 118 and is also in contact with the intermediate layer 106 at the interface 120. The trapping layer 116 is sandwiched between the support substrate 102 and the intermediate layer 106.

[0054] The trapping layer 116 is a layer based on polycrystalline or amorphous or porous silicon, having a thickness of between 200 nm and 5 μm , more particularly between 500 nm and 2 μm . The trapping layer 116 has a third acoustic impedance with a value of about $21 \cdot 10^6 \text{ Pa} \cdot \text{s/m}$, this value being close to the average acoustic impedance value for the three possible silicon orientations mentioned above.

[0055] In this variant, the value of the quantity qt_1 of the variable composition of the silicon oxynitride SiO_xN_y layer 106 varies such that the acoustic impedance of the intermediate layer 106 at the interface 120 with the trapping layer 116 is of the order of the third acoustic impedance of the trapping layer 116.

[0056] The piezoelectric-on-insulator (POI) substrate 200 has the same advantages as the piezoelectric-on-insulator (POI) substrate 100 described in Figure 1.

[0057] Figure 5a is a schematic representation of a process for producing a piezoelectric-on-insulator (POI) substrate according to a second embodiment of the invention to obtain a POI substrate as described above in Figures 1 and 4 according to the first embodiment of the invention. Elements with the same reference numbers and the properties thereof will not be described again, but reference is made to their description above.

[0058] The process for producing a piezoelectric-on-insulator (POI) substrate 200 starts with step I) of providing a support substrate 102, in particular a silicon-based substrate, more particularly a crystalline or polycrystalline silicon substrate.

[0059] According to the invention, step II) consists of the forming of the trapping layer 116 on the free surface 122 of the support substrate 102. The forming of the trapping layer 116 may be achieved by a thermal or plasma-assisted growth technique such as PECVD (plasma-enhanced chemical vapor deposition) or PVD (physical vapor deposition).

[0060] The trapping layer 116 formed on the support substrate 102 is a layer based on silicon, especially polycrystalline silicon. The thickness of the trapping layer 116 is

between 200 nm and 5 μm , more particularly between 500 nm and 2 μm . The trapping layer 116 has a fourth acoustic impedance that may be the same as that of the support substrate 102 or it may be different.

[0061] In step III), the intermediate layer 106 is formed on the free surface 124 of the trapping layer 116.

[0062] The forming of the intermediate layer 106 may be achieved by a thermal or plasma-assisted growth technique such as LPCVD (low-pressure chemical vapor deposition) or PECVD (plasma-enhanced chemical vapor deposition).

[0063] The intermediate layer 106 is a layer based on silicon oxynitride SiO_xN_y . The thickness of the intermediate layer 106 is between 100 nm and 1000 nm, more particularly between 200 nm and 1000 nm.

[0064] To obtain the variable composition in the intermediate layer 106, the deposition parameters are varied during deposition so as to modify the amount of nitrogen and/or the amount of oxygen in the thickness of the deposited layer in a way that achieves the gradual variation in the composition of the deposited layer 106 necessary to obtain the desired acoustic impedance at the free upper surface 126 of the deposited layer 106, as explained above.

[0065] The variation in the composition of the deposited layer of silicon oxynitride SiO_xN_y is defined by $q_t = y/(y+x)$.

[0066] The variation in the quantity q_{t1} is a decreasing variation between the interface 108 with the support substrate 102 and the free upper surface 126 of the silicon oxynitride SiO_xN_y layer 106. The variation is a stepwise decrease or a linear decrease.

[0067] At the interface 118 with the support substrate 102, the quantity q_{t1} is at least equal to 0.4, more particularly the quantity q_{t1} is of the order of 0.7. The acoustic impedance of the intermediate layer 106 at the interface 118 with the support substrate 102 is thus of the order of the first acoustic impedance of the support substrate 102, more particularly it is the same.

[0068] At the free surface 126 of the intermediate layer 106, which is intended to contact another layer in a subsequent process step, the quantity q_{t1} is defined by the acoustic impedance value of the layer that is to be contacted with the free surface 126.

[0069] In step IV), the piezoelectric substrate 128 is provided.

[0070] In step V), the dielectric layer 110 is produced on the free surface 130 of the piezoelectric substrate 128. Before forming the dielectric layer 110, one or more steps of cleaning, brushing or polishing the surface 130 of the piezoelectric substrate 128 can be carried out to eliminate the presence of particles and dust in order to thus obtain a cleaner free surface 130, which makes it possible to obtain a deposited dielectric layer 110 of better quality.

[0071] The forming of the dielectric layer 110 on the free surface 130 of the piezoelectric substrate 128 can be achieved by a thermal or plasma-assisted growth technique such as LPECVD at low pressure and/or low temperature. A thermal treatment may be carried out after deposition of the dielectric layer 110 in order to densify the dielectric layer 110.

[0072] According to one variant, surface-treatment steps on the free surface 130 of the piezoelectric substrate 128 may be carried out before the formation of the dielectric layer 110. Examples include a surface activation treatment such as a plasma treatment or an ozone-based treatment.

[0073] According to the invention, the dielectric layer 110 is a layer of silicon oxide.

[0074] According to the invention, the piezoelectric substrate 128 obtained after step V) is then joined to the support substrate 102 obtained in step III) during a step VI) of joining to form a support substrate-piezoelectric substrate assembly 132. The joining of the piezoelectric substrate 128 on the support substrate 102 is achieved by positioning the intermediate layer 106 in contact with the dielectric layer 110 of the piezoelectric substrate 128 such that the intermediate layer 106 is sandwiched between the dielectric layer 110 of the piezoelectric substrate 128 and the support substrate 102. The intermediate layer 106 is thus in direct contact with the dielectric layer 110 of the piezoelectric substrate 128 at the interface 112.

[0075] In this structure, the acoustic impedance of the intermediate layer 106 at the free surface 126 is of the order of the acoustic impedance of the dielectric layer of silicon oxide 110. In addition, the bond between the substrates is created at an interface 112 that is essentially made of the same material on both sides of the interface 112.

[0076] Once the two substrates have been joined, a step (not illustrated) of thinning VII) of the piezoelectric substrate 128 may be carried out to obtain a thinner piezoelectric layer 104. For example, the thinning step may be carried out by grinding or by a step of forming a weakened zone in the piezoelectric substrate 128 in such a way as to delineate the piezoelectric layer 104 to be transferred onto the support substrate 102, and fracturing. This step of forming a weakened zone is carried out by implanting atomic

or ionic species in the piezoelectric substrate 128. The atomic or ionic implantation may be carried out in such a way that the weakened zone is situated inside the piezoelectric substrate 128 and separates a piezoelectric layer 104 from the remainder of the piezoelectric substrate 128.

[0077] This is followed by the performance of a step of fracturing of the support substrate-piezoelectric substrate assembly 132 through an input of thermal and/or mechanical energy at the weakened zone of the piezoelectric substrate 128 so as to obtain a piezoelectric-on-insulator (POI) substrate 200 as illustrated in step VII) of Figure 5a and in Figure 4 that has a thinner piezoelectric layer 104 on a support substrate 102.

[0078] This method may also be applied to obtain the substrate of Figure 1.

[0079] Figure 5b is a schematic representation of a process for producing a piezoelectric-on-insulator (POI) substrate according to a first variant of the second embodiment of the invention.

[0080] None of the characteristics common to the second embodiment employing the same reference number as above will be described again, but reference is made to their detailed description above.

[0081] The sole difference between this process and the one in Figure 5a consists of the formation IIIc) of a dielectric layer 134 on the free surface of the intermediate layer 106 after step III) of Figure 5a. The dielectric layer 134 is of the same material as the dielectric layer 110, i.e. silicon oxide. The dielectric layer 134 may be produced in the same way as the dielectric layer 110.

[0082] Thus, in the joining step VI), the dielectric layer 134 is contacted with the dielectric layer 110 of the piezoelectric substrate 128 at the interface 138. The assembly 140 is therefore created by molecular adhesion between the two dielectric layers 110 and 134 which are made of the same material, in this case silicon oxide. This achieves an improved bond between the substrates 102 and 128.

[0083] All other process steps in this variant are the same as the steps for the process according to the second embodiment described in Figure 5a for obtaining the (POI) substrate 200.

[0084] Figure 5c is a schematic representation of a process for producing a piezoelectric-on-insulator (POI) substrate according to a second variant of the second embodiment of the invention.

[0085] None of the characteristics common to the second embodiment and variants thereof employing the same reference number as above will be described again, but reference is made to their detailed description above.

[0086] The sole difference between this process and the one in Figure 5a consists of the separation of the intermediate layer 106 into two parts. Step III) of Figure 5a is replaced by two steps, IIIa) and IIIb). A first intermediate layer 144 is formed on the trap-rich layer 116 in step IIIa). A second intermediate layer 150 is produced on the dielectric layer 110 in step IIIb).

[0087] For the first intermediate layer 144 formed on the support substrate 102 and therefore on the trap-rich layer 116, the first layer 144 is deposited in such a way in step IIIa) that the quantity qt_2 of the variable composition of the first silicon oxynitride SiO_xN_y layer 144 varies along its thickness, where $qt_2(0)$ is at least 0.4 at the interface 146 with the trap-rich layer 116 of the support substrate 102.

[0088] The first layer 144 is deposited such that the quantity qt_2 of the first silicon oxynitride SiO_xN_y layer 144 varies in a decreasing manner along the thickness of the first intermediate layer 144.

[0089] At the free surface 148 of the first intermediate layer 144, the quantity qt_2 is set at the same value as that of the layer to be contacted in step VII). In this case, for example, $qt_2(e_2) = 0.2$.

[0090] For the second intermediate layer 150 formed on the piezoelectric substrate 128, the second layer 150 is deposited in such a way in step IIIb) that the quantity qt_3 of the variable composition of the second silicon oxynitride SiO_xN_y layer 150 varies along its thickness, where $qt_3(e_3 = 0)$ is 0 at its interface 152 with the dielectric layer 110.

[0091] The second layer 150 is deposited such that the quantity qt_3 of the second silicon oxynitride SiO_xN_y layer 150 varies in an increasing manner along the thickness e_3 of the intermediate layer 150.

[0092] At the free surface 154 of the second intermediate layer 150, the quantity qt_3 is the same as the quantity qt_2 at the free surface 148 of the first intermediate layer 144. In this case, therefore, $qt_3(e_3) = 0.2$.

[0093] Thus, in the joining step VI), the first intermediate layer 144 of the support substrate 102 is contacted with the second intermediate layer 150 of the piezoelectric substrate 128.

- [0094] As in the other processes described in relation to Figures 5a and 5b, the acoustic impedance varies across the first and second intermediate layers 144 and 150 between the value of the trap-rich layer 116 and the value of the dielectric layer 110.
- [0095] The assembly 156 is created by molecular adhesion between the two substrates 102 and 128 at the interface 158 between the first intermediate layer 144 and the second intermediate layer 150. The assembly 156 is therefore created by molecular adhesion between the two intermediate layers 144 and 150, which have essentially the same material at the interface, in this case the silicon oxynitride SiO_xN_y layer where $q_t = 0.2$. This achieves an improved bond between the substrates 102 and 128.
- [0096] All other process steps in this variant are the same as the steps for the process according to the second embodiment described in Figure 5a for obtaining the (POI) substrate 200.
- [0097] The process according to the second embodiment may also be used to produce the piezoelectric-on-insulator (POI) substrate 100 according to Figure 1 without the presence of a trap-rich layer 116 on the support substrate 102.
- [0098] The embodiments described are simply possible configurations and it should be kept in mind that the individual characteristics of the different embodiments can be combined with one another or provided independently of one another.

Claims

1. Piezoelectric-on-insulator (POI) substrate (100, 200) comprising:
 - a support substrate (102) having a first acoustic impedance,
 - a piezoelectric layer (104), especially a layer of lithium tantalate (LTO), lithium niobate (LNO), aluminium nitride (AlN), lead zirconate titanate (PZT), langasite or langatate,
 - a dielectric layer (110) having a second acoustic impedance and sandwiched between the piezoelectric layer (104) and the support substrate (102),
 - an intermediate layer (106) positioned between the support substrate (102) and the dielectric layer (110),

characterized in that

the intermediate layer (106) is a layer having a variable composition, more particularly along its thickness, such that the acoustic impedance of the intermediate layer (106) varies, especially in a gradual manner, between the values of the first and the second acoustic impedance.

2. Piezoelectric-on-insulator (POI) substrate (100, 200) according to Claim 1, wherein the support substrate (102) is a silicon-based substrate, the dielectric layer (110) is a layer of silicon oxide and the intermediate layer (106) is a layer of silicon oxynitride SiO_xN_y having a variable oxygen composition and/or a variable nitrogen composition.
3. Piezoelectric-on-insulator (POI) substrate (100, 200) according to Claim 1 or 2, wherein the variation in the composition of the intermediate layer (106) is a gradual linear or a stepwise variation.
4. Piezoelectric-on-insulator (POI) substrate (100, 200) according to any of Claims 1 to 3, wherein the variable composition of the intermediate silicon oxynitride SiO_xN_y layer (106) of the quantity q_t of the variable composition of the silicon oxynitride SiO_xN_y layer (106)

is defined by $q_t = y/(y+x)$ and varies along its thickness, more particularly where q_t is 0 at the interface (112) with the dielectric layer (110) and q_t is at least 0.4 at the interface (108) with the support substrate (102).

5. Piezoelectric-on-insulator (POI) substrate (100, 200) according to Claim 4, wherein the quantity q_t at the interface (108) with the support substrate (102) is equal to about 0.5 for a support substrate (102) of the type where Si has an orientation (100), q_t is equal to about 0.68 for a support substrate (102) of the type where Si has an orientation (110), and q_t is equal to about 0.7 for a support substrate (102) of the type where Si has an orientation (111).
6. Piezoelectric-on-insulator (POI) substrate (100, 200) according to Claim 4 or 5, wherein the quantity q_t of the silicon oxynitride SiO_xN_y layer (106) varies in an increasing manner between the interface (112) with the dielectric layer (110) of the piezoelectric layer (104) and the interface (108) with the support substrate (102), especially in a stepwise or linear increasing manner.
7. Piezoelectric-on-insulator (POI) substrate (100, 200) according to any of Claims 1 to 6, further comprising a trapping layer (116) on the support substrate (102), especially a polycrystalline silicon-based layer.
8. Process for producing a piezoelectric-on-insulator (POI) substrate according to any of Claims 1 to 7 comprising the steps of:
 - providing a support substrate having a first acoustic impedance, especially a silicon-based substrate,
 - providing a piezoelectric substrate, especially a lithium tantalate (LTO), lithium niobate (LNO), aluminium nitride (AlN), lead zirconate titanate (PZT), langasite or langatate substrate,

- forming a dielectric layer having a second acoustic impedance on the piezoelectric substrate, especially a layer of silicon oxide,
- forming an intermediate layer on a free surface of the support substrate, especially a layer based on silicon oxynitride SiO_xN_y , the intermediate layer having a variable composition, more particularly along its thickness e , such that the acoustic impedance of the intermediate layer varies, especially in a gradual manner, between the values of the first and the second acoustic impedance, and

joining the piezoelectric substrate with the dielectric layer with the support substrate with the intermediate layer.

9. Process for producing a piezoelectric-on-insulator (POI) substrate according to Claim 8, wherein the joining between the piezoelectric substrate and the support substrate is achieved between the intermediate layer and the dielectric layer.
10. Process for producing a piezoelectric-on-insulator (POI) substrate according to Claim 8, further comprising a step of forming of a dielectric layer on the intermediate layer of the support substrate before the joining step, such that the joining is then achieved between the dielectric layer of the support substrate and the dielectric layer of the piezoelectric substrate.
11. Process for producing a POI substrate according to any of Claims 8 to 10, wherein the step of forming of the intermediate layer on the support substrate comprises the formation of a layer based on silicon oxynitride SiO_xN_y in which the amount of nitrogen in relation to the oxygen in the silicon oxynitride SiO_xN_y layer defined by $qt_1 = y/(y+x)$ varies along its thickness e_1 , more particularly where qt_1 is 0 at the interface with the dielectric layer and qt_1 is at least 0.4 at the interface with the support substrate.
12. Process for producing a piezoelectric-on-insulator (POI) substrate according to Claim 8, wherein the step of forming of the intermediate layer on the support substrate comprises

the formation of a layer based on silicon oxynitride SiO_xN_y in which the quantity qt_2 of the silicon oxynitride SiO_xN_y layer defined by $qt_2 = y/(y+x)$ varies along its thickness e_2 , more particularly where qt_2 is at least 0.4 at the interface with the support substrate, and

the process further comprises a step of forming of a SiO_xN_y layer on the dielectric layer of the piezoelectric substrate before the joining step, said SiO_xN_y layer having a quantity qt_3 for the silicon oxynitride SiO_xN_y layer defined by $qt_3 = y/(y+x)$ that varies along its thickness e_3 , more particularly $qt_3 = 0$ at the interface with the dielectric layer of the piezoelectric substrate,

such that the joining is then achieved between the SiO_xN_y layer of the support substrate and the SiO_xN_y layer of the piezoelectric substrate, where qt_2 is equal to qt_3 at the interface between the SiO_xN_y layers of the piezoelectric substrate and the support substrate.

13. Process for producing a piezoelectric-on-insulator (POI) substrate according to any of Claims 8 to 12, further comprising a step of forming of a trapping layer on the support substrate, especially a polycrystalline silicon-based layer.

14. Process for producing a piezoelectric-on-insulator (POI) substrate according to any of Claims 8 to 13, wherein the step of forming of the intermediate layer is carried out by radiofrequency sputtering in a mixed oxygen and nitrogen atmosphere.

15. Surface acoustic wave device (SAW) comprising a piezoelectric-on-insulator substrate (100, 200) according to any of Claims 1 to 7.