

Published
With international search report.

SG 9612152-0

The diagram illustrates a packet-based digital transmission system, organized into several functional layers and networks:

- TRANSPORT LAYER:**
 - DATA SOURCE (2):** Provides input to the **TRANSPORT PROCESSOR (14)**.
 - TRANSPORT PROCESSOR (14):** Receives a **PACKET REQUEST TO TRANSPORT** and outputs **DATA VALID** and **MPER BYTE DATA** to the **FFIO**.
 - FFIO (First-In-First-Out):** Receives **DATA VALID** and **MPER BYTE DATA**. It outputs **SOP** (Start of Packet) to the **TRANSPORT PROCESSOR** and **PACKET ERROR** to the **ALIGNMENT** block.
 - ALIGNMENT (4):** Receives **PACKET ERROR** and outputs **DATA** to the **FORWARD ERROR CORRECTION INSERTION** block.
- INTERFACE:**
 - 30 SC GEN (30):** Generates **30 SC** (Symbol Clock) signals, providing one to the **TRANSPORT PROCESSOR** and another to the **TIMEING CONTROL** block.
 - 14 SC:** A clock signal provided to the **FFIO** and **ALIGNMENT** blocks.
 - 1/4 SC:** A clock signal provided to the **SYS. CONTROL** block.
 - 42:** A signal input to the **FFIO**.
 - 44:** A signal input to the **SYS. CONTROL** block.
 - 16:** A signal input to the **FFIO**.
- INTERFERENCE:**
 - TIMEING CONTROL (40):** Receives **30 SC** and **14 SC** signals. It outputs **DATA FIELD PACKET REQUEST** to the **FORWARD ERROR CORRECTION INSERTION** block and provides timing signals to the **FIELD/SYMBOL SYNC GEN.** and **PARALLEL-SERIAL BYTE TO BIT PAIR CONVERSION** blocks.
- FORWARD ERROR CORRECTION INSERTION (30):** Receives **DATA FIELD PACKET REQUEST** and **DATA VALID** signals. It outputs to the **PARALLEL-SERIAL BYTE TO BIT PAIR CONVERSION** block.
- PARALLEL-SERIAL BYTE TO BIT PAIR CONVERSION (32):** Receives input from the **FORWARD ERROR CORRECTION INSERTION** block and outputs to the **TRELLIS CODER**.
- TRELLIS CODER (34):** Receives input from the **PARALLEL-SERIAL BYTE TO BIT PAIR CONVERSION** block and outputs to the **TRELLIS BIT GEN.**
- TRELLIS BIT GEN. (36):** Receives input from the **TRELLIS CODER** and outputs to the **SYMBOL MAP AND MUX**.
- FIELD/SYMBOL SYNC GEN. (38):** Receives timing signals from the **TIMEING CONTROL** block and outputs to the **SYMBOL MAP AND MUX**.
- SYMBOL MAP AND MUX (39):** Receives input from the **TRELLIS BIT GEN.** and the **FIELD/SYMBOL SYNC GEN.**. It outputs **OUTPUT SYMBOL DATA** to the **OUTPUT PROCESSOR (MODULATOR)**.

- TRANSMISSION LAYER:**
- OUTPUT PROCESSOR (MODULATOR) (18):** Receives **OUTPUT SYMBOL DATA** and outputs **TO OUTPUT CHANNEL**.
- CODES AND DATA FIELD CONSTRUCTION NETWORK:** This network encompasses the **TIMEING CONTROL**, **FORWARD ERROR CORRECTION INSERTION**, **PARALLEL-SERIAL BYTE TO BIT PAIR CONVERSION**, **TRELLIS CODER**, **TRELLIS BIT GEN.**, **FIELD/SYMBOL SYNC GEN.**, and **SYMBOL MAP AND MUX** blocks.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AT	Austria	GB	United Kingdom	MR	Mauritania
AU	Australia	GE	Georgia	MW	Malawi
BB	Barbados	GN	Guinea	NE	Niger
BE	Belgium	GR	Greece	NL	Netherlands
BF	Burkina Faso	HU	Hungary	NO	Norway
BG	Bulgaria	IE	Ireland	NZ	New Zealand
BJ	Benin	IT	Italy	PL	Poland
BR	Brazil	JP	Japan	PT	Portugal
BY	Belarus	KE	Kenya	RO	Romania
CA	Canada	KG	Kyrgyzstan	RU	Russian Federation
CF	Central African Republic	KP	Democratic People's Republic of Korea	SD	Sudan
CG	Congo	KR	Republic of Korea	SE	Sweden
CH	Switzerland	KZ	Kazakhstan	SI	Slovenia
CI	Côte d'Ivoire	LI	Liechtenstein	SK	Slovakia
CM	Cameroon	LK	Sri Lanka	SN	Senegal
CN	China	LU	Luxembourg	TD	Chad
CS	Czechoslovakia	LV	Latvia	TG	Togo
CZ	Czech Republic	MC	Monaco	TJ	Tajikistan
DE	Germany	MD	Republic of Moldova	TT	Trinidad and Tobago
DK	Denmark	MG	Madagascar	UA	Ukraine
ES	Spain	ML	Mali	US	United States of America
FI	Finland	MN	Mongolia	UZ	Uzbekistan
FR	France			VN	Viet Nam
GA	Gabon				

9612152-0

TRANSPORT PROCESSOR INTERFACE FOR A DIGITAL TELEVISION SYSTEM

5

Field of the Invention

10 This invention is related to the field of digital signal processing. In particular, the invention concerns a system to facilitate transport processor operation while processing a field structured datastream suitable for conveying high definition television (HDTV) information.

15

Background of the Invention

Recent developments in the field of video signal processing have produced digital high definition television signal processing and transmission systems. One such system is described in US
20 Patent 5,168,356-Acampora et al. In that system, a codeword datastream, including codewords compatible with the known MPEG data compression standard, is conveyed to a transport processor. A major function of the transport processor is to pack variable length codeword data into packed data words. An
25 accumulation of packed data words, called a data packet or data cell, is prefaced by a header containing information identifying the associated data words, among other information. Thus an output from the transport processor is a packetized datastream comprising a sequence of transport packets. The transport packet
30 format enhances the prospects of resynchronization and signal recovery at a receiver, eg., after a signal disruption which may result from a transmission channel disturbance. This is accomplished by providing header data from which a receiver can determine re-entry points into the datastream upon a loss or
35 corruption of transmitted data.

A high definition television (HDTV) terrestrial broadcast system recently proposed as the Grand Alliance HDTV system in the United States employs a vestigial sideband (VSB) digital transmission format for transmitting a packetized datastream with a prescribed data field structure. The Grand Alliance HDTV system is a proposed transmission standard that is under consideration in the United States by the Federal Communications Commission (FCC) through its Advisory Committee of Advanced Television Service (ACATS). A description of the Grand Alliance HDTV system as submitted to the ACATS Technical Subgroup February 22, 1994 (draft document) is found in the 1994 Proceedings of the National Association of Broadcasters, 48th Annual Broadcast Engineering Conference Proceedings, March 20-24, 1994.

In the Grand Alliance system, data is arranged as a sequence of data fields. Each field structure includes 313 segments: a field sync segment (which does not contain payload data) followed by 312 data segments. Each data segment includes a data component and a forward error correction (FEC) component. A synchronizing (sync) component prefaces each data segment. A transport processor provides fixed length 188 byte packets to a transmission processor, which performs various coding functions on each packet to produce output symbol segments to be conveyed to an output transmission channel. Each byte comprises a predetermined number of symbols, eg., 4 symbols. The data packets contain data in conformance with the ISO-MPEG (International Standards Organization-Moving Pictures Experts Group) MPEG-2 data compression standard. The transport processor provides only the data packets to the transmission processor, which adds an overhead FEC error detection and correction component to each segment, and an overhead field sync segment at the beginning of each data field, ie., between each group of data field segments. The rate of data flow must be

regulated to perform these operations since, as will be seen, the overhead FEC components and the overhead field sync segment occur at different times and exhibit different durations.

The packets are separated by an interval which permits overhead required by each data segment (eg., FEC data) to be inserted into the datastream by the transmission processor. However, the packet datastream must be interrupted and delayed for a period of time equal to a segment interval when the longer duration field sync segment, which does not contain a data payload like the other packets, is to be inserted into the datastream. A datastream created by the need to interrupt and insert different duration overhead information (FEC and Field sync) at different times is illustrated by Figure 3. This datastream comprises 312 packet byte plus FEC intervals between Field sync intervals, as will be discussed.

Summary of the Invention

The inventors have recognized that an interrupted datastream as mentioned above not only undesireably reduces the data throughput rate, but also produces non-uniform intervals between data packets. The occurrence of such non-uniform inter-packet intervals significantly complicates the signal processing requirements.

In particular, the inventors have recognized that an interrupted data stream undesirably complicates the interfacing requirements between the transport processor and the transmission processor at the transmitter, particularly with respect to data synchronization, and between any system for recording the packetized datastream. It is very likely that an HDTV datastream will be subject to recording by either studio or consumer equipment. To satisfy MPEG timing requirements, any

recording system must faithfully reproduce the packet timing, including any non-uniform gaps between packets, which must be maintained between the packets as such gaps occurred. This requirement significantly increases the complexity of circuits needed to interface to a recording system. In addition, any such gaps produced by transmission processing must be maintained at a demodulator in a receiver.

The present invention is advantageously employed in the context of a system intended to process a packetized datastream representing a predetermined sequential data field structure. A system according to the invention eliminates the need to align the data field structure, which may be of the type exhibiting a non-uniform data rate due to different types of non-data overhead information of different duration such as that employed by the Grand Alliance HDTV system as described above.

At a transmitter, a transport processor (eg., for forming data packets with associated headers) is operated at an uninterrupted constant uniform data rate in a system which inserts non-data overhead information of different duration into the datastream to form the predetermined sequential data field structure. The transport processor is advantageously operated at such constant uniform data rate without having to modify a predetermined original data field structure. This process is facilitated by transferring data from the transport processor to an associated interface/buffer network in response to a predetermined clock.

In accordance with a feature of the invention at a transmitter, a video recording/playback device is situated in a constant data rate datastream path from the output of the transport processor.

5 A counterpart transport processor/decoder at a receiver similarly exhibits uninterrupted operation at a constant uniform data rate.

10 In a disclosed transmitter embodiment of the present invention, a transport processor operates at an uninterrupted constant uniform data rate in response to a 3/8 SC symbol clock for providing byte data to a buffer interface network at a uniform data rate. The buffer writes data in response to the 3/8 SC clock and reads out data at a non-uniform rate to a data field construction network. The field construction network operates at a non-uniform data rate for producing a sequence of output symbol
15 field structures in response to byte data and non-data overhead information. The data field construction network requests data at a non-uniform rate. The interface network converts this request to a uniform data rate request to the transport processor.

20 In a disclosed receiver embodiment of the present invention, a received symbol datastream exhibits a sequential data field structure. A data field processor processes the received symbol data field structure at a non-uniform data rate to produce output data at a non-uniform rate. A buffer interface network
25 responds to a 3/8 SC read clock for converting this data to an output MPEG byte datastream exhibiting a constant uniform data rate. This datastream is processed by a transport decoder which exhibits uninterrupted operation at a constant uniform data rate in response to the 3/8 SC SC clock.

30

Brief Description of the Drawings

In the drawing:

35 Figure 1 illustrates a sequential data field structure including synchronizing (sync) and data segments.

Figure 2 is a block diagram generally illustrating apparatus for processing a packetized datastream.

5

Figure 3 depicts a packetized datastream having non-uniform overhead intervals between data packets.

Figure 4 is a block diagram of a transmitter encoder including a buffer/interface network and data field structuring network according to the invention responsive to packetized input byte data for providing output symbols to a transmission channel.

10

Figure 5 illustrates a television channel spectrum that may be used to convey output data provided by the system of Figure 4, shown in relation to a conventional NTSC television channel spectrum.

15

Figures 6-16 depict waveforms associated with the operation of the transmitter system shown in Figure 4.

20

Figure 17 is a block diagram of a receiver decoder including a baseband data field processor and buffer/interface network according to the invention responsive to packetized input symbol data for providing output byte data to a transport processor.

25

Figures 18-27 depict waveforms associated with the operation of the receiver system shown in Figure 17.

Figures 28 and 29 respectively show additional details of the systems of Figures 4 and 17.

30

Figures 30-32 depict waveforms helpful in understanding the operation of the invention.

35

Figures 33 and 34 respectively illustrate apparatus as disclosed in Figures 4 and 17 in the context of a video recording/playback system..

Detailed Description of the Drawings

Figure 1 depicts a data field structure proposed for use by the Grand Alliance HDTV system in the United States, in a system for processing a packetized datastream. An output symbol datastream representing the data field structure is produced by a transmission processor in response to input data packets from a preceding transport processor. The transmission processor and the transport processor will be discussed in connection with Figure 4. Each data field structure includes an overhead field sync segment (which does not contain payload data) preceding a group of field data segments each having an associated sync component. Each field data segment includes an 187 byte data packet component, a one byte sync component prefacing each data segment, and a forward error correction (FEC) component following the data. Associated with each segment is an interval "Y" defining a data disable interval between each data packet. The transport processor provides 188 byte packets of input data plus segment sync to the transmission processor. The transmission processor adds FEC coding and field sync overhead information, and produces output segments in symbol form to be conveyed to an output transmission channel.

The sync component associated with each segment and the field sync component facilitate packet and symbol clock acquisition and phase lock at a receiver under extreme noise and interference conditions. The 4-symbol sync component is binary (2-level) in order to make packet and clock recovery rugged, and exhibits a pattern that repeats regularly at a unique rate to permit reliable detection at a receiver under noise and

interference conditions. The sync symbols are not Reed-Solomon or trellis coded, nor are they interleaved. The field sync component may contain pseudo-random sequences, and serves several purposes. It provides a means to determine the beginning of each data field, and may also be used by an equalizer in a receiver as a training reference signal to remove intersymbol and other forms of interference. It also provides a means by which a receiver may determine whether or not to use an interference rejection filter, and it may be used for diagnostic purposes such as measuring signal-to-noise characteristics and channel response. The field sync component furthermore may be used by phase tracking networks in the receiver to determine phase control loop parameters. Like the sync component, the field sync component is not error coded, trellis coded, or interleaved. In this example the data fields do not necessarily correspond to the interlaced picture fields which comprise a picture frame of an NTSC television signal.

Figure 2 illustrates, in general form, the processing of one type of data field segment 22 by transmission processor and output processor units in Figure 4. This segment is one of 312 data segments of a given data field totalling 832 symbols. The segment illustrated by Figure 2 includes a 187 byte MPEG-2 transport data packet prefaced by a one byte sync component and followed by an associated FEC component containing 20 Reed-Solomon parity bytes. Each transport packet as used in the Grand Alliance HDTV system includes a 4 byte link header, the first byte of which is a sync byte to facilitate packet synchronization. This may be followed by an optional adaptation header, with the remainder of the packet being MPEG data payload. The one byte sync component is mapped to 4 symbols before being 2-VSB modulated. The 187 byte MPEG packet segment and the FEC coding component are 2/3 trellis coded and mapped to 828 symbols before being 8-VSB modulated. Techniques for performing such 2-VSB and 8-VSB modulation are well known. A

resulting output field segment 24 conveyed to an output channel contains a 4 symbol sync component followed by an 828 symbol data field component containing MPEG data and FEC data.

Figure 3 represents a packetized datastream in conformance with the data field structure shown in Figure 1. Each data field has 312 segments each including sync, data and FEC components. More specifically, each data field segment includes an interval encompassing 188 data bytes including sync ("packet bytes") and an interval encompassing 20 FEC bytes. The 188 data bytes of each segment are accompanied by 188 clock intervals (cycles), and the 20 FEC bytes of each segment are accompanied by 20 clock intervals (cycles). When the time for inserting a field sync segment arrives, the transmission of data/FEC segments should be inhibited for a 228 clock cycle interval, which corresponds to a segment clock interval (ie., $20 + 188 + 20$ clock cycles). The field sync segment does not contain a data payload as is contained in each packet data segment. This disruption of the data flow undesirably produces uneven intervals, or gaps, between packets as shown in Figure 3. Such disrupted data flow and uneven inter-packet gaps greatly complicates the signal control and hardware requirements with respect to the interface between the transport and transmission processors at both the transmitter and receiver, and also reduces the data throughput rate. Moreover, it is difficult to synchronize to the data field structure when playing back pre-recorded material. The non-uniform gaps between packets greatly complicates the task of recording the packetized datastream on studio or consumer recording equipment, since the uneven inter-packet gaps must be maintained as they occurred, ie., the recording equipment must faithfully reproduce the MPEG packet timing. In addition, the uneven gaps must be maintained in an output signal produced by a demodulator at a receiver.

The described problems produced by the uneven inter-
packet gaps associated with irregular overhead data are
5 addressed and resolved by a system in accordance with the
present invention. In the disclosed system a transport processor
processes data packets at a constant uniform data rate in response
to a clock chosen as function of the data modulation scheme being
used. This clock also controls the operation of a buffer/interface
10 network located between the transport processor and a
transmission layer which processes the data in accordance with a
predetermined data field structure. An advantage of the disclosed
system is that it is not necessary to modify the original data field
structure to achieve the desired constant uniform data rate
15 operation. In addition, parameters such as symbol rate, segment
interleaving, Reed-Solomon error coding and synchronization
components are unaffected.

In the transmitter system of Figure 4 according to the
20 present invention, a transport processor 14 operates at an
uninterrupted constant uniform data rate for providing MPEG
Byte Data to a buffer interface network 16 at a uniform data rate.
Interface 16 provides output byte Data at a non-uniform rate to a
data field construction network and coder 17. Network 17
25 operates at a non-uniform data rate for producing a sequence of
output symbol field structures in response to the byte data and
non-data overhead information (FEC and field sync). Network 17
requests data at a non-uniform rate via a Data Field Packet
Request signal. Interface network 16 converts this request to a
30 uniform data rate request signal (Packet Request To Transport)
which is supplied to transport processor 14.

More specifically, transport processor 14 is included in a
system transport layer, and network 17 is included in a system
35 transmission layer (also including output processor 18) which is
separated from the transport layer by interface 16. Data source 12

includes MPEG compatible data compression networks and provides MPEG-2 byte data to transport processor 14. Transport processor 14 packs the MPEG bytes into fixed length data words that are eventually formed into fixed length (188 byte) data packets. Each packet is prefaced by a header containing information illustratively denoting program source, service type and other information describing and relating to the data in the associated packet payload data. Transport processor 14 also inserts a 1-byte MPEG packet sync at the beginning of each packet. Transmission processor 10 performs operations including input buffering, FEC error detection/correction coding, field sync insertion, trellis coding to improve carrier-to-noise ratio, interleaving to reduce the impact of data burst transmission errors, and symbol mapping.

Network 17 performs a data field construction function wherein input data packets are formed into a data field structure including data, FEC and field sync components as described previously. Data packets are provided from interface network 16 to network 17 with constant uniform inter-packet gaps such that the data fields are formed by network 17 seamlessly and without interrupting the datastream. The transmission system of Figure 4 operates in response to a symbol clock SC and clocks derived therefrom as will be discussed. A suitable symbol clock frequency is 10.762237 MHz.

The disclosed system according to the present invention achieves uniform data rate operation of the transport processor without modifying the original data field structure, eg., one field sync segment every 312 data segments, producing a uniform data flow using a 313 segment field. Moreover, it is not necessary to interrupt the datastream for inserting field sync overhead information between data fields.

The transmitter system of Figure 4 uses a $1/4$ SC clock and a $3/8$ SC clock where SC is the system symbol clock. The choice of a $1/4$ SC clock for signal processing as will be seen results from the fact that 1 byte (8 bits) comprises 4 symbols at 2 bits/symbol. A $3/8$ SC clock is preferred for 8-VSB systems, while a $3/4$ SC clock, also within the scope of the present invention, is preferred for faster data rate 16-VSB systems. In the system to be described, network 16 includes a FIFO buffer 46 between the output of transport processor 14 and the input of data field construction network 17. Byte data packets from transport processor 14 are read out from transport processor 14 and are written into buffer 46 in response to the $3/8$ SC clock, and data packets are read out of buffer 46 to coder 17 in response to the $1/4$ SC clock. Both of these clocks are generated by a digital machine rather than by a more expensive phase locked loop network. The $3/8$ SC signal clocks both transport processor 14 and buffer 46 so that data is transferred synchronously between the transport processor and the buffer. A similar requirement applies to the receiver as will be discussed.

Referring to Figures 6-9, symbol clock SC (Figure 6) and a derived, synchronous clock $1/4$ SC (Fig. 7) are generated by a timing control network 40, eg., a microprocessor, in network 17. Network 40 also generates a Data Field Packet Request signal (Figure 10) which is synchronized to symbol clock SC since the $1/4$ SC clock is used to generate the Data Field Packet Request. A timing signal generator 42 in network 16 generates the $3/8$ SC clock (Fig. 8) synchronous with the SC and $1/4$ SC clocks from timing network 40. Figure 9 (shown for reference only) depicts a one-byte wide pulse associated with the presence of the one byte sync pulse that appears as the first byte at the beginning of every data packet.

The 3/8 SC clock is generated by counting cycles of symbol clock SC. Unit 42 generates three output pulses for every eight pulses of symbol clock SC. Figures 7 and 8 illustrate one possible relationship between the 1/4 SC clock and the 3/8 SC clock. Any combination of 3 clock pulses within an 8 clock pulse interval may be used to develop the 3/8 SC clock, but the three pulses must have a fixed phase relationship to the 1/4 SC clock, and the same relationship must be maintained between the 3/8 SC clock and the 1/4 SC clock in the transmitter and receiver. The illustrated configuration of the 3/8 SC clock in Figure 8 is advantageous in that this signal is easy to develop and align with the sync byte (which is easily detected at the beginning of each packet), and is easy to replicate at a receiver. Analogous observations pertain to the use of any six of eight symbol clocks to generate a 3/4 SC clock, particularly for a 16-VSB signal. The illustrated relationship between the illustrated clocks is produced in timing control network 40 by resetting a counter at the rising edge of the 1/4 SC clock that causes the packet sync byte to be output from buffer 46. The symbol clock is counted from 0 to 7, with 0 being synchronous with the packet sync byte being output from buffer 46. Any three of eight counts of symbol clock SC may be used, but the same three must also be used at the receiver/decoder.

25

Timing control network 40 facilitates the generation of the data field structure containing 312 data segments and one field sync segment. The Data Field Packet Request signal (Figures 10, 13) from network 40 exhibits a high logic level for 188 bytes and a low logic level for 20 bytes in response to the 1/4 SC clock. The Data Field Packet Request signal from controller 40 (Figure 10) exhibits non-uniform inter-packet gaps. A portion of a data field is depicted, specifically the last two data segments 311 and 312 of one data field, a field sync segment 313 at the beginning of the next data field, and the first data segment of the next data field. This signal exhibits data "enable" intervals when data is

35

requested (each comprising 188 data bytes synchronized with 188
1/4 SC symbol clocks), and data "disable" intervals (each
5 comprising 20 1/4 SC symbol clock intervals) when FEC
information is to be added to the datastream, or 228 1/4 SC
symbol clock intervals when field sync information is to be added
between data fields. This signal is a free-running input to a
system control network 44 associated with network 16.

10

Control network 44 responds to the 3/8 SC and 1/4 SC clocks
for generating an output Packet Request to Transport signal as
shown in Figure 11. This signal requests a 188 byte data packet
from transport processor 14 every 313th clock cycle of the 3/8 SC
15 clock. This Packet Request signal contains constant uniform gaps
between packet requests for producing a uniform data rate and
uninterrupted data flow. The constant uniform gaps of 125 cycles
of the 3/8 SC clock between packet requests facilitates the
uninterrupted seamless insertion of overhead data such as FEC
20 information and the field sync between data fields into the data
stream by network 17 to create the data field structure, as will be
explained subsequently.

25

The disclosed system is concerned with processing a
datastream having a field structure with 313 segments per field,
consisting of a field sync segment followed by 312 data field
segments. In this context the disclosed system will work with
multiples of the 3/8 SC byte clock, eg., faster clocks including
3/4 SC, 3/2 SC and 3 SC in data modulation schemes including
30 8-VSB and 16-VSB for example. These options will be better
understood after the following discussion relating Figures 10 and
11 to Figures 30, 31 and 32. From this discussion it will also
become clear that the principles of the present invention are also
applicable to other types of data field structures.

35

The waveform of Figure 10 is a constant for the disclosed embodiment in the context of the described 313 segment data field structure. The structure of the Figure 11 waveform may vary as a function of factors as follows. Figure 30 corresponds to Figure 11, which depicts the uniform data rate Packet Request sent to transport processor 14 by network 44 in response to the 3/8 SC byte clock for an 8-VSB signal. If a twice as fast 3/4 SC clock is used for the same 8-VSB modulation, the Packet Request to transport processor 14 would be configured as shown in Figure 31. Since the size of each data packet is fixed at 188 bytes, the data packet interval remains unchanged at 188 cycles of the 3/4 SC clock. However, the inter-packet data disable interval has increased significantly, to 438 cycles of the 3/4 SC byte clock. In this example the number of cycles in each data segment has increased to 626 (twice as many as the previous example) due to the twice as fast 3/4 SC byte clock. In other words:

$$626 \text{ segment clocks} - 188 \text{ data clocks (fixed)} = 438 \text{ clocks}$$

Although the number of bytes/segment has increased, the structure of the data packet remains unchanged. The structure of the data field also remains unchanged since each data field still comprises 312 segments each containing a 188 byte data packet, prefaced by a field sync segment. Analogous observations pertain to other faster clock multiples such as 3/2 SC or 3 SC, where the number of byte clocks in the interval between data packets would increase proportionally. The 3/8 SC clock has been found to be the lowest rate clock for clocking 313 bytes/segment in a 313 segment data field.

30

Figure 32 illustrates the use of a faster 3/4 SC clock in a higher data rate 16-VSB modulation system. The result is the same as in Figure 30. In the 16-VSB case the symbol clock frequency (SC) doubles, and twice as many packets are throughput per unit of time compared to the 8-VSB system. The 188 byte-clock data interval and the 125 byte-clock inter-data

disable interval are the same as in the 8-VSB case because of the relationship between the clock speed and the data rate of its associated modulation type. The slower 3/8 SC clock is to lower data rate 8-VSB modulation as the faster 3/4 SC clock is to higher data rate 16-VSB modulation.

It can be shown that the desired symbol clock relationships (eg., 3/8 SC, 3/4 SC etc.) can be derived in accordance with the following expression which relates the symbols per field:

$$NX(188 + Y) = S(X + 1), \text{ where}$$

$X(188 + Y)$ and $S(X + 1)$ both represent symbols/field;

$(188 + Y)$ represents symbols/data segment;

$(X + 1)$ represents segments/field (eg., 313);

S represents symbols/segment (eg., 832);

X represents data segments/field (eg., 312);

Y represents the inter-data interval; and

N is a factor to be determined.

N has been found to be 8/3 in the case of a 3/8 SC clock in an 8-VSB system, and N has been found to be 4/3 in the case of a 3/4 SC clock.

Transport processor 14 is clocked by the 3/8 SC clock to read out data, and responds to the Packet Request signal from unit 44 by delivering the 188 bytes of an MPEG data packet during 188 cycles of the 3/8 SC clock, as represented by Fig. 12. Figure 12 actually depicts a Data Valid signal that is output by transport processor 14 simultaneously with the 188 byte data packets. The Data Valid signal exhibits the form of the Packet Request To Transport signal (Fig. 11). The Data Field Packet Request from timing circuit 40 in network 17 (Figure 10) is not synchronous with the Packet Request To Transport signal from network 44 (Fig. 11).

The data packets from transport processor 14 (Data) are applied to buffer 46 in network 16. This buffer is relatively small, several packets in depth. Buffer 46 also receives the Data Valid signal at a Write Enable (WEN) input to enable the data packets to be written to buffer 46 in response to the 3/8 SC Write clock (WCK). Buffer 46 also receives a Start Of Packet (SOP) flag from transport processor 14. This flag is generated at the beginning of each data packet concurrent with the sync byte which prefaces each data packet. Requests for transport processor 14 to send a packet of data to network 17 via interface network 16 are not honored until buffer 46 has reached a predetermined fullness level, eg., half full. The fullness level of buffer 46 is indicated by a Fullness flag, which is applied to a control input of controller 44.

A 188 byte data packet is clocked into buffer 46 every 188/313 cycles of the 3/8 SC clock (Figs. 11 and 12). During the remaining 125 cycles of the 3/8 SC clock, no data is clocked into FIFO 46. The input data rate to buffer 46 is uniform and exactly matches the output data rate from buffer 46. The output data rate is controlled by the Data Frame Packet Request signal from circuit 40. The Data Frame Packet Request signal and the Packet Request to Transport signal are not synchronous but are related through the 3/8 SC and 1/4 SC clock relationships.

Controller 44 contains logic networks responsive to the 3/8 SC clock, to the Data Field Packet Request signal, to the buffer Fullness flag (Fig. 15) from buffer 46, and to the Start of Packet (SOP) flag received from an alignment network 45 via buffer 46. Controller 44 provides a control signal (Figure 14) to the Read Enable (REN) input of buffer 46 to enable buffered transport packet data to be read out to network 17 at the appropriate time. This occurs as follows with reference to Figs. 13-16. The Fig. 13 signal is similar to the previously discussed Figure 10 signal.

Normally, the Read Enable signal (Fig. 14) is synchronous with the Field Data Packet Request signal (Fig. 13). The SOP flag that normally appears at the beginning of each data packet causes controller 44 to provide an output to the REN input of buffer 46 to stop buffer 46 from reading out data. Specifically, controller 44 is programmed to respond to the SOP flag by reading out buffer 46 for 188 bytes, then stopping buffer read out for the 20 byte FEC interval. This allows FEC network 50 in transmission coder 17 to calculate error coding information for the packet that immediately precedes the current packet being held in buffer 46. This error coding information is inserted into the datastream during the 20 byte FEC overhead interval at the end of the preceding packet. Both the Data Field Packet Request (Figure 13) and the buffer Read Enable signal when present (Figure 14) exhibit a non-uniform inter-packet gap structure required for inserting the 20 byte FEC overhead information by unit 50 of network 17, and for inserting the longer duration field sync overhead information by unit 58. This insertion of overhead information is accomplished without interrupting the datastream.

Referring to Figure 4, inserting the field sync segment without stopping or disrupting the datastream is facilitated by the manner of read/write clocking of buffer 46 in combination with the predetermined buffer fullness level. Packets are continuously written into buffer 46 from the transport processor as packets are requested. Over one data field period, the exact number of data bytes needed to constitute a data field will have been transferred from transport processor 14 to buffer 46. Buffer 46 is relatively small, in this example large enough to accomodate 4 data packets. The predetermined buffer fullness level is 2 data packets, but this level may vary with the requirements of a particular system. In practice, this level should be determined so that, for the known data internals and data disable intervals in a given system, the buffer will not overflow when buffer read out is stopped to insert

overhead information into the datastream, and will not empty at other times. When buffer read out is momentarily stopped to insert overhead information (eg., field sync) into the datastream, data packets continue to be written to buffer 46 at a constant uniform rate (Figure 11). During this time buffer 46 does not fill up completely. The constant uniform gap between data packets (Figure 11) allows enough time for buffer 46 to refill while read out is momentarily disabled for overhead insertion. After the overhead has been inserted during the read disable interval, data is again read out from buffer 46. During all of this time transport processor 14 has been continuously sending data packets to buffer 46, whereby the datastream flows without interruption while transport 14 processes data packets without interruption.

When a faster byte clock is used, eg., $3/4$ SC or $3/2$ SC, buffer 46 will not run empty because the inter-packet intervals in 8-VSB mode are longer. This allows additional time for the buffer to refill from the transport processor.

The buffer 46 Read Enable is also disabled by controller 44 if the buffer Fullness flag exhibits a low logic level, indicating that buffer 46 contains less than a predetermined number of data packets. At this time the Data Valid signal from network 44 (Fig. 16) is "low" (absent) since the reading out of buffer 46 has been disabled. This condition may occur, for example, when system operation is initiated or after a system reset, eg., at a time T1. Typically the data field structure is initiated at the beginning of the transmission day, and the transmission of data packets continues uninterrupted from then until station sign-off at the end of the transmission day. During this time, while reading out of buffer 46 is disabled, transport processor 14 continues to send data packets to buffer 46 in response to the Packet Request To Transport signal from controller 44. After a predetermined number of packets has been stored and the buffer fullness condition has

been satisfied, the Fullness flag (Fig. 15) changes state and exhibits a high logic level. Buffer 46 again receives a Read Enable
5 signal for outputting data packets. The buffer Read Enable operation is initiated at the leading edge of the first data enable interval that appears after the Fullness flag goes high in response to the fullness condition being satisfied. Consequently, at a time
10 T2, the first (sync) byte of a data packet is aligned with the beginning of a packet request from the Data Field Packet Request signal (Fig. 13) and with the beginning of the Data Valid signal (Fig. 16).

Alignment circuit 45 in Figure 4 facilitates the above-
15 described operation illustrated by Figures 13-16. Circuit 45 is shown in Figure 28 together with networks 17, 42, 44 and 46 of Figure 4. Alignment circuit 45 comprises cascaded "D" type flip-flops (registers) 102 and 104 which are clocked by the 1/4 SC Read Clock of buffer 46, and which are enabled by the Read
20 Enable input (REN) provided to buffer 46 from system controller 44. Data from buffer 46 is conveyed via flip-flops 102 and 104 to transmission coder 17. Controller 44 produces a buffer Read Enable signal in response to a Start Of Packet (SOP) flag (a register delayed version of the input Packet Start signal) from an output of
25 flip-flop 102. The Packet Start signal is a buffer delayed version of the SOP signal input to buffer 46.

Continuing with Figure 4, output 8 byte parallel Data packets from network 45 and the Data Valid signal (Figure 16) are applied
30 to respective inputs of FEC unit 50 in transmission coder 17. FEC unit 50 adds 20 bytes of FEC data to the datastream during the data "invalid" overhead intervals between each data packet interval in accordance with the waveform of Figure 16. The datastream from FEC unit 50 is applied to a parallel-to-serial data
35 converter 52. Unit 52 converts each parallel 8 bit byte into a group of four 2 bit words which are output serially. Using well-

21

known techniques, the data from unit 52 are 2/3 trellis coded by unit 54 for producing three output bits (two information bits and one derived redundancy bit) for every two input bits to improve signal-to-noise performance. These bits are provided according to a predetermined algorithm, examples of which are known in the art. Coder 54 operates in conjunction with bit generator unit 56, which provides the third bit in accordance with the predetermined algorithm.

The output of trellis coder 54 comprises a sequence of 3 bit trellis coded words, with four 3 bit words constituting a byte. Symbol mapper 58 maps each 3 bit input word from coder 54 to one output symbol, and time multiplexes these output symbols with a field sync component of predetermined value from unit 60 to produce an output symbol datastream. In the mapping function of unit 58, eight progressively increasing numerical binary output values from unit 54, from 000, 001, 010,.... to 111, are translated into the following eight symbol levels, respectively

-7 -5 -3 -1 +1 +3 +5 +7.

Control signals for field sync generator 60 and mapper 58 are provided by timing control network 40, eg., a microprocessor. Network 40 controls the operation of field sync generator 60 so that unit 60 is enabled to output field sync segment information during an interval of predetermined duration produced between adjacent data fields, ie., after every 312 data segments as discussed. Each field sync segment is predictably multiplexed into the data stream between groups of field data without interrupting the data flow, as previously discussed regarding the operation of buffer 46. Multiplexer 58 also replaces the MPEG sync component at the beginning of each packet with a segment sync before output processing by unit 18.

An 8-level symbol data signal from unit 58 is provided to output processor 18, where a small pilot signal may be added to a

suppressed RF carrier to allow robust carrier recovery at a receiver under difficult reception conditions. Using known signal processing techniques, an 8-VSB modulator in processor 18 receives the trellis coded composite data signal, filters and spectrum shapes the signal for transmission over a standard 6 MHz television channel, modulates (upconverts) the data signal onto an intermediate frequency (IF) carrier, and translates the resulting signal to an RF carrier. Figure 5 depicts, in the upper diagram, the spectrum of the baseband VSB modulation signal for this example, relative to a standard 6 MHz NTSC channel spectrum as shown in the lower diagram.

Figure 17 depicts a VSB receiver incorporating the principles of the present invention. A baseband demodulated Symbol Data datastream from a preprocessor 72 exhibits a sequential data field structure as described previously, with a non-uniform data rate. A data field processor 75 associated with a system transmission layer processes the symbol data field structure with a non-uniform data rate to produce output Data at a non-uniform rate. A buffer interface network 84 converts this data to an MPEG Byte datastream exhibiting a constant uniform data rate. This datastream is processed by a transport decoder 86 which exhibits uninterrupted operation at a constant uniform data rate for providing decoded byte data to an output processor 88. Transport decoder 86 is associated with a system transport layer.

More specifically, a signal received from a transmission channel is processed by an RF tuner 70 including channel selection and mixer circuits to produce a frequency downconverted signal. This signal is subjected to IF filtering and synchronous detection by pre-processor unit 72 using known signal processing techniques to produce a baseband signal. Unit 72 also includes an equalizer to compensate for transmission channel amplitude and phase perturbations. A Symbol Data output signal from unit 72 is

afterwards subjected to trellis decoding, forward error
detection/correction and other signal processing in a manner
5 which is the inverse of the processing performed by the
transmitter system of Figure 4.

Symbol clock SC and derived clocks $1/4$ SC and $3/8$ SC are
identical to corresponding clocks at the transmitter. Thus an
10 output datastream (MPEG Byte Data) provided to a transport
processor/decoder 86 corresponds to the datastream (MPEG Byte
Data) provided from transport processor 14 in the Figure 4
transmitter system. The input Symbol Data applied to symbol
mapper and de-mux unit 74 corresponds to the Output Symbol
15 Data from network 17 in Figure 4. The input Symbol Data
datastream contains a relatively long duration field sync
component between groups of shorter duration data packets that
respectively define adjacent data fields (Figures 1 and 3). Thus
the receiver input symbol datastream exhibits a non-uniform data
20 rate. Before being applied to receiver transport processor 86, this
non-uniform rate input symbol datastream is converted to an
MPEG Byte Data output signal (from network 84) which contains
data packets occurring at a constant uniform data rate separated
by uniform inter-packet gaps. Such a constant uniform rate
25 datastream advantageously facilitates data processing and data
de-multiplexing by transport decoder 86, which operates without
interrupting the datastream.

More specifically, a non-uniform rate baseband input
30 symbol datastream produced after demodulation and equalization
is applied to symbol mapper and de-multiplexer 74, which
performs the inverse of the operations performed by mapper 58
in Figure 4. Unit 74 maps each symbol to a 3 bit word which is
trellis decoded to a 2 bit word by trellis decoder 76 in conjunction
35 with unit 78. Unit 74 also replaces the segment sync at the
beginning of each segment packet with an MPEG packet sync. A

symbol datastream processed by unit 74 is monitored by unit 90 to detect the appearance of Control information present during field sync intervals, eg., so-called "training" signal information for use by a preceding equalizer in unit 72, mode selection information, and other information. This information is extracted by unit 90 and conveyed to preceding circuits in accordance with the requirements of a particular system.

10

Output groups of four 2 bit data words from trellis decoder 76 are converted from serial form to 8 bit (1 Byte) parallel form by serial-to-parallel converter 80. Serial words from converter 80 are applied to error detection and correction unit 82, eg., a Reed-Solomon decoder. An error corrected Data signal from unit 82 is applied to receiver buffer/interface network 84 together with a Data Valid signal, clocks SC and 1/4 SC, and a Packet Start signal from controller 92. The SC symbol clock and the 1/4 SC clock are synchronous and are produced by a local oscillator in controller 92. The Packet Start Signal is generated in response to the appearance of the sync byte at the beginning of each packet. FEC unit 82 generates the Data Valid signal in response to the Packet Start signal.

15

20

25

Buffer/interface network 84 is similar to transmitter network 16 and is shown in Figure 29. The interface network of Figure 29 includes a FIFO buffer 100, a system controller 120, a 3/8 SC clock generator 122 and an alignment circuit 145, all of which elements exhibit characteristics similar to those of counterpart elements for transmitter network 16 shown in Figure 28. Buffer 100 of Figure 29 is essentially the same as FIFO buffer 46 in transmitter buffer network 16 in Figure 4, except that the Read and Write clocks are interchanged. Specifically, the Write clock input WCK of buffer 100 responds to the 1/4 SC clock, and the Read clock input RCK of buffer 100 responds to the 3/8 SC clock. In Figure 29 the SOP input signal to register 110 is a

30

35

buffered version of the Packet Start signal, and the SOP input to transport processor 86 is a delayed version of the SOP input to register 110.

Continuing with Figure 17, a packetized baseband MPEG byte datastream from network 84 is processed by a transport processor/decoder 86, which basically performs the inverse of the operations performed by transport processor 14 at the transmitter (Figure 4). Transport processor 86 decodes data into its constituent components. Processor 86 includes various data processing and demultiplexing circuits including header analysers, signal routers responsive to header information, MPEG decompression networks and other image and audio data processors which provide signals that are formatted as required by video/audio processor 88 in Figure 17. Video and audio data recovered by transport decoder 86 are respectively processed by video and audio networks in a unit 88 to provide image and sound information suitable for reproduction.

Detector 90 in network 75 also provides a Field Marker signal to control unit 92. The Field Marker instructs controller 92 not to write the field sync segment to buffer network 84, whereby a resulting output datastream is devoid of the field sync component. Output data packets from buffer network 84 form a single datastream that is devoid of the field sync component, whereby the MPEG Byte Data datastream from network 84 exhibits a constant, uniform data rate and constant, uniform inter-packet gaps.

Removing the overhead field sync segment without stopping or disrupting the datastream is facilitated by the manner of read/write clocking of buffer 84 in combination with the predetermined buffer fullness level. Packets are continuously read out of buffer 46 to the transport processor as packets are

available. Over one data field period, the exact number of data bytes needed to constitute a data field will have been transferred to transport processor 86 from buffer 84. Buffer 84 exhibits the same size and fullness requirement as buffer 46 at the transmitter. When writing to buffer 84 is momentarily disabled to remove overhead information (eg., field sync) from the datastream, data packets continue to be read out to transport processor 86 at a constant uniform rate. During this time buffer 84 does not empty completely. The constant uniform gap between data packets allows enough time for buffer 84 to empty partially while writing in is momentarily disabled to remove the overhead information from the datastream. After overhead information has been removed during the write disable interval, data is again written to buffer 84. During all of this time transport processor 86 has been continuously receiving data packets from buffer 84, whereby the datastream flows without interruption while transport 86 processes data packets without interruption.

The waveforms shown in Figures 18-27 pertain to receiver operation. Clock synchronization at the receiver is achieved by using the packet sync byte, which as explained previously is the first byte of every data packet. As in the case of the transmitter, after the sync byte at the beginning of a packet is sensed (Figure 21) a symbol clock SC (Figure 18) and a mutually synchronized $1/4$ SC clock (Figure 19) are generated. Also as in the transmitter, a counter is used to count cycles of the $1/4$ SC clock for producing the receiver $3/8$ SC clock (Figure 20). This counter is reset to zero synchronously with each packet sync byte. The observations made previously with respect to the structure and characteristics of the $3/8$ SC symbol clock at the transmitter also apply to the $3/8$ SC clock at the receiver. The $1/4$ SC clock and the $3/8$ SC clock should be identical at the transmitter and receiver.

Figure 22 illustrates the output Data Valid timing signal produced by unit 82 of network 75 concurrent with the Data signal from processor 75. The shape of the Data Valid signal corresponds to the shape of the Data signal from processor 75. This Data Valid timing signal exhibits a non-uniform characteristic with non-uniform inter-packet gaps, including a 20-(clock) count gap corresponding to inserted FEC data in the Data signal, and a significantly wider, 228-count gap corresponding to the inserted field sync in the Data signal. Data packets in the Data signal appear during the positive-going 188 count intervals of the Data Valid signal. Thus the Data signal from network 82 exhibits a non-uniform data flow with respect to the packet data. The counterpart of the Figure 22 Data Valid signal at the transmitter is shown in Figures 3 and 10.

In contrast, the Data Valid signal provided from buffer network 84 to transport processor/decoder 86 (Figure 23) exhibits a uniform structure with uniform inter-packet gaps. This signal signifies that the MPEG Byte Data datastream from buffer network 84 is constituted by constant uniform inter-packet gaps ("data disable" intervals of 125 counts of the $3/8$ SC clock) between constant uniform data packets ("data enable" intervals of 188 counts of the $3/8$ SC clock). Thus the MPEG Byte Data datastream exhibits a constant uniform data flow to facilitate the uninterrupted operation of transport processor 86. In response to the Data Valid signal of Figure 23, transport processor 86 acquires data packets for processing during each 188-count clock interval based on an uninterrupted flow of data. Transmitter counterparts of the Figure 23 Data Valid signal are shown in Figures 11 and 12.

Receiver buffer/interface network 84 operates in a manner similar to that of the counterpart transmitter network shown in Figure 28. As noted previously, the respective FIFO buffers differ with respect to the Read and Write clock inputs. Also, whereas

transmitter system controller 44 in Figure 28 provides a Packet Request To Transport signal in response to a Data Field Packet Request, the counterpart receiver network in Figure 29 sends an SOP flag to receiver transport processor 86 to indicate the beginning of a new packet. As in the case of counterpart buffer 46 at the transmitter, receiver buffer 100 in Figure 29 is cleared and refilled to a predetermined level each time the receiver system is reset. Buffer 100 must reach a predetermined "fullness" level before data is permitted to be read out. This operation is illustrated by Figures 24-27 and is analogous to the related transmitter operation previously discussed with respect to Figures 13-16.

Controller 120 generates a free-running internal timing waveform shown in phantom form in Figure 24. This signal exhibits a constant uniform structure. Specifically, this signal is constituted by constant uniform intervals of 125 counts of the 3/8 SC clock (corresponding to inter-packet data disable intervals) between constant uniform intervals of 188 counts of the 3/8 SC clock (corresponding to data packet data enable intervals). From this signal controller 120 produces a FIFO Read Enable signal (Figure 25) for buffer 100 and a Data Valid signal (Figure 27) for transport processor 86, both with a constant uniform structure. These signals are produced in response to the buffer Fullness signal (Figure 26) and the SOP flag input to register 110. This flag is a buffered and delayed version of the Packet Start signal. The (register delayed) SOP output of register 110 is applied to a control input of unit 120 and to transport processor 86. The buffer Fullness signal is produced when buffer 100 exhibits a predetermined fullness. The buffer Read Enable operation is initiated at the leading edge of the first (positive going) data Enable interval that appears after the Fullness signal goes high in response to the buffer fullness condition being satisfied. Consequently, at a time T2, the first (sync) byte of a data packet is

aligned with the beginning of a valid data interval of the Data Valid signal (Figure 27).

5

Both flip-flops and the Read clock (RCK) input of buffer 84 are clocked by the 3/8 SC clock locally generated by unit 122 in response to the SC and 1/4 SC clocks as discussed previously. The 3/8 SC clock is also applied to controller 120. MPEG Byte Data are conveyed via flip-flops 110 and 112 to a data input of transport processor 86 when these flip-flops are enabled by the Read Enable signal produced by controller 120. At the same time, the SOP flag is conveyed to transport processor 86 together with the Data Valid signal (Figure 27) from controller 120. The Data Valid signal is provided to transport processor 86 to enable it to acquire data during intervals when valid packet data are present.

The interface between the transport processor and the transmission processor including network 17 is important in many applications. In television broadcast for example, the transmission processor will be required to generate and output data fields without interruption once transmission has begun. Television receivers rely on this uninterrupted stream of data fields including field sync segments to maintain synchronization. Any change in the data field rate or structure during broadcast would result in a loss of synchronization at the receiver. A broadcast studio normally has multiple banks of video tape players pre-programmed to automatically switch to appropriate source material in a timed manner. These tape players output transport packets containing transport stream information. Each tape player synchronizes its output to the flow of data to the transmission processor, which is not permitted to alter its field rate or field structure. Non-uniform gaps in the flow of packets from the transport processor to the transmission processor have the effect of making the transmission data field structure an artifact in the data flow at the interface, which would have both a packet and a

data field structure. Each studio recorder would be undesireably required to have complicated interfaces that synchronize the tape
5 output to both the packet and field boundaries. Additional information about the field structure would be required to be passed across the interface, or developed by monitoring the data flow at the interface. The tape interface would contain provision for packet sync detection, field detection and sufficient memory to
10 buffer the data field structure. Additional complications are produced by pre-recorded tapes, and insertion of local programming and commercials. These complications and other difficulties are successfully resolved by a recording/playback system employing the principles of the present invention, as
15 shown in Figures 33 and 34.

Figures 33 and 34 respectively represent the transmitter and receiver systems shown in Figures 4 and 17, except that the systems of Figures 33 and 34 include a video recorder device. In
20 Figure 33 a video tape recorder/playback device 15 receives a uniform data rate datastream from transport processor 14, a provides playback data at a uniform rate to coder and data field construction network 17 via buffer/interface 16. As in the case of the Figure 4 system, the Figure 33 system exhibits a uniform data
25 flow at the interface between the transport layer and the transmission layer. In this example data source 12 includes a broadcast studio video camera and an MPEG coder for encoding camera output signals prior to packetizing by transport processor 14.

30

Video recorder 15 may be a commercial device such as a Panasonic™ D3 video tape recorder for providing byte-by-byte recording to tape. In some video recorder designs interface 16 may be included in the recorder device itself. Recorder 15 may
35 comprise one of a bank of several video recorders commonly

employed at broadcast studios as known to facilitate the transmission of various type of program material from the studio.

5

In Figure 34 a video tape recorder/playback device 85 receives and processes a uniform data rate datastream (with overhead information removed) from interface/buffer 84, and provides playback data at a uniform rate to transport processor/decoder 86. The system of Figure 34 also exhibits a uniform data flow at the interface between the transmission layer and the transport layer. In this system recorder 85 represents a consumer device (VCR) capable of recording off-the-air, or for playing back material such as may have been pre-recorded by a device having the characteristics of unit 15 in Figure 33. Unit 85 may be a separate unit in a system where elements 72, 75, 84 and 86 are incorporated in a television receiver. Alternatively, elements 72, 75, 84 and 86 may all be included in recorder 85.

10

15

CLAIMS

- 5 1. A system for processing a packetized digital
datastream containing video information to produce an output
datastream representing a sequence of data fields each comprising
313 segments constituted by (a) 312 data segments each including
a data interval and a segment overhead interval, and (b) a field
10 overhead segment with a different overhead interval prefacing
said data segments, said system being responsive to a system
clock (SC) and comprising:
a transport processor (14) responsive to input data for
forming data packets of predetermined length;
15 an interface network (16) for receiving output data from
said transport processor;
a data field construction network (17) operative at a
non-uniform data rate and responsive to data from said interface
network for generating said output datastream representing said
20 sequence of data fields, said output datastream exhibiting data
intervals and overhead intervals of different duration; and
an output processor (18); wherein
said transport processor provides output data packets to
said interface network at a constant uniform data rate; and
25 said data field construction network operates at said
non-uniform data rate without interrupting said datastream.
- 30 2. A system according to claim 1 wherein
said interface network includes a buffer (46) for
transferring data from said transport processor to said data field
construction network;
said transport processor transfers data to said buffer at a
constant uniform data rate; and
35 said buffer transfers data to said data field construction
network at a non-uniform data rate.



3. A system according to claim 1, wherein
said data field construction network requests data from
5 said interface network at a non-uniform data rate (Data Field
Packet Request); and
said interface network requests data from said transport
processor at a constant uniform data rate (Packet Request To
Transport).

10

4. A system according to claim 2, wherein
said data field construction network responds to said
system clock;
15 said transport processor operates in response to a clock
which is an integer multiple of $3/8$ SC where SC is said system
clock; and
said buffer writes in data in response to said even
multiple of said $3/8$ SC clock.

20

5. A system according to claim 2 wherein
said buffer size is significantly less than a field of data;
and
25 said integer is an even integer.

6. A system according to claim 1, wherein
said input data is MPEG compatible data;
30 said segment overhead interval encompasses FEC error
correction information;
said field overhead segment contains field sync
information; and
said data interval contains 188 data bytes.

35



7. A system according to claim 1, wherein
output data from said transport processor is in the form
5 of Byte data; and
said system clock SC is a symbol clock.

8. A system according to claim 1 and further including:
10 video recorder/playback apparatus (Fig. 33; 15) located
in a constant uniform data rate datastream path between said
transport processor and said interface network.

9. A system for processing a digital datastream
15 containing video information to produce an output datastream
representing a sequence of data fields each comprising plural data
segments each including data and overhead intervals, and a field
overhead segment with a different overhead interval prefacing
20 plural data segments, comprising:

a transport processor (14) responsive to input data for
forming data packets of predetermined length;
an interface network (16) for receiving output data from
said transport processor;

25 a data field construction network (17) operative at a
non-uniform data rate and responsive to data from said interface
network for generating said output datastream representing said
sequence of data fields, said output datastream exhibiting data
intervals and overhead intervals of different duration; and

30 an output processor (18); wherein

said transport processor transfers output data packets to
said interface network at a constant uniform data rate in response
to a clock which is an integer multiple of $3/8$ SC where SC is a
system clock.



10. A system according to claim 9, wherein
said segment data intervals each include constituent data
5 elements D in number;
said output processor includes an 8-VSB modulator;
said data is transferred in response to a $3/8$ SC clock;
and
data and inter-data intervals of transferred data from
10 said transport processor respectively correspond to intervals of
said $3/8$ SC clock, D and E in number, where D is greater than E.
11. A system according to claim 10 wherein
15 D is 188 and E is 125.
12. A system according to claim 9, wherein
said segment data intervals each include constituent data
20 elements D in number;
said output processor includes an 8-VSB modulator;
said data is transferred in response to a $3/4$ SC clock;
and
data and inter-data intervals of transferred data from
25 said transport processor respectively correspond to D and E
intervals of said $3/4$ SC clock, D and E in number, where D is less
than E.
13. A system according to claim 12, wherein
30 D is 188 and E is 438.



36

14. A system according to claim 9, wherein
said segment data intervals each include constituent data
5 elements D in number;
said output processor includes a 16-VSB modulator;
said data is transferred in response to a 3/4 SC clock;

and

10 data and inter-data intervals of transferred data from
said transport processor respectively correspond to intervals of
said 3/4 SC clock, D and E in number, where D is greater than E.

15 15. A system according to claim 14, wherein
D is 188 and E is 125.

16. A system according to claim 9 and further including:
video recorder/playback apparatus (Fig. 33; 15) located
20 in a constant uniform data rate datastream path between said
transport processor and said interface network.

17. A receiver system for processing a modulated
25 packetized digital datastream containing video information
representative of a sequence of data fields each comprising 313
segments constituted by (a) 312 data segments each including a
data interval and a segment overhead interval, and (b) a field
overhead segment with a different overhead interval prefacing
30 said data segments, said system being responsive to a system
clock (SC) and comprising:

an input processor (72) for providing a demodulated
datastream exhibiting said sequence of data fields and exhibiting
a non-uniform data rate;

35



a data field processor (75) for removing overhead information from said demodulated datastream to produce a datastream exhibiting said non-uniform data rate;
an interface network (84) for receiving output data from said data field processor; and
a transport decoder (86) for decoding data packets received from said interface network to produce output data;
wherein
said transport decoder receives data packets from said interface network at a constant uniform data rate; and
said data field processor operates at said non-uniform data rate without interrupting said datastream.

15

18. A system according to claim 17, wherein
said interface network includes a buffer for transferring data from said data field processor to said transport decoder;
said data field processor transfers data to said buffer at a non-uniform data rate; and
said buffer transfers data to said transport decoder at a constant uniform data rate.

25

19. A system according to claim 18, wherein
said data field processor responds to said system clock;
said transport decoder operates in response to a clock which is an integer multiple of $3/8$ SC where SC is said system clock; and
said buffer reads out data in response to said multiple of said $3/8$ SC clock.

30



20. A system according to claim 18, wherein
said buffer size is significantly less than a field of data;
5 and
said integer is an even integer.

21. A system according to claim 17, wherein
10 said output data is MPEG compatible data;
said segment overhead interval encompasses FEC error
correction information; and
said field overhead interval contains field sync
information.

15

22. A system according to claim 17, wherein
said output data from said transport decoder is in the
form of Byte data; and
20 said system clock SC is a symbol clock.

23. A system according to claim 17 and further
including
25 video recorder/playback apparatus (85) located in a
constant uniform data rate datastream path between said
interface network and said transport decoder.

30 24. In a receiver for processing a modulated packetized
digital datastream containing video information representing a
sequence of data fields each comprising 313 segments constituted
by (a) 312 data segments each including a data interval and a
segment overhead interval, and (b) a field overhead segment with
35 a different overhead interval prefacing said data segments, a data
processing method comprising the steps of



(a) demodulating (72) said datastream to produce a demodulated datastream with a non-uniform data rate;

5 (b) removing (75) overhead information from said demodulated datastream without interrupting said datastream, to produce a datastream with a non-uniform data rate;

(c) decoding (86) data from said datastream produced in step (b) at a constant uniform data rate; and

10 (d) conveying (84) data from processing step (b) to processing step (c) at a constant uniform data rate.

25. A receiver system for processing a modulated digital
15 datastream containing video information representative of a sequence of data fields each comprising plural data segments each including data and overhead intervals, and a field overhead segment with a different overhead interval prefacing plural data segments, comprising:

20 an input processor (72) for providing a demodulated datastream exhibiting said sequence of data fields and exhibiting a non-uniform data rate;

a data field processor (75) for removing overhead information from said demodulated datastream to produce a
25 datastream exhibiting said non-uniform data rate;

an interface network (84) for receiving output data from said data field processor; and

a transport decoder (86) for decoding data packets received from said interface network to produce output data;

30 wherein

said transport decoder receives data packets from said interface network at a constant uniform data rate in response to a clock which is an integer multiple of $3/8$ SC where SC is a system clock.

35



40

26. A system according to claim 25, wherein
said segment data intervals each include constituent data
5 elements D in number;
said input processor includes an 8-VSB demodulator;
said transport decoder receives data packets from said
interface network in response to a $3/8$ SC clock; and
data and non-data intervals of a datastream received by
10 said transport decoder from said interface network respectively
correspond to intervals of said $3/8$ SC clock, D and E in number,
where D is greater than E.

15 27. A system according to claim 26, wherein
D is 188 and E is 125.

20 28. A system according to claim 25, wherein
said segment data intervals each include constituent data
elements D in number;
said input processor includes an 8-VSB demodulator;
said transport decoder receives data packets from said
interface network in response to a $3/4$ SC clock; and
25 data and non-data intervals of a datastream received by
said transport decoder from said interface network respectively
correspond to intervals of said $3/4$ SC clock, D and E in number,
where D is less than E.

30 29. A system according to claim 28, wherein
D is 188 and E is 438.



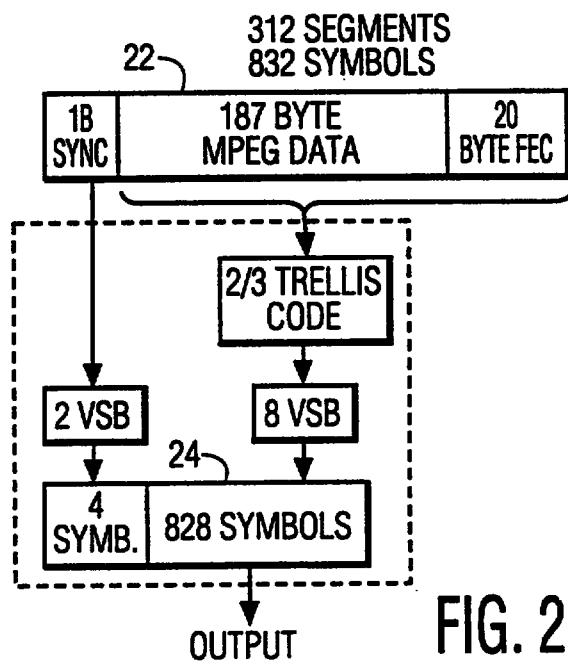
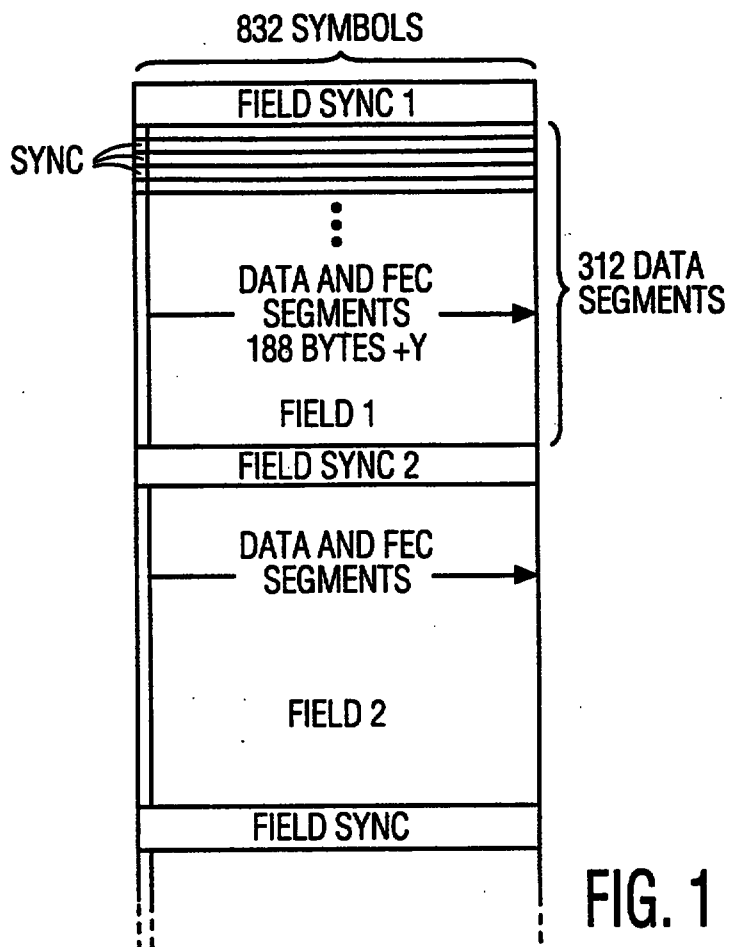
30. A system according to claim 25, wherein
said segment data intervals each include constituent data
5 elements D in number;
said input processor includes a 16-VSB demodulator;
said transport decoder receives data packets from said
interface network in response to a 3/4 SC clock; and
data and non-data intervals of a datastream received by
10 said transport decoder from said interface network respectively
correspond to intervals of said 3/4 SC clock, D and E in number,
where D is greater than E.
- 15 31. A system according to claim 30, wherein
D is 188 and E is 125.
- 20 32. A system according to claim 25 and further
including
video recorder/playback apparatus (85) located in a
constant uniform data rate datastream path between said
interface network and said transport decoder.
- 25 33. In a receiver for processing a modulated digital
datastream containing video information representing a sequence
of data fields each comprising plural data segments each including
data and overhead intervals, and a field overhead segment with a
30 different overhead interval prefacing plural data segments, a data
processing method comprising the steps of
(a) demodulating (72) said datastream to produce a
demodulated datastream with a non-uniform data rate;
(b) removing (75) overhead information from said
35 demodulated datastream without interrupting said datastream, to
produce a datastream with a non-uniform data rate;



(c) decoding (86) data from said datastream produced in step (b); and

- 5 (d) conveying (84) data from processing step (b) to processing step (c) at a constant uniform data rate in response to a clock which is an integer multiple of $3/8$ SC where SC is a system clock.

1/13



2/13

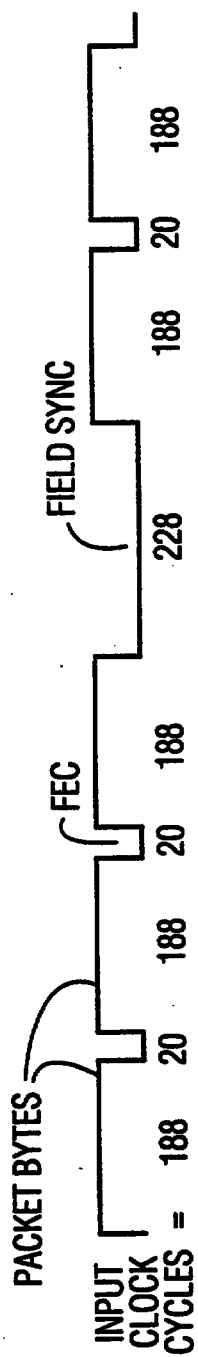


FIG. 3

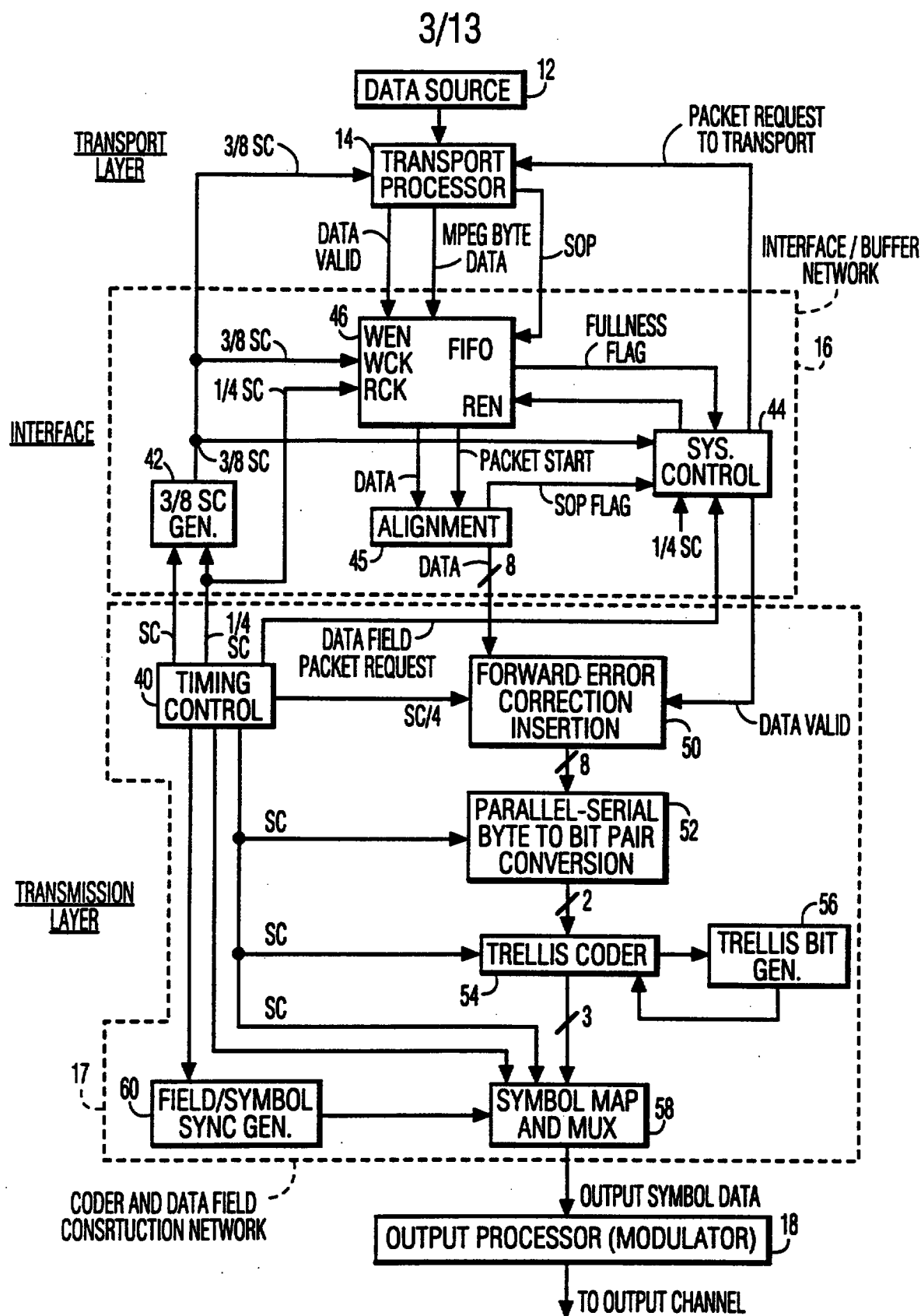


FIG. 4

4/13

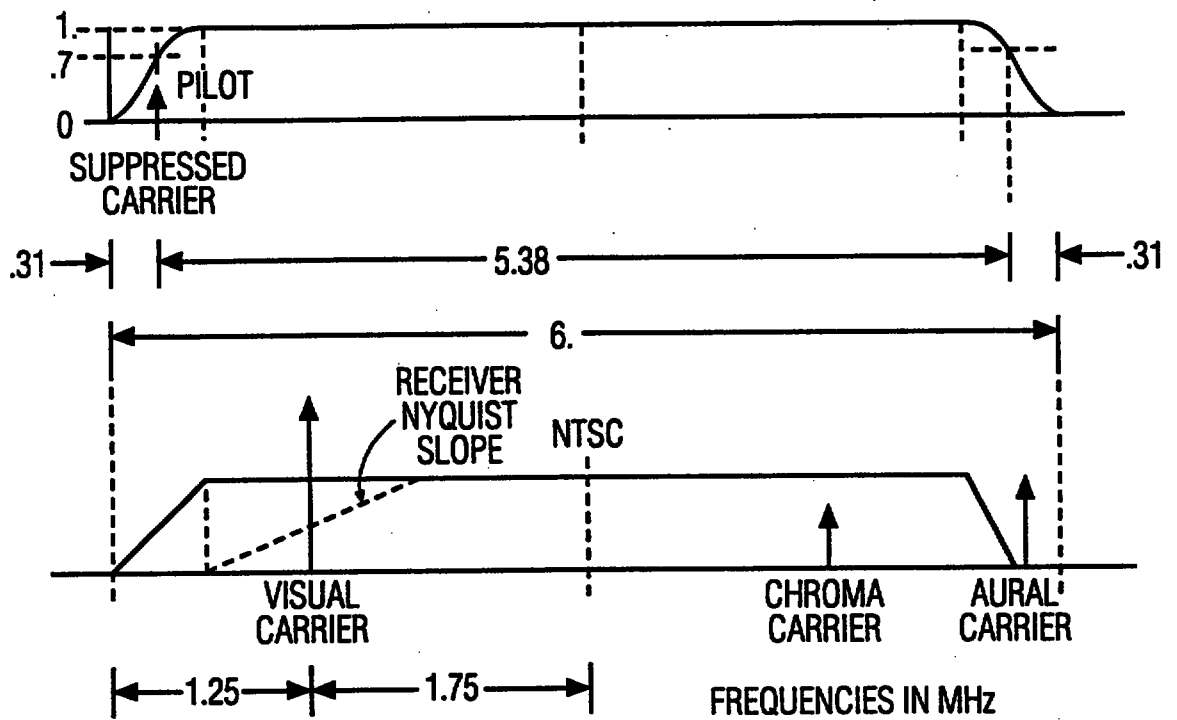
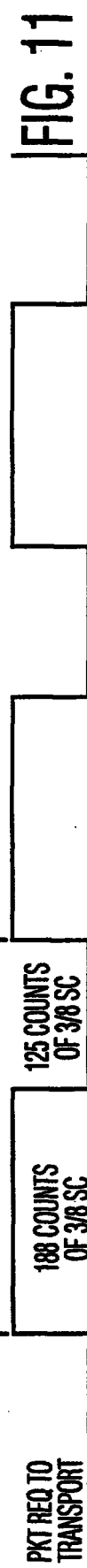
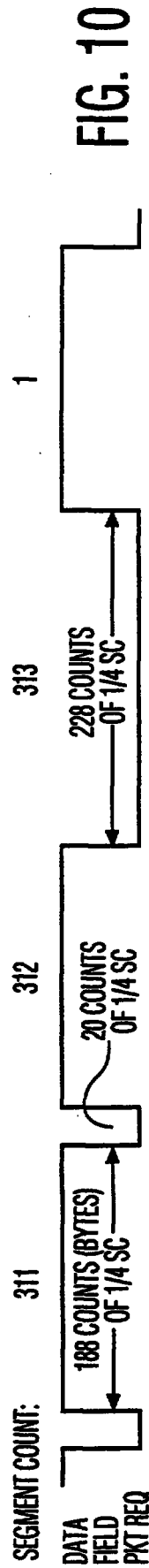
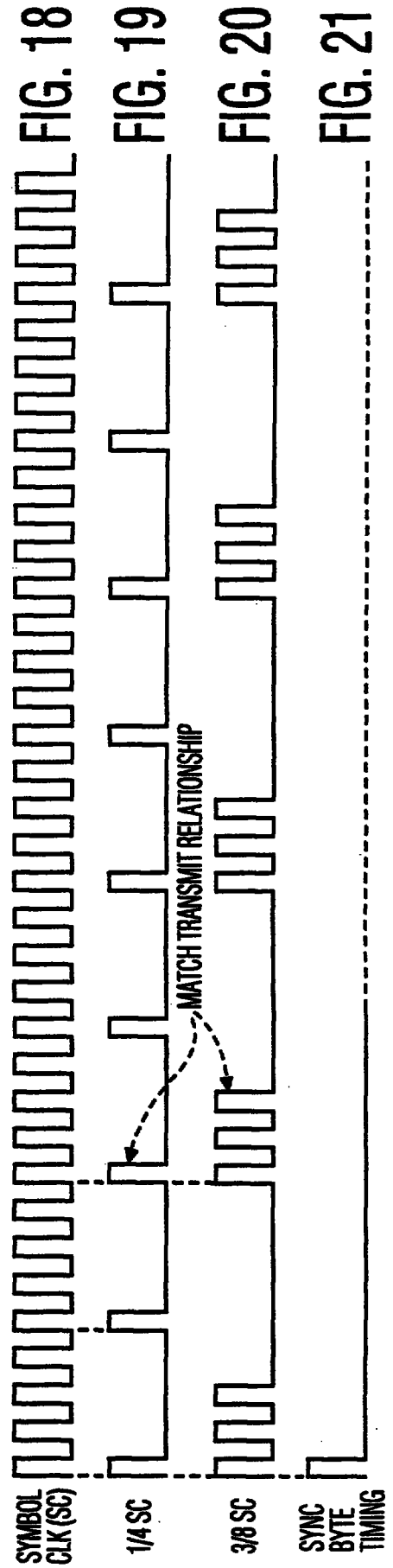
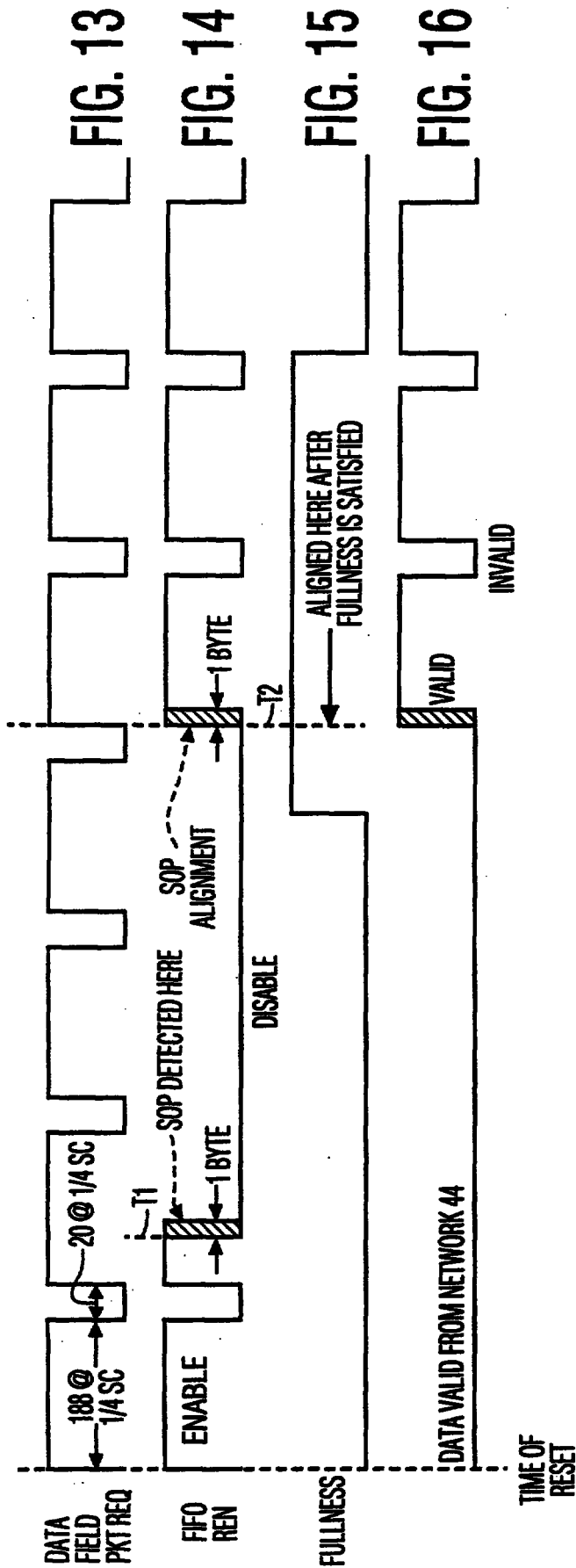


FIG. 5

5/13



6/13



7/13

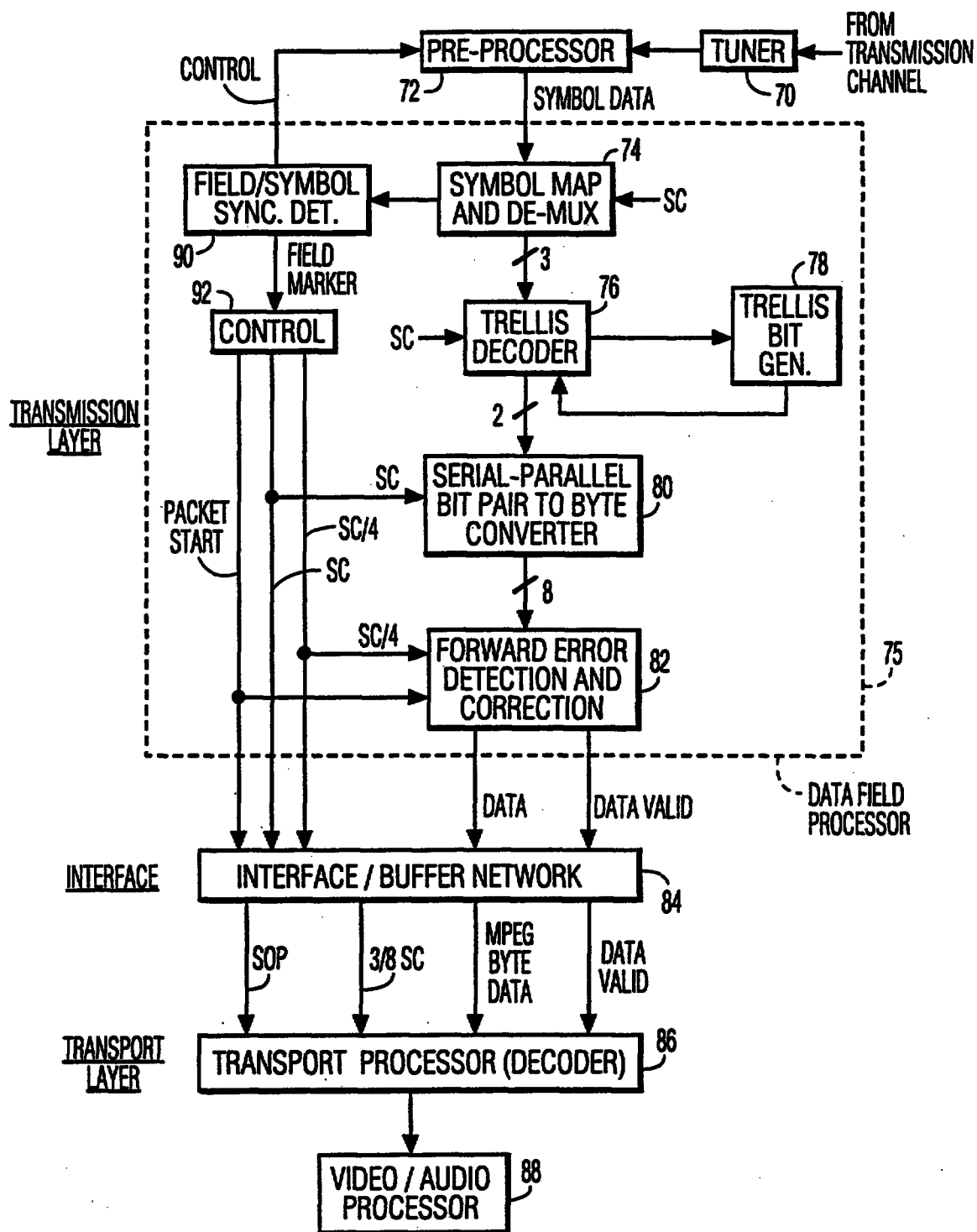
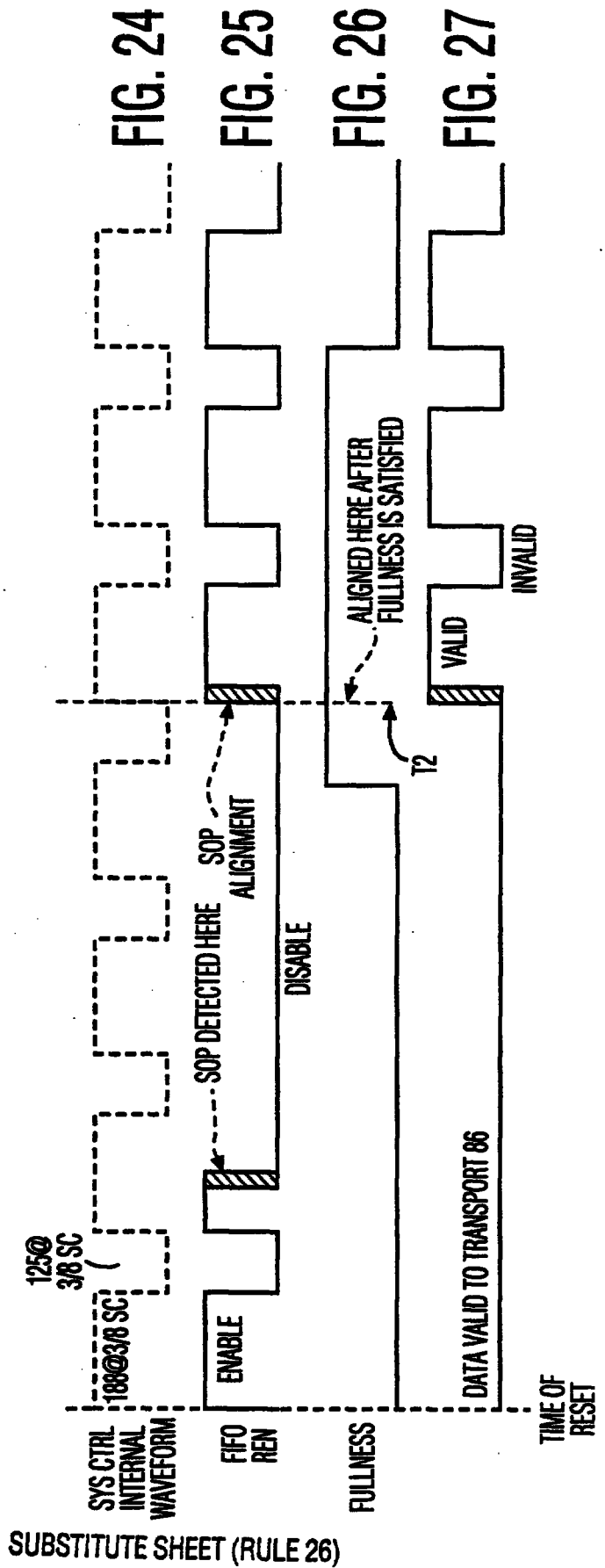
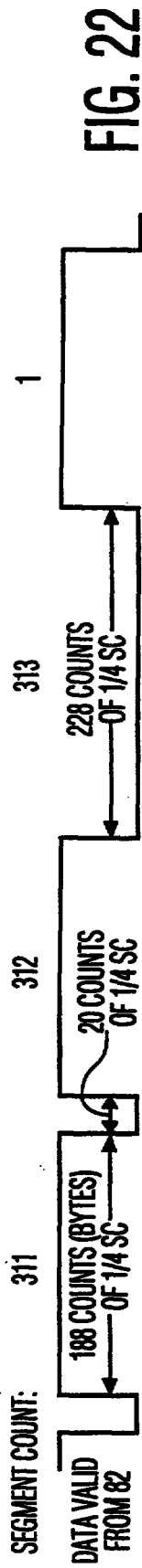


FIG. 17

8/13



9/13

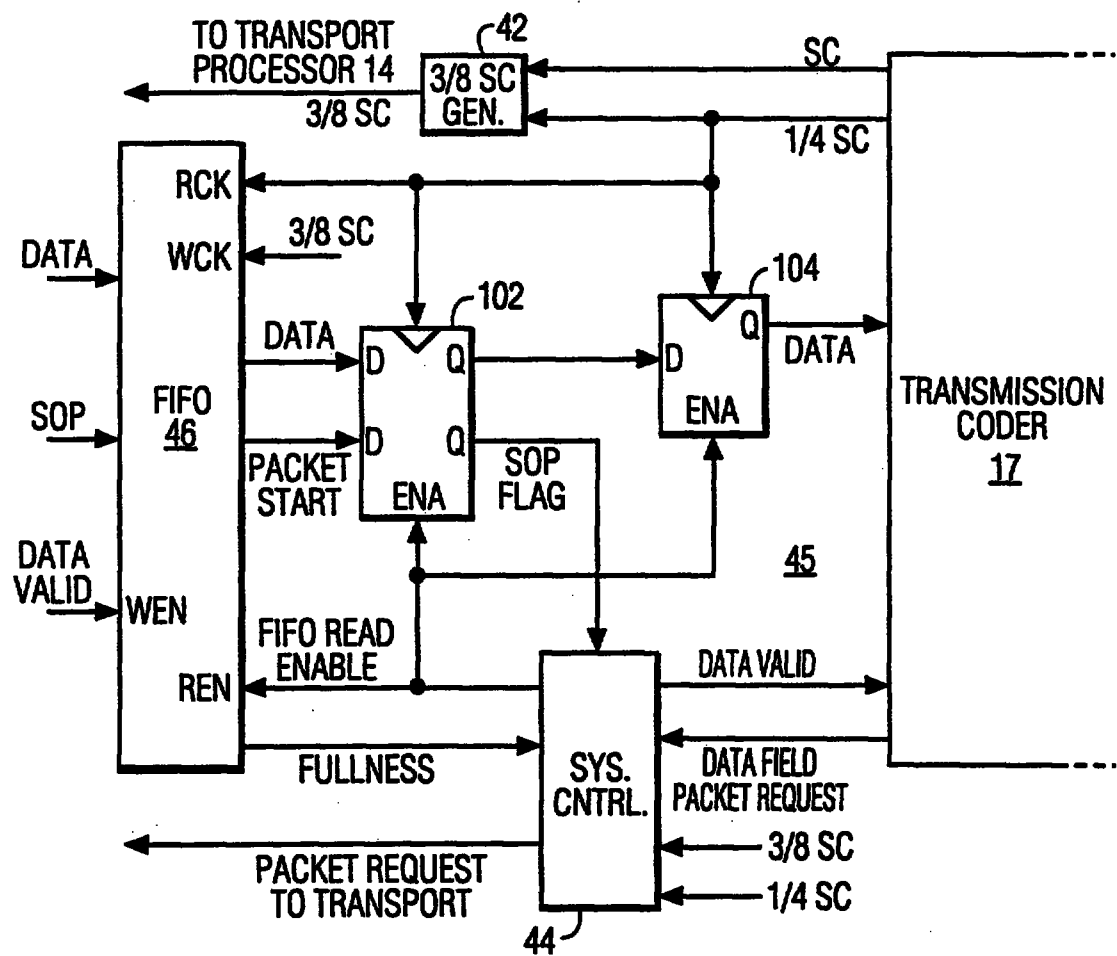


FIG. 28

10/13

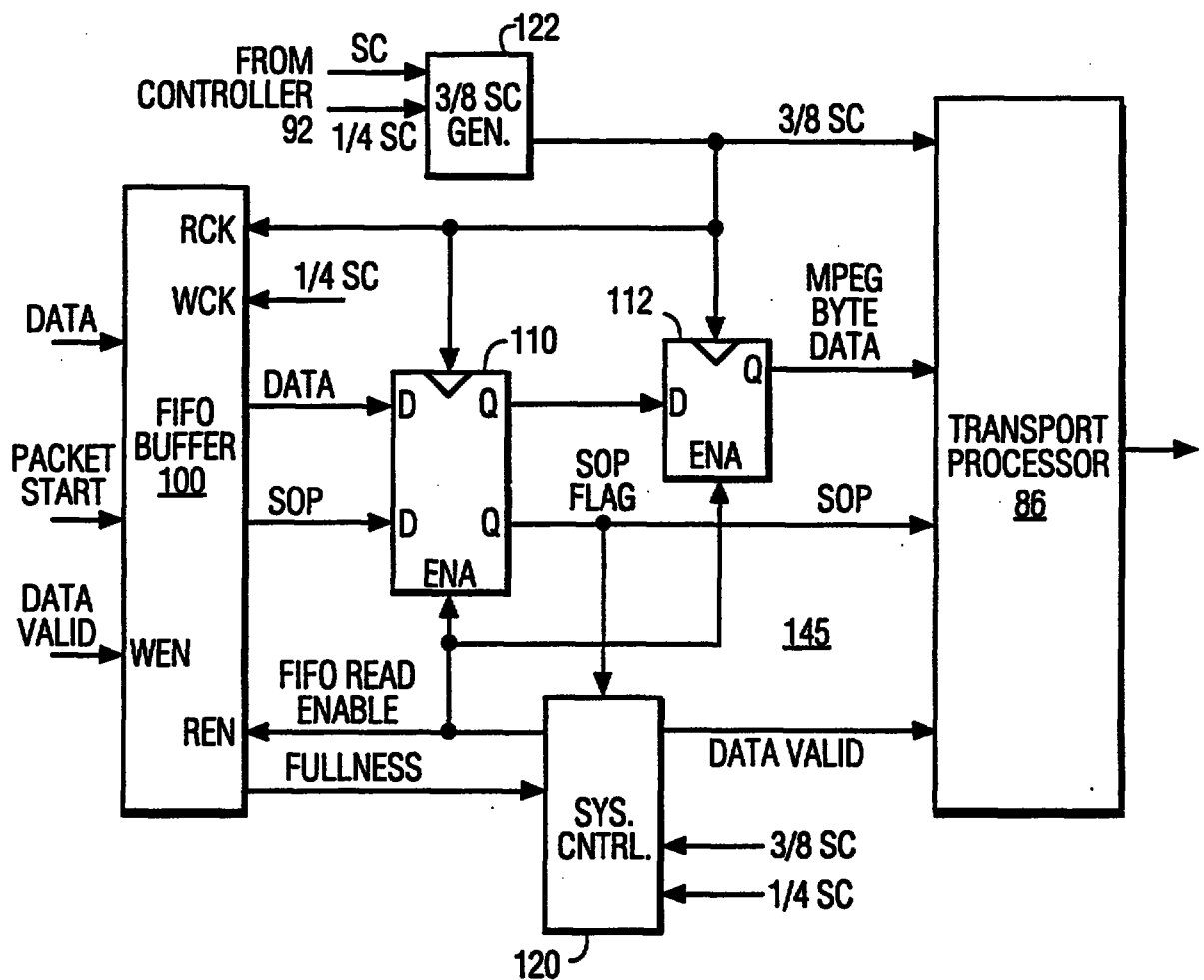


FIG. 29

11/13

FIG. 30

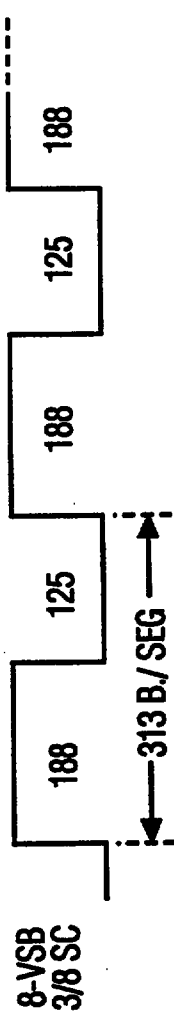
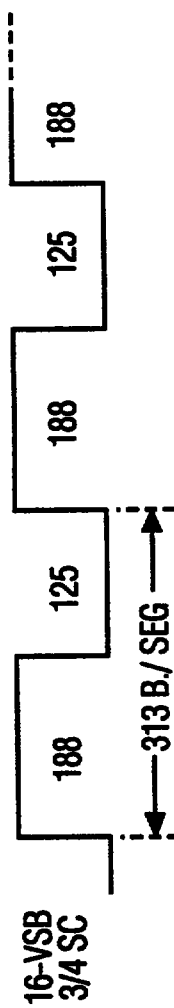


FIG. 31



FIG. 32



12/13

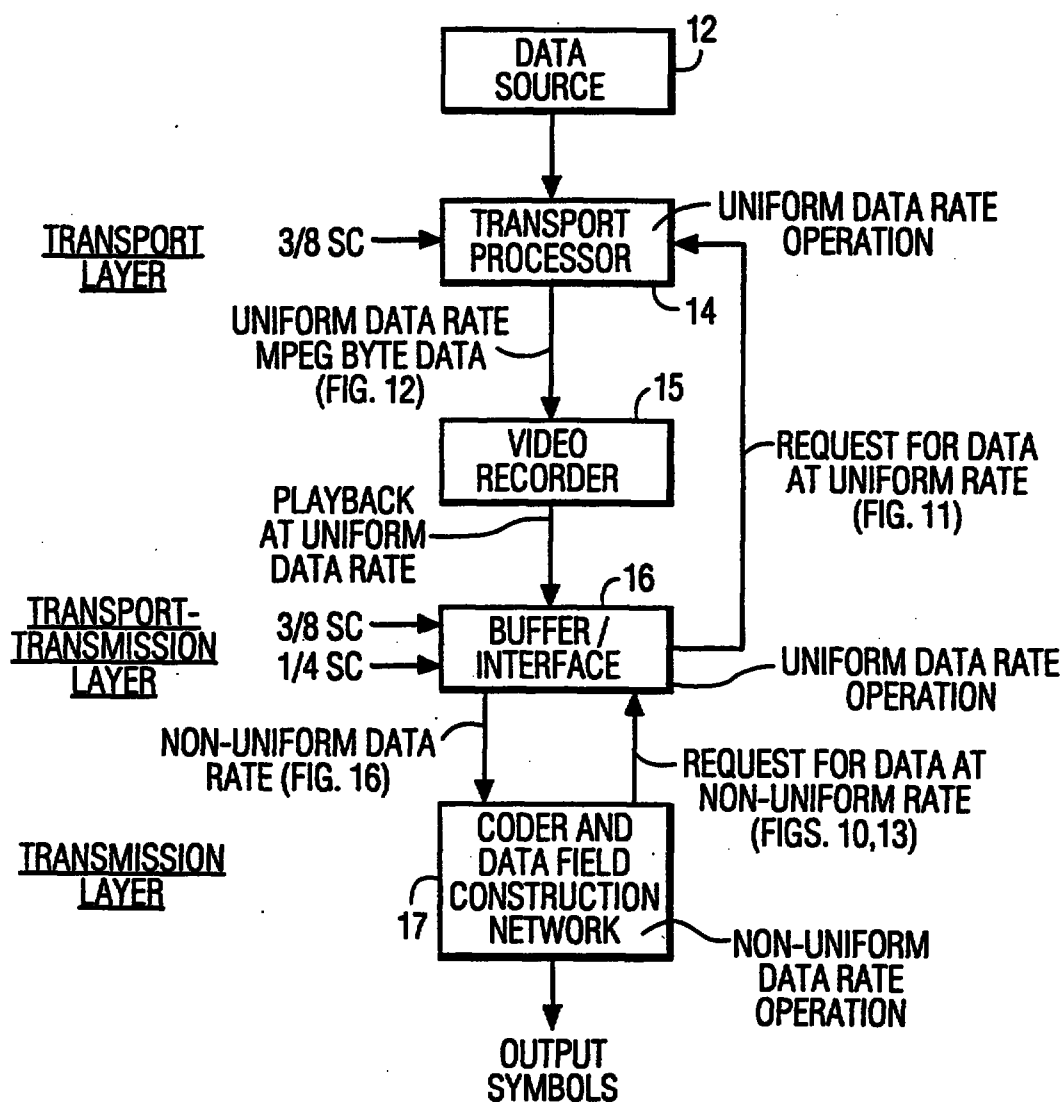


FIG. 33

13/13

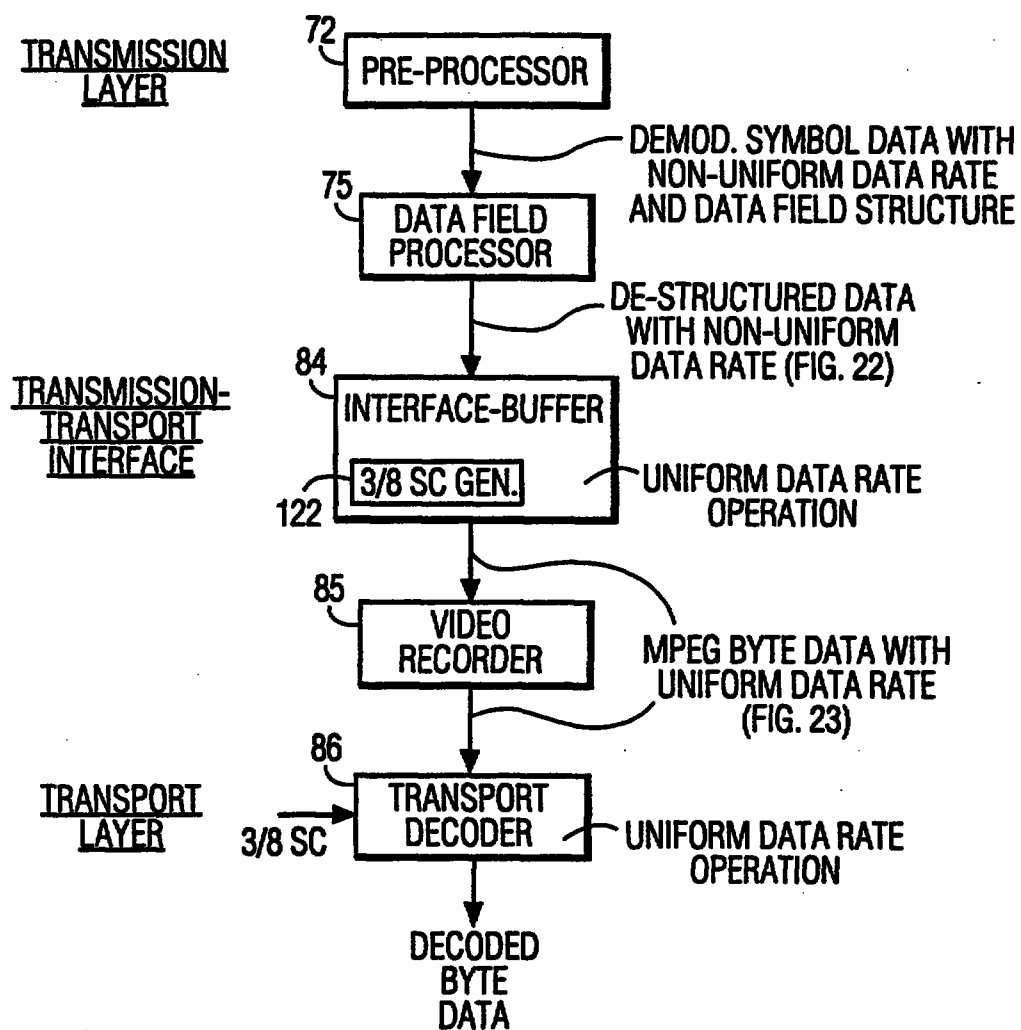


FIG. 34