CLAIMS

1. A non-volatile memory device comprising:

a first stack comprising first conductive patterns and first dielectric layers that are alternately stacked in a first direction on a substrate;

a second stack comprising second conductive patterns and second dielectric layers that are alternately stacked in the first direction on the first stack opposite the substrate;

a first monitoring channel structure that penetrates the first stack in the first direction; and

a second monitoring channel structure that penetrates the second stack in the first direction and is on the first monitoring channel structure,

wherein a width of a top of the first monitoring channel structure opposite the substrate is smaller than a width of a bottom of the second monitoring channel structure adjacent the top of the first monitoring channel structure,

wherein the non-volatile memory device further comprises a channel structure that penetrates the first stack and the second stack in the first direction, and

wherein the channel structure is configured to store data, and the first monitoring channel structure and the second monitoring channel structure are not configured to store data.

2. The non-volatile memory device of claim 1, further comprising:

a capping film on the second monitoring channel structure opposite the bottom thereof,

wherein a bottom of the capping film has a curved shape.

3. The non-volatile memory device of claim 1 or claim 2, further comprising:

a first channel structure that penetrates the first stack in the first direction; and

a second channel structure that penetrates the second stack in the first direction and is on the first channel structure,

wherein a width of a top of the first channel structure opposite the substrate is greater than a width of a bottom of the second channel structure adjacent the top of the first channel structure.

4. The non-volatile memory device of any one of claims 1 to 3, wherein the width of the top of the first monitoring channel structure is smaller than a narrowest width of the second monitoring channel structure.

5. The non-volatile memory device of claim 1 or claim 2, further comprising:

a first channel structure that penetrates the first stack in the first direction; and

a second channel structure that penetrates the second stack in the first direction and is placed on the first channel structure,

wherein a width of a top of the first channel structure opposite the substrate is the same as a width of a top of the second channel structure opposite the top of the first channel structure.

6. A non-volatile memory device comprising:

a first stack comprising first conductive patterns and first dielectric layers that are alternately stacked in a first direction;

a second stack comprising second conductive patterns and second dielectric layers that are alternately stacked in the first direction on the first stack;

a first monitoring channel structure that penetrates the first stack in the first direction;

a second monitoring channel structure that penetrates the second stack in the first direction and is on the first monitoring channel structure; and

a capping film on the second monitoring channel structure,

wherein a width of a top of the first monitoring channel structure is smaller than a width of a bottom of the second monitoring channel structure that is opposite the capping film,

the first monitoring channel structure and the second monitoring channel structure comprise a data storage layer, a channel layer, and a buried insulating layer that are sequentially stacked along side walls of the first monitoring channel structure and side walls of the second monitoring channel structure,

wherein the non-volatile memory device further comprises a channel structure that penetrates the first stack and the second stack in the first direction,

wherein the channel structure is configured to store data, and the first monitoring channel structure and the second monitoring channel structure are not configured to store data.

7. The non-volatile memory device of claim 6, wherein a bottom of the capping film is adjacent the buried insulating layer and has a curved shape.

8. The non-volatile memory device of claim 6 or claim 7, further comprising:

a first channel structure that penetrates the first stack in the first direction; and

a second channel structure that penetrates the second stack in the first direction and is on the first channel structure,

wherein a width of a top of the first channel structure opposite a substrate is greater than a width of a bottom of the second channel structure adjacent the top of the first channel structure.

9. The non-volatile memory device of any one of claims 6 to 8, wherein the width of the top of the first monitoring channel structure is smaller than a narrowest width of the second monitoring channel structure.

10. The non-volatile memory device of claim 6 or claim 7, further comprising:

a first channel structure that penetrates the first stack in the first direction; and

a second channel structure that penetrates the second stack in the first direction and is on the first channel structure,

wherein a width of a top of the first channel structure opposite a substrate is the same as a width of a top of the second channel structure opposite the top of the first channel structure.

11. A non-volatile memory system comprising:

a non-volatile memory device comprising:

a first stack comprising first conductive patterns and first dielectric layers that are alternately stacked in a first direction on a substrate;

a second stack comprising second conductive patterns and second dielectric layers that are alternately stacked in the first direction on the first stack opposite the substrate;

a first monitoring channel structure that penetrates the first stack in the first direction;

a second monitoring channel structure that penetrates the second stack in the first direction and is on the first monitoring channel structure, a width of a top of the first monitoring channel structure opposite the substrate being smaller than a width of a bottom of the second monitoring channel structure adjacent the top of the first monitoring channel structure;

a peripheral circuit comprising a decoder, a page buffer, and a logic circuit; and

an I/O pad that is electrically connected to the peripheral circuit; and

a controller that is electrically connected to the non-volatile memory device through the I/O pad and is configured to control the non-volatile memory device,

wherein the non-volatile memory system further comprises a channel structure that penetrates the first stack and the second stack in the first direction, and

wherein the channel structure is configured to store data, and the first monitoring channel structure and the second monitoring channel structure are not configured to store data.

12. The non-volatile memory system of claim 11, further comprising:

a capping film on the second monitoring channel structure opposite the bottom thereof; and

a data storage layer, a channel layer, and a buried insulating layer stacked sequentially along side walls of the first monitoring channel structure and side walls of the second monitoring channel structure.

13. The non-volatile memory system of claim 12, wherein a bottom of the capping film adjacent the buried insulating layer has a curved shape.

14. The non-volatile memory system of any one of claims 11 to 13, further comprising:

a first channel structure that penetrates the first stack in the first direction; and

a second channel structure that penetrates the second stack in the first direction and is on the first channel structure,

wherein a width of a top of the first channel structure opposite the substrate is greater than a width of a bottom of the second channel structure adjacent the top of the first channel structure.

15. The non-volatile memory system of any one of claims 11 to 14, wherein the first monitoring channel structure extends from the bottom of the second monitoring channel structure to the substrate, and wherein the width of the top of the first monitoring channel structure is smaller than a narrowest width of the second monitoring channel structure.