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(54) IMPROVEMENTS IN OR RELATING TO SEMICONDUCTOR MEMORY APPARATUS

(71) We, WESTERN ELECTRIC COMPANY, INCORPORATED, of 195, Broadway, New York City, New York State, United States of America, a Corporation organised and existing under the laws of the State of New York, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to semiconductor memory apparatus.

In many computer and other systems there exists the need for large information capacity semiconductor memories in which digital information can be temporarily stored and then retrieved within a useful period of time. In furtherance of this need, it is desirable that each individual memory cell of the array require as little semiconductor area for its implementation as possible and contain as few terminals as possible.

In the publication *Electronics Review* of March 1, 1971, an article entitled "Bipolar Memory Cells Strike Back in War with MOS" on page 19 and copending Application No. 60662/71 (Serial No. 1,358,190), a two-terminal memory cell comprising a single junction transistor is described. This structure requires an extremely small semiconductor area for its implementation and contains only two terminals, but requires avalanche breakdown of one of the junctions of the transistor. While this cell has many desirable electrical and physical features, it is recognized that repeated avalanche breakdown tends to degrade semiconductor device performance.

United States Patent No. 3,693,173 describes a two-terminal memory array comprising a plurality of interconnected two-terminal memory cells each of which comprises two serially connected PNP transistors. This memory cell has many desirable electrical characteristics and does not utilize avalanche breakdown. However, its physical size is still

approximately five times that of the single transistor cell previously discussed.

According to this invention semiconductor memory apparatus includes a plurality of member cells each for storing bit information and each of which includes first and second terminals, and first and second complementary-type junction transistors, the collector of the first transistor comprising said first terminal, the emitters of the transistors being electrically coupled and comprising said second terminal, the collector and base of the first transistor being coupled to the base and collector respectively of the second transistor, and the base of the first transistor being capacitively coupled to said first and second terminals.

Preferably in each cell the first transistor is NPN-type, and the second transistor is PNP-type.

The apparatus may include first and second control means coupled respectively to the first terminals and to the second terminals of said cells and adapted to cooperate for respectively (i) causing conduction in the first transistor of a selected cell only if the potential of the base of that transistor represents a predetermined binary value and for causing the potential of the base of that transistor to be set to a potential representative of the other binary value, and (ii) forward biasing the emitter-base junction of the second transistor of a selected cell to set the potential of the base of the first transistor of the selected cell to said potential representative of said predetermined binary value; and detection means coupled to the second terminals of said cells for detecting conduction in said first transistors.

The invention will now be described with reference to the accompanying drawing, in which:

Fig. 1 illustrates schematically memory apparatus embodying the invention;

Fig. 2 illustrates schematically a preferred circuit of one memory cell of the apparatus of Fig. 1;

Figs. 3 and 4 graphically illustrate the potentials applied in operation to the terminals of a selected memory cell as a function of time; and

5 Figs. 5 and 6 illustrate the corresponding potential of the base of the NPN transistor as a function of time and the conduction through it as a function of time, respectively.

Referring now to Fig. 1, a plurality of individual memory cells 12 are arranged in a two-dimensional array of M rows and N columns to form a memory having $M \times N$ memory cells. Each of the memory cells 12, having two terminals, 14 and 16, as illustrated, is capable of storing bit information for a useful period of time. Each terminal 16 is connected to a word line 18 and each terminal 14 is connected to a digit line 20. All of the word lines 18 are connected to word line voltage control circuits 22 and all of the digit lines 20 are connected to digit line voltage control circuits 24 and conduction detectors 26.

Referring now to Fig. 2, the cell shown inside the broken line rectangle 12 comprises a preferred form of the inner structure of cell 12 of Fig. 1. As illustrated, the cell comprises an NPN junction transistor 30 and a PNP junction transistor 32. The base of the NPN transistor is common with the collector of the PNP transistor; the common node is denoted as 34. The emitters of both devices are coupled together and constitute terminal 14 of the memory cell. The collector of transistor 30 and the base of transistor 32 are coupled and constitute terminal 16 of the memory cell. Capacitance C_1 represents the equivalent parasitic capacitance associated with the collector-base junctions of both transistors. Capacitance C_2 represents the equivalent parasitic capacitance associated with the emitter-base junction of transistor 30 and the emitter collector of transistor 32.

Operation of the memory cell of Fig. 2 can be easily seen from the voltage and current graphs of Figs. 3, 4, 5 and 6. Figs. 3 and 4 illustrate the potentials applied to terminals 16 and 14 by the word line control circuits 22 through word line 18, and the digit line control circuits 24, through digit line 20, respectively, as a function of time. Fig. 5 illustrates the corresponding potential of the base 34 of transistor 30 as a function of time. Fig. 6 illustrates the current flowing through transistor 30 as a function of time.

As illustrated in Figs. 3 and 4, at time $T=0$ the voltage applied to terminal 16 is at a first positive level, v_1 , and terminal 14 is held at a reference potential which is a typically ground potential. Fig. 5 illustrates that the potential of the base 34 of transistor 30 is assumed to be at a positive potential which is defined as a "1" level. Typically this potential is .4 volt. Fig. 6

illustrates that there is no conduction in transistor 30 at $T=0$.

In order to read out the "1" stored in the cell and write a "0" into the cell, a positive polarity voltage pulse is applied at $T=t_1$ to node or terminal 16 by the word line control circuits 22 through word line 18. The leading edge of this pulse forces the potential of the collector of transistor 30 to potential v_2 . As shown in Fig. 4, at $T=t_1$, the voltage on node or terminal 14 remains at the reference potential. The increase in potential of the collector of transistor 30 is capacitively coupled through C_1 and C_2 to the base 34 of transistor 30. As is illustrated in Fig. 5, the potential of the base 34 increases in response to the change in potential at the collector until the emitter-base junction of transistor 30 is forward-biased and prevents any further increase in base potential. Transistor 30 then starts to conduct since the potential of its collector is more positive than that of the emitter and its emitter-base junction is forward-biased. The current flow, which is illustrated in Fig. 6, represents an output "1" signal. This is indicative of the fact that the voltage on the base 34 of transistor 30 was at the "1" level as was originally assumed. The width of the read voltage pulse is such that conduction in transistor 30 ceases prior to time $T=t_2$.

At $T=t_2$ the potential on the word line is decreased from v_2 to the reference potential. The trailing edge of the read waveform lowers the word line potential and, through capacitive coupling causes the potential of the base 34 of transistor 30 to decrease to a level which is defined as the "0" level. Typically, the "0" level is approximately -3.6 volts. It is clear, therefore, that the positive edge of the read voltage pulse causes a readout of a "1" from the memory cell and that the trailing edge causes a "0" to be written into the cell.

The initial read pulse voltage waveform is repeated in order to now read out the "0" which has been written into the cell. At $T=t_3$ the voltage on the word line is increased from the reference potential to v_1 while the potential on the digit line is held at the reference potential. This causes the potential on the base of transistor 30 to increase slightly from the "0" level, to a level which is significantly less positive than the "1" level. At $T=t_4$ the potential of the word line is increased from v_1 to v_2 . This, as is illustrated in Fig. 5, causes the base 34 of transistor 30 to increase in potential, but not sufficiently enough to cause the emitter-base junction of transistor 30 to be forward-biased and thereby allow conduction. This lack of conduction in transistor 30, as illustrated in Fig. 6, is indicative of a "0" stored in the cell.

At $T=t_2$, the potential of the word line potential is lowered to the reference potential. This causes the potential of the base of transistor 30 to return to the "0" level. During the entire interval from $T=t_2$ to $T=t_3$, the potential of the digit line is held at the reference potential. It is now clear that the read voltage pulse, which is applied to the word line (terminal 16) in addition to causing bit information stored in the cell to be read out, causes a "0" to be written into the cell.

In order to now write a "1" into the cell, the voltage on the digit line (terminal 14) is increased to v_1 at $T=t_3$, while the word line (terminal 16) is held at the reference potential. This causes the emitter-base junction of transistor 32 to be forward-biased and allows conduction within transistor 32 that causes the base 34 of transistor 30 to rise in potential to the "1" level at $T=t_3$, i.e. the initial base 34 potential assumed at $T=t_0$.

Preferably the two-terminal memory cells of Fig. 2 are used as components of the memory array of Fig. 1. Potentials v_1 and v_2 of Fig. 3 may be +1 and +8 volts, respectively. The time interval between $T=t_1$ and $T=t_2$ may be 60 nanoseconds. Potential v_1 of Fig. 4 may be +1 volt.

As has been denoted previously, the memory array of Fig. 1 is a word-organized memory. This means that when bit information is written into a selected memory cell information in all other memory cells coupled to the same word line is affected. In order to ensure that bit information stored in all memory cells not connected to the word line containing a selected cell is not affected during the write or read operations of the selected cell, it is necessary to maintain the nonselected word lines all at potential v_1 . This ensures that information stored within these nonselected cells will not be disturbed.

The memory cell of Fig. 2 can be fabricated using standard integrated circuit fabrication techniques in approximately 2 square mils of a semiconductive substrate. Starting with a P-type semiconductor substrate, an N-type epitaxial layer is deposited thereon which serves as the collector of the NPN transistor. A P-type diffusion is then made into a central portion of the N-type epitaxial layer and then an N-type diffusion is made within the P diffusion. The P diffusion serves as the base of the NPN transistor and the N diffusion serves as the base of the NPN transistor and the N diffusion serves as the emitter. A second P diffusion is then made in the N-type epitaxial layer relatively close to the initial P-type diffusion. This second P diffusion serves as the emitter of a lateral PNP transistor whose base is common with the collector of the NPN transistor and whose collector is common with

the base of the NPN transistor. The emitters of both transistors are then electrically connected and serve as one of the two terminals of the memory cell. A second electrical connection made to the N-type epitaxial layer serves as the second terminal of the memory cell.

From the foregoing, it is clear that the memory cell described herein is well-suited as a component for use in large information capacity memory arrays because its relatively simple structure allows for small physical size, only two connections need be made per cell, and there is no need for avalanche breakdown operation.

As will be apparent to those skilled in the art various modifications are possible. For example, a PNP transistor may be substituted for the NPN transistor and an NPN transistor may be substituted for the PNP transistor providing the relevant voltages are reversed. This configuration may be readily implemented using an oxide insulation fabrication scheme.

WHAT WE CLAIM IS:—

1. Semiconductor memory apparatus including a plurality of memory cells each for storing bit information and each of which includes first and second terminals, and first and second complementary-type junction transistors, the collector of the first transistor comprising said first terminal, the emitters of the transistors being electrically coupled and comprising said second terminal, the collector and base of the first transistor being coupled to the base and collector respectively of the second transistor, and the base of the first transistor being capacitively coupled to said first and second terminals.
2. Apparatus as claimed in claim 1 wherein in each cell the first transistor is NPN-type and the second transistor is PNP-type.
3. Apparatus as claimed in claim 1 or 2 including first and second control means coupled respectively to the first terminals and to the second terminals of said cells and adapted to cooperate for respectively (i) causing conduction in the first transistor of a selected cell only if the potential of the base of that transistor represents a predetermined binary value and for causing the potential of the base of that transistor to be set to a potential representative of the other binary value, and (ii) forward biasing the emitter-base junction of the second transistor of a selected cell to set the potential of the base of the first transistor of the selected cell to said potential representative of said predetermined binary value; and detection means coupled to the second terminals of



At $T=t_5$ the potential of the word line potential is lowered to the reference potential. This causes the potential of the base of transistor 30 to return to the "0" level. During the entire interval from $T=t_2$ to $T=t_5$ the potential of the digit line is held at the reference potential. It is now clear that the read voltage pulse, which is applied to the word line (terminal 16) in addition to causing bit information stored in the cell to be read out, causes a "0" to be written into the cell.

In order to now write a "1" into the cell, the voltage on the digit line (terminal 14) is increased to v_1 at $T=t_5$, while the word line (terminal 16) is held at the reference potential. This causes the emitter-base junction of transistor 32 to be forward-biased and allows conduction within transistor 32 that causes the base 34 of transistor 30 to rise in potential to the "1" level at $T=t_5$, i.e. the initial base 34 potential assumed at $T=t_0$.

Preferably the two-terminal memory cells of Fig. 2 are used as components of the memory array of Fig. 1. Potentials v_1 and v_2 of Fig. 3 may be +1 and +8 volts, respectively. The time interval between $T=t$ and $T=t_2$ may be 60 nanoseconds. Potential v_1 of Fig. 4 may be +1 volt.

As has been denoted previously, the memory array of Fig. 1 is a word-organized memory. This means that when bit information is written into a selected memory cell information in all other memory cells coupled to the same word line is affected. In order to ensure that bit information stored in all memory cells not connected to the word line containing a selected cell is not affected during the write or read operations of the selected cell, it is necessary to maintain the nonselected word lines all at potential v_1 . This ensures that information stored within these nonselected cells will not be disturbed.

The memory cell of Fig. 2 can be fabricated using standard integrated circuit fabrication techniques in approximately 2 square mils of a semiconductive substrate. Starting with a P-type semiconductor substrate, an N-type epitaxial layer is deposited thereon which serves as the collector of the NPN transistor. A P-type diffusion is then made into a central portion of the N-type epitaxial layer and then an N-type diffusion is made within the P diffusion. The P diffusion serves as the base of the NPN transistor and the N diffusion serves as the base of the NPN transistor and the N diffusion serves as the emitter. A second P diffusion is then made in the N-type epitaxial layer relatively close to the initial P-type diffusion. This second P diffusion serves as the emitter of a lateral PNP transistor whose base is common with the collector of the NPN transistor and whose collector is common with

the base of the NPN transistor. The emitters of both transistors are then electrically connected and serve as one of the two terminals of the memory cell. A second electrical connection made to the N-type epitaxial layer serves as the second terminal of the memory cell.

From the foregoing, it is clear that the memory cell described herein is well-suited as a component for use in large information capacity memory arrays because its relatively simple structure allows for small physical size, only two connections need be made per cell, and there is no need for avalanche breakdown operation.

As will be apparent to those skilled in the art various modifications are possible. For example, a PNP transistor may be substituted for the NPN transistor and an NPN transistor may be substituted for the PNP transistor providing the relevant voltages are reversed. This configuration may be readily implemented using an oxide insulation fabrication scheme.

WHAT WE CLAIM IS:—

1. Semiconductor memory apparatus including a plurality of memory cells each for storing bit information and each of which includes first and second terminals, and first and second complementary-type junction transistors, the collector of the first transistor comprising said first terminal, the emitters of the transistors being electrically coupled and comprising said second terminal, the collector and base of the first transistor being coupled to the base and collector respectively of the second transistor, and the base of the first transistor being capacitively coupled to said first and second terminals.

2. Apparatus as claimed in claim 1 wherein in each cell the first transistor is NPN-type and the second transistor is PNP-type.

3. Apparatus as claimed in claim 1 or 2 including first and second control means coupled respectively to the first terminals and to the second terminals of said cells and adapted to cooperate for respectively (i) causing conduction in the first transistor of a selected cell only if the potential of the base of that transistor represents a predetermined binary value and for causing the potential of the base of that transistor to be set to a potential representative of the other binary value, and (ii) forward biasing the emitter-base junction of the second transistor of a selected cell to set the potential of the base of the first transistor of the selected cell to said potential representative of said predetermined binary value; and detection means coupled to the second terminals of



said cells for detecting conduction in said first transistors.

- 5 4. Semiconductor memory apparatus arranged and adapted to operate substantially as herein described with reference to the accompanying drawings.

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