

**TITLE : A SCALABLE ARCHITECTURE FOR ASYNCHRONOUS TRANSFER MODE
SEGMENTATION AND REASSEMBLY**

ABSTRACT

A scalable, asynchronous transfer mode ("ATM") interface for generating an ATM cell comprising an addressing element, a memory element and a cell generating element. The addressing element is used to initiate generation of the ATM cell by transmitting one or more memory addresses to the memory element. The memory element, accessible to the addressing element, is used to store at least one datagram corresponding to the memory address(es) and to subsequently output the at least one datagram to the cell generating element. The cell generating element is coupled to the memory element in order to receive at least one datagram and produce the ATM cell. Finally, a controlling element is coupled to the addressing element and the cell generating element in order to control their operations.