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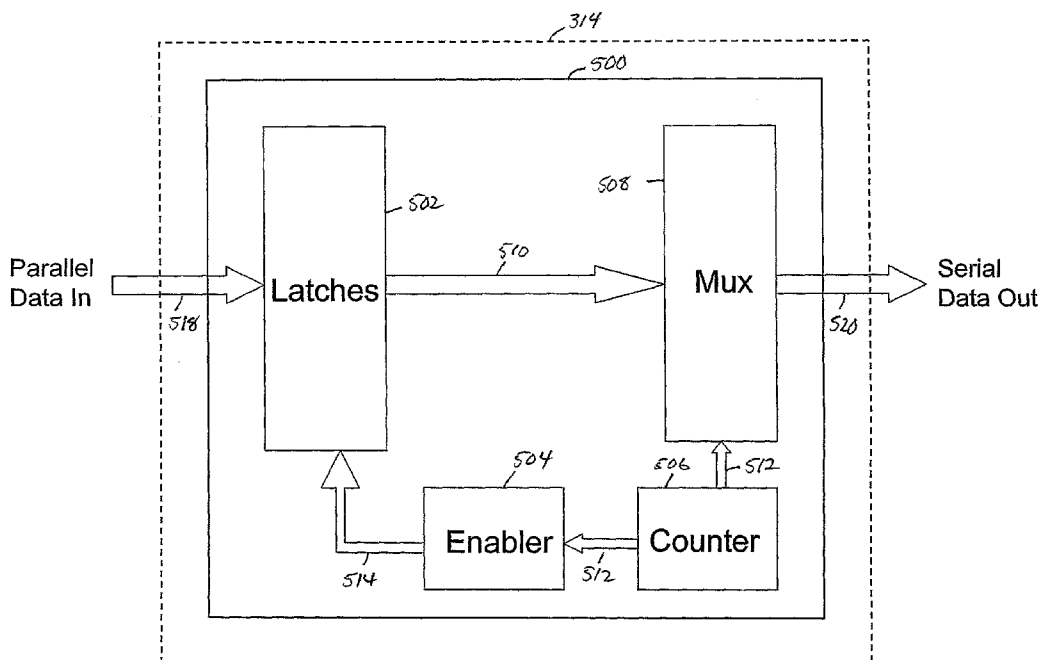
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Declarations under Rule 4.17:

— as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))

[Continued on next page]

(54) Title: DOUBLE DATA RATE SERIAL ENCODER



(57) Abstract: A double data rate serial encoder (Fig.5) is provided. The serial encoder comprises a mux (508) having a plurality of inputs (510), a plurality of latches (502) coupled to the inputs of the mux, an enabler (504) to enable the latches to update their data inputs (518), and a counter (506) to select one of the plurality of inputs of the mux for output. In another aspect, the mux (508) provides a glitch-less output (520) during input transitions. The mux includes an output selection algorithm optimized based on a priori knowledge of an input selection sequence provided by the counter.

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- *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

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