CLAIMS

1. A method of dicing a semiconductor wafer comprising a plurality of integrated circuits, the method comprising:

forming a mask above the semiconductor wafer, the mask comprising a layer covering and protecting the integrated circuits;

patterning the mask with a laser scribing process to provide a patterned mask with gaps, exposing regions of the semiconductor wafer between the integrated circuits;

subsequent to patterning the mask, performing a breakthrough treatment, the breakthrough treatment comprising a first physical bombardment operation, a second iterative isotropic and directional plasma etch operation subsequent to the first physical bombardment operation, and a third directional breakthrough operation subsequent to the second iterative isotropic and directional plasma etch operation; and

subsequent to performing the breakthrough treatment, plasma etching the semiconductor wafer through the gaps in the patterned mask to singulate the integrated circuits.

2. The method of claim 1, wherein the first physical bombardment operation of the breakthrough treatment comprises an Ar-only physical bombardment process performed at a source power greater than approximately 1500W, with a bias power of approximately 200W for a duration between 10 seconds and 120 seconds.

3. The method of claim 1, wherein the first physical bombardment operation of the breakthrough treatment removes physically attached debris from the gaps.

4. The method of claim 1, wherein the second iterative isotropic and directional plasma etch operation of the breakthrough treatment comprises an iterative isotropic and directional plasma etch process using SF_6 gas only, wherein the directional etch is performed using a power of approximately 1000W source and approximately a 200W bias power for a duration in the range of 0.4 – 1.5 second, and wherein the isotropic etch portion is performed using approximately 0W bias power for a duration in the range of 0.1 to 0.6 seconds.

5. The method of claim 4, wherein the isotropic and directional plasma etch processes are alternated iteratively to provide a cyclic etch treatment for a total treatment time in the range of 5 to 60 seconds.

6. The method of claim 1, wherein the third directional breakthrough operation of the breakthrough treatment comprises a combination of Ar and SF6 gases at an approximately 1500W source power and approximately 200 W bias and is performed for a duration in the range of 3-10 seconds.

7. The method of claim 6, wherein a total amount SF_6 is approximately 20-40% of a total SF_6/Ar volume.

8. The method of claim 1, wherein the first physical bombardment operation of the breakthrough treatment comprises an Ar-only physical bombardment process performed at a source power greater than approximately 1500W, with a bias power of approximately 200W for a duration between 10 seconds and 120 seconds, wherein the second iterative isotropic and directional

plasma etch operation of the breakthrough treatment comprises an iterative isotropic and directional plasma etch process using SF_6 gas only, wherein the directional etch is performed using a power of approximately 1000W source and approximately a 200W bias power for a duration in the range of 0.4 – 1.5 second, and wherein the isotropic etch portion is performed using approximately 0W bias power for a duration in the range of 0.1 to 0.6 seconds, and wherein the third directional breakthrough operation of the breakthrough treatment comprises a combination of Ar and SF6 gases at an approximately 1500W source power and approximately 200 W bias and is performed for a duration in the range of 3-10 seconds.

9. A system for dicing a semiconductor wafer comprising a plurality of integrated circuits, the system comprising:

a factory interface;

a laser scribe apparatus coupled with the factory interface and comprising a laser;

a first plasma etch chamber coupled with the factory interface, the first plasma etch chamber configured for performing a breakthrough treatment, the breakthrough treatment comprising a first physical bombardment operation, a second iterative isotropic and directional plasma etch operation subsequent to the first physical bombardment operation, and a third directional breakthrough operation subsequent to the second iterative isotropic and directional plasma etch operation; and

a second plasma etch chamber coupled with the factory interface, the second plasma etch chamber configured for performing a deep silicon plasma etch operation.

10. The system of claim 9, wherein the first physical bombardment operation of the breakthrough treatment comprises an Ar-only physical bombardment process performed at a source power greater than approximately 1500W, with a bias power of approximately 200W for a duration between 10 seconds and 120 seconds.

11. The system of claim 9, wherein the first physical bombardment operation of the breakthrough treatment removes physically attached debris from the gaps.

12. The system of claim 9, wherein the second iterative isotropic and directional plasma etch operation of the breakthrough treatment comprises an iterative isotropic and directional plasma etch process using SF_6 gas only, wherein the directional etch is performed using a power of approximately 1000W source and approximately a 200W bias power for a duration in the range of 0.4 – 1.5 second, and wherein the isotropic etch portion is performed using approximately 0W bias power for a duration in the range of 0.1 to 0.6 seconds.

13. The system of claim 12, wherein the isotropic and directional plasma etch processes are alternated iteratively to provide a cyclic etch treatment for a total treatment time in the range of 5 to 60 seconds.

14. The system of claim 9, wherein the third directional breakthrough operation of the breakthrough treatment comprises a combination of Ar and SF6 gases at an approximately 1500W source power and approximately 200 W bias and is performed for a duration in the range of 3-10 seconds.

15. The system of claim 14, wherein a total amount SF_6 is approximately 20-40% of a total SF_6/Ar volume.

16. The system of claim 9, wherein the first physical bombardment operation of the breakthrough treatment comprises an Ar-only physical bombardment process performed at a source power greater than approximately 1500W, with a bias power of approximately 200W for a duration between 10 seconds and 120 seconds, wherein the second iterative isotropic and directional plasma etch operation of the breakthrough treatment comprises an iterative isotropic and directional plasma etch process using SF_6 gas only, wherein the directional etch is performed using a power of approximately 1000W source and approximately a 200W bias power for a duration in the range of 0.4 – 1.5 second, and wherein the isotropic etch portion is performed using approximately 0W bias power for a duration in the range of 0.1 to 0.6 seconds, and wherein the third directional breakthrough operation of the breakthrough treatment comprises a combination of Ar and SF6 gases at an approximately 1500W source power and approximately 200 W bias and is performed for a duration in the range of 3-10 seconds.

17. A method of dicing a semiconductor wafer comprising a plurality of integrated circuits, the method comprising:

forming a mask layer above a silicon substrate, the mask layer covering and protecting integrated circuits disposed on the silicon substrate, the integrated circuits comprising a layer of silicon dioxide disposed above a layer of low K material and a layer of copper;

patterning the mask layer, the layer of silicon dioxide, the layer of low K material, the layer of copper, and a portion of the silicon substrate with a laser scribing process to expose regions of the silicon substrate between the integrated circuits;

subsequent to performing the laser scribing process, performing a breakthrough treatment, the breakthrough treatment comprising a first physical bombardment operation, a second iterative isotropic and directional plasma etch operation subsequent to the first physical bombardment operation, and a third directional breakthrough operation subsequent to the second iterative isotropic and directional plasma etch operation; and

subsequent to performing the breakthrough treatment, plasma etching the silicon substrate through the exposed regions of the silicon substrate to singulate the integrated circuits.

18. The method of claim 17, wherein the first physical bombardment operation of the breakthrough treatment comprises an Ar-only physical bombardment process performed at a source power greater than approximately 1500W, with a bias power of approximately 200W for a duration between 10 seconds and 120 seconds.

19. The method of claim 18, wherein the second iterative isotropic and directional plasma etch operation of the breakthrough treatment comprises an iterative isotropic and directional plasma etch process using SF_6 gas only, wherein the directional etch is performed using a power of approximately 1000W source and approximately a 200W bias power for a duration in the range of 0.4 – 1.5 second, and wherein the isotropic etch portion is performed using approximately 0W bias power for a duration in the range of 0.1 to 0.6 seconds.

20. The method of claim 19, wherein the third directional breakthrough operation of the breakthrough treatment comprises a combination of Ar and SF6 gases at an approximately 1500W source power and approximately 200 W bias and is performed for a duration in the range of 3-10 seconds.