

LEAD-ON-CHIP SEMICONDUCTOR DEVICE

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Abstract of the Disclosure

A semiconductor device (10) has a lead-on-chip (LOC) configuration. Leads (24) of the device have central portions (36) which are electrically coupled to peripheral bond pads (14) by
10 conductive wires (30). Inner portions (38) of the leads extend from the central portions toward centerline A-A for improved adhesion and to provide an internal clamping area (41) which stabilizes the leads during wire bonding. In one embodiment, tie bar (22) of leadframe (16) is used to distribute power across
15 semiconductor chip (12). The leadframe may also include chip alignment features (50) and tape alignment features (52) to align chip (12) and insulating tape (18) to the leadframe, respectively.

Fig. 1 accompanies this abstract.