

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
3 July 2008 (03.07.2008)

PCT

(10) International Publication Number
WO 2008/077240 A1

(51) International Patent Classification:

GI1C 17/14 (2006.01) **GI1C 8/08** (2006.01)
GI1C 7/12 (2006.01)

(21) International Application Number:

PCT/CA2007/002287

(22) International Filing Date:

20 December 2007 (20.12.2007)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

60/871,519 22 December 2006 (22.12.2006) US

(71) Applicant (for all designated States except US): **SIDENSE CORP.** [CA/CA]; 84 Hines Road, Suite 260, Ottawa, Ontario K2K 3G3 (CA).

(72) Inventor; and

(75) Inventor/Applicant (for US only): **KURJANOWICZ, Wlodek** [CA/CA]; 56 Sherring Crescent, Ottawa, Ontario K2K 2T1 (CA).

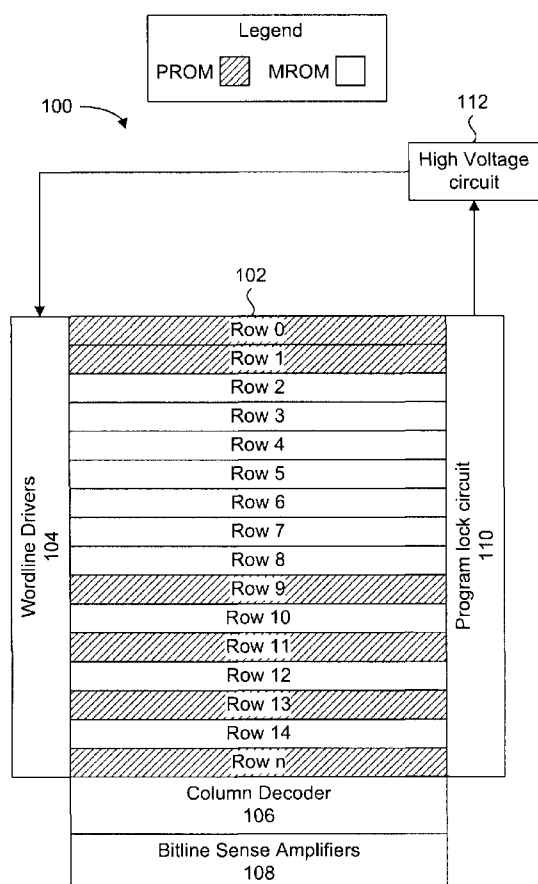
(74) Agents: **HUNG, Shin** et al.; Borden Ladner Gervais LLP, World Exchange Plaza, 100 Queen Street, Suite 1100, Ottawa, Ontario K1P 1J9 (CA).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, PL,

[Continued on next page]

(54) Title: MASK PROGRAMMABLE ANTI-FUSE ARCHITECTURE



(57) Abstract: A memory array having both mask programmable and one-time programmable memory cells connected to the wordlines and the bitlines. All memory cells of the memory array are configured as one-time programmable memory cells. Any number of these one-time programmable memory cells are convertible into mask programmable memory cells through mask programming, such as diffusion mask programming or contact/via mask programming. Manufacturing of such a hybrid memory array is simplified because both types of memory cells are constructed of the same materials, therefore only one common set of manufacturing process steps is required. Inadvertent user programming of the mask programmable memory cells is inhibited by a programming lock circuit.



PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM,
GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report*

Declarations under Rule 4.17:

- *as to applicant's entitlement to apply for and be granted a
patent (Rule 4.17(ii))*
- *of inventorship (Rule 4.17(iv))*