

ABSTRACT

A semiconductor device includes a cell vertical active pattern and a peripheral vertical active pattern at the same vertical level; a cell upper extended source/drain pattern and a cell contact plug sequentially stacked on the cell vertical active pattern; a peripheral upper extended source/drain pattern and a peripheral contact plug sequentially stacked on the peripheral vertical active pattern; and an upper interconnection on the peripheral contact plug and the peripheral isolation pattern. A first distance between a vertical level of an upper end of the cell contact plug and a vertical level of an upper end of the cell isolation pattern is different from a second distance between a vertical level of an upper end of the peripheral contact plug and a vertical level of an upper end of the peripheral isolation pattern.

FIG. 4