CLAIMS

1. A semiconductor package structure, comprising:

a first base plate provided with a first surface;

a first chip stack body located on the first base plate, wherein the first chip stack body comprises a plurality of first semiconductor chips that are successively stacked onto one another in a direction perpendicular to the first base plate, and the first chip stack body is electrically connected to the first surface of the first base plate;

an interposer layer located on the first chip stack body, wherein the interposer layer is provided with a first interconnection surface, the first interconnection surface is provided with a first interconnection region and a second interconnection region, and the first interconnection region is electrically connected to the first base plate; and

a molding layer configured to seal the first chip stack body, the interposer layer and the first surface of the first base plate, wherein the first interconnection region is unsealed by the molding layer, the second interconnection region is sealed by the molding layer, and a first material layer is formed on a sidewall between the first interconnection region and a top surface of the molding layer on the second interconnection region;

a second material layer located on the top surface of the molding layer;

a second package structure, wherein the second package structure comprises a joint face and a first solder ball located on the joint face, the first solder ball is electrically connected to the first interconnection region, and the joint face is connected to the second material layer.

2. The semiconductor package structure of claim 1, wherein

a material of the first material layer comprises a conductive material or an insulation material.

3. The semiconductor package structure of claim 1,

wherein a material of the second material layer is the same as a material of the first material layer.

4. The semiconductor package structure of claim 1, further comprising:

a plurality of first conductive wires, wherein each of the plurality of first semiconductor chips is electrically connected to the first base plate by means of a respective one of the plurality of first conductive wires; and

a plurality of second conductive wires, wherein the second interconnection region is electrically connected to the first base plate by means of the plurality of second conductive wires.

5. The semiconductor package structure of claim 1, wherein

the first interconnection region comprises a plurality of first pads, and the second interconnection region comprises a plurality of second pads, wherein a number of the plurality of second pads is greater than a number of the plurality of first pads, and an area of each of the plurality of second pads is less than an area of each of the plurality of first pads.

6. The semiconductor package structure of claim 1, wherein

the sidewall between the first interconnection region and the top surface of the molding layer forms a first angle with the direction perpendicular to the first base plate, wherein the first angle is greater than or equal to 0° and less than 90°.

7. The semiconductor package structure of claim 1,

wherein there is a preset height between the first interconnection region and the top surface of the molding layer on the second interconnection region, and a height of the first solder ball is greater than the preset height.

8. A method for manufacturing a semiconductor package structure, comprising:

providing a first base plate, wherein the first base plate is provided with a first surface;

forming a first chip stack body on the first base plate, wherein the first chip stack body comprises a plurality of first semiconductor chips that are successively stacked onto one another in a direction perpendicular to the first base plate, and the first chip stack body is electrically connected to the first surface of the first base plate;

forming an interposer layer on the first chip stack body, wherein the interposer layer is provided with a first interconnection surface, the first interconnection surface is provided with a first interconnection region and a second interconnection region, and the first interconnection region is electrically connected to the first base plate; and

forming a molding layer, wherein the molding layer is configured to seal the first chip stack body, the interposer layer and the first surface of the first base plate, wherein the first interconnection region is unsealed by the molding layer, and the second interconnection region is sealed by the molding layer, wherein there is a preset height between the first interconnection region and a top surface of the molding layer on the second interconnection region, and a first material layer is formed on a sidewall between the first interconnection region and the top surface of the molding layer on the second interconnection region;

forming a second material layer on the top surface of the molding layer;

forming a second package structure, wherein the second package structure comprises a joint face and a first solder ball located on the joint face;

electrically connecting the first solder ball to the first interconnection region; and

connecting the joint face to the second material layer.

9. The method of claim 8, further comprising:

after forming the interposer layer,

forming a plurality of first conductive wires, wherein each of the plurality of first semiconductor chips is electrically connected to the first base plate by means of a respective one of the plurality of first conductive wires; and

forming a plurality of second conductive wires, wherein the second interconnection region is electrically connected to the first base plate by means of the plurality of second conductive wires.

10. The method of claim 8, further comprising:

forming a plurality of first pads on the first interconnection region; and forming a plurality of second pads on the second interconnection region, wherein a number of the plurality of second pads is greater than a number of the plurality of first pads, and an area of each of the plurality of second pads is less than an area of each of the plurality of first pads.

11. The method of claim 8, further comprising:

after forming the interposer layer, forming a covering layer on the first interconnection region of the interposer layer, wherein the covering layer comprises a first portion and second portions located on two sides of the first portion, and the first portion and the second portions form an inverted U-shape to form a sealed cavity with the interposer layer; wherein an angle between each of the second portions and the direction perpendicular to the first base plate is a first angle, and the first angle is greater than or equal to 0° and less than 90°.

12. The method of claim 11, wherein

a material of the covering layer comprises a conductive material or an insulation material.

13. The method of claim 11, further comprising:

forming a molding layer pre-layer which is configured to seal the first chip stack body, the interposer layer, the covering layer and the first surface of the first base plate; and

removing a part of the molding layer pre-layer and the first portion of the covering layer, wherein the second portions are retained to form the first material layer.

14. The method of claim 8, wherein a material of the second material layer is the same as a material of the first material layer.

15. The semiconductor package structure of claim 1, wherein the first base plate includes a first signal transmission region located on one side of the first base plate, and a second signal transmission region located on another side of the first base plate opposite to the one side, and the first signal transmission region is electrically connected to the first chip stack body, and the second signal transmission region is electrically connected to the interposer layer.