CLAIMS

1. A semiconductor device comprising:

a first transistor over a substrate, the first transistor comprising a first semiconductor layer including a first channel formation region, a first gate electrode, a first source electrode and a first drain electrode;

a logic circuit comprising a second transistor over the substrate, the second transistor comprising a second semiconductor layer including a second channel formation region, a second gate electrode, a second source electrode and a second drain electrode; and

a capacitor over the substrate, the capacitor comprising two electrodes,

wherein the first transistor is provided over the logic circuit,

wherein one of the first source electrode and the first drain electrode is electrically connected to the second gate electrode of the second transistor, and one of the electrodes of the capacitor,

wherein the first transistor is electrically separated from the other of the electrodes of the capacitor, and

wherein the first semiconductor layer comprises an oxide semiconductor in the first channel formation region.

2. The semiconductor device according to claim 1, wherein an off-current of the first transistor is 1×10^{-17} A/μm or less.

3. The semiconductor device according to claim 1,

wherein the logic circuit comprises an inverter, and

wherein the second transistor is included in the inverter.

4. The semiconductor device according to claim 1, wherein the semiconductor device is designed so that an input signal is applied to the logic circuit through the first transistor when the first transistor is in an on state, and the input signal is stored at the second gate electrode of the second transistor when the first transistor is in an off state.

5. The semiconductor device according to claim 1, wherein the first transistor is provided above the logic circuit.

6. A semiconductor device comprising:

a first transistor over a substrate, the first transistor comprising a first semiconductor layer including a first channel formation region, a first gate electrode, a first source electrode and a first drain electrode;

an insulating layer over the first transistor, the insulating layer including an opening;

a first electrode in the opening, the first electrode being in contact with one of the first source electrode and the first drain electrode;

a logic circuit comprising a second transistor over the substrate, the second transistor comprising a second semiconductor layer including a second channel formation region, a second gate electrode, a second source electrode and a second drain electrode;

a second electrode in contact with the second gate electrode; and

a capacitor over the substrate, the capacitor comprising two electrodes,

wherein the first transistor is provided over the logic circuit,

wherein the one of the first source electrode and the first drain electrode is electrically connected to the second gate electrode of the second transistor through the first electrode and the second electrode, and is electrically connected to one of the electrodes of the capacitor,

wherein the first transistor is electrically separated from the other of the electrodes of the capacitor,

wherein the first semiconductor layer comprises an oxide semiconductor in the first channel formation region, and

wherein a top surface of the first electrode is effectively in conformity to a top surface of the insulating layer.

7. The semiconductor device according to claim 6, wherein the first electrode and the insulating layer are planarized by CMP method.

8. The semiconductor device according to claim 6, wherein an off-current of the first transistor is 1×10^{-17} A/μm or less.

9. The semiconductor device according to claim 6,
wherein the logic circuit comprises an inverter, and
wherein the second transistor is included in the inverter.

10. The semiconductor device according to claim 6, wherein the semiconductor device is designed so that an input signal is applied to the logic circuit through the first transistor when the first transistor is in an on state, and the input signal is stored at the second gate electrode of the second transistor when the first transistor is in an off state.

11. The semiconductor device according to claim 6, wherein the first transistor is provided above the logic circuit.

12. The semiconductor device according to claim 6, wherein the first electrode and the second electrode do not overlap each other.