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"A semiconductor memory"

The present invention relates to a semiconductor memory, and more particularly to a semiconductor memory which includes insulated-gate field

effect transistors (hereinafter referred to as "MOSFETs")
5 as principal circuit elements.

Semiconductor memories, for example, random access memories (RAMs) are classified into the dynamic type and the static type. Since the dynamic type RAM is smaller than the static type in the number
10 of elements constituting memory cells for storing data, the former is readily rendered large in capacity as compared with the latter. The dynamic type RAM, however, needs to be externally supplied with more timing signals for operation than those of the static type
15 RAM and has the disadvantage of a difficult timing control.

We have therefore thought out a pseudo static type RAM which can be put into a large memory capacity and the external timing control of which
20 is simple as in the static type RAM.

According to the present invention there is provided a semiconductor memory including:

(a) a plurality of dynamic memory cells;

(b) a first selector circuit which receives first address signals, and which selects one of said plurality of dynamic memory cells specified by the first address signals, and the time of operation of which is controlled by a first timing signal;

(c) a plurality of pairs of data lines connected to said dynamic memory cells so that each pair of data lines is respectively provided with a potential difference in accordance with the data read out from a selected dynamic memory cell;

(d) a plurality of sense amplifiers each of which has a pair of input and output terminals that are coupled to a corresponding pair of data lines, the respective sense amplifiers having their operations controlled by second timing signals;

(e) a first precharge circuit which is coupled to said plurality of pairs of data lines and operates so as to precharge said data lines at a potential intermediate between binary signal levels to be stored in dynamic memory cells in accordance with a third timing signal;

(f) a first detector circuit including means connected to receive said first address signals for detecting level changes in the first address signals; and

(g) a timing generator circuit connected to

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receive the detection outputs of said first detector circuit, and including means for generating said third timing signal for operating said first precharge circuit, said first timing signal for operating said
5 first selector circuit after stopping the operation of said first precharge circuit, and said second timing signals for operating said sense amplifiers.

The present invention will now be described in greater detail by way of example with reference to the accompanying drawings, wherein:-

Figure 1 is a block diagram showing a preferred
5 form of semiconductor memory;

Figures 2A and 2B are circuit diagrams showing detailed circuit arrangements of the semiconductor memory shown in Figure 1; and

Figure 3 is a waveform diagram which assists
10 in the explanation of the operation of the semiconductor memory.

Referring to Figure 1, various circuit blocks enclosed with a dotted line are formed on a single semiconductor substrate by the manufacturing technology
15 of known CMOS (Complementary Metal-Oxide-Semiconductor) integrated circuits. Terminals I/O; $A_{i+1} - A_j$; $\overline{CS}$, $\overline{WE}$; $A_0 - A_i$; and V_{CC} , V_{SS} are formed as the external terminals of the single chip. A supply voltage is fed across the terminals V_{CC} and V_{SS} from an external
20 power source unit (not shown).

A memory array M-ARY is composed of known 1-MOSFET type memory cells arranged in the shape of a matrix. Each memory cell is constructed of one MOSFET and one capacitor. In the embodiment disclosed,
25 the memory array has the folded bit line organization, although it will be appreciated that the invention

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is not restricted thereto. In the memory array of the folded bit line organization, the respective memory cells have their input or output nodes coupled to either of a pair of complementary data lines D and $\bar{D}$ extended on the semiconductor substrate in parallel to each other, as will be understood with reference to Figures 2A and 2B to be described later.

A data line precharge circuit PC_1 is constructed of a MOSFET that short-circuits the complementary data lines D and $\bar{D}$ by receiving a precharge pulse ϕ_{pcl} .

A sense amplifier SA is constructed of a plurality of unit circuits each of which is made up of a CMOS (complementary type metal-oxide-semiconductor) FET latch circuit, and power switch MOSFETs which are respectively located on the supply voltage V_{CC} side of the unit circuits and the earth potential V_{SS} side of the circuitry. A pair of input and output nodes of the sense amplifier are coupled to the complementary data lines D and $\bar{D}$ corresponding thereto. The power switch MOSFETs located on the supply voltage V_{CC} side and the earth potential V_{SS} side of the circuitry, respectively, have their conductance controlled by timing signals $\overline{\phi_{pa1}}$, $\overline{\phi_{pa2}}$ and ϕ_{pa1} , ϕ_{pa2} .

A column switch C-SW is provided by which only one pair of complementary data lines to be

selected are coupled to common complementary data lines in accordance with column select signals supplied from a column address decoder C-DCR to be described later.

5 An X address buffer X-ADB forms internal complementary address signals $a_0, \overline{a_0}$ to $a_i, \overline{a_i}$ by receiving external address signals through the terminals A_0 to A_i . A Y address buffer Y-ADB forms internal complementary address signals $a_{i+1}, \overline{a_{i+1}}$ to $a_j, \overline{a_j}$
10 by receiving external address signals through the terminals A_{i+1} to A_j .

A row address decoder R-DCR forms the word line select signals of the memory array M-ARY by receiving the complementary address signals $a_0, \overline{a_0}$
15 to $a_i, \overline{a_i}$. The word line select signals are transmitted to the memory array M-ARY in synchronism with a timing pulse ϕ_X .

A column address decoder C-DCR forms data line select signals to be supplied to the memory
20 array M-ARY by receiving the complementary address signals $a_{i+1}, \overline{a_{i+1}}$ to $a_j, \overline{a_j}$.

The data line select signals are transmitted to the column switch C-SW in synchronism with a timing pulse ϕ_Y .

25 A precharge circuit PC_2 , for precharging the common data lines, is constructed of a MOSFET

that short-circuits the common complementary data lines by receiving a precharge pulse ϕ_{pc2} .

A main amplifier MA has a circuit arrangement similar to that of the sense amplifier SA. That is, the main amplifier MA is constructed of a CMOS FET latch circuit, and a power switch MOSFETs which are respectively located on the supply voltage V_{CC} side of the latch circuit and the earth potential V_{SS} side of the circuitry. A pair of input and output nodes of the CMOS FET latch circuit are respectively coupled to the pair of common complementary data lines. The respective power switch MOSFETs have their conductance controlled by timing signals $\overline{\phi_{ma1}}$, $\overline{\phi_{ma2}}$ and ϕ_{ma1} , ϕ_{ma2} .

A data output buffer DOB responds to a timing signal $\overline{\phi_{RW}}$ to supply the external terminal I/O with data corresponding to read data fed from the main amplifier MA. During a writing operation, the data output buffer DOB is held in its non-operating state by the timing signal $\overline{\phi_{RW}}$. In addition, a timing signal ϕ_{HZ} renders the output of the DOB a high impedance during a reading operation. This timing signal ϕ_{HZ} is principally used for performing a refresh operation. The memory array M-ARY is so constructed that, when the address signals are changed during the reading operation, the refresh operation is responsively executed. With the arrangement wherein the output of the data output buffer DOB is brought into the high impedance state by the timing

signal ϕ_{HZ} , wired OR logic can be simply formed among the outputs of a plurality of semiconductor memories.

A data input buffer DIB responds to a timing signal ϕ_{RW} to supply the common data lines with write data fed to the terminal I/O. During the reading mode, the data input buffer DIB is held in its non-operating state by the timing signal ϕ_{RW} .

The various timing signals referred to above are formed by circuit blocks to be described below.

10 An edge trigger circuit EGT_X (address transient detector) detects the rising or falling edges of the address signals by receiving the internal address signals a_0 to a_i (or $\overline{a_0}$ to $\overline{a_i}$).

15 An edge trigger circuit EGT_Y (address transient detector) detects the rising or falling edges of the address signals by receiving the internal address signals a_{i+1} to a_j (or $\overline{a_{i+1}}$ to $\overline{a_j}$).

Each of the edge trigger circuits EGT_X and EGT_Y is constructed of exclusive OR circuits which receive the internal address signals a_0 to a_i and a_{i+1} to a_j and the delay signals thereof respectively, and an OR circuit which receives the outputs of the exclusive OR circuits, as will be described later. When the level of at least one of the internal address signals a_0 to a_i and a_{i+1} to a_j has changed, the edge trigger circuits EGT_X and EGT_Y form edge detection pulses ϕ_{EX} and ϕ_{EY} synchronous with the timing of the change, respectively.

Since the edge detection pulse ϕ_{EX} indicating the transient of the row address signals and the edge detection pulse ϕ_{EY} indicating the transient of the column address signals are clearly distinguished, it is possible to generate the timing signals which ought to respond to the transient of the row address signals and those which ought to respond to the transient of the column address signals.

A timing generator circuit TG forms the various timing signals referred to above. The timing generator circuit TG forms the series of timing pulses by receiving a write enable signal $\overline{WE}$ and a chip select signal $\overline{CS}$ from the corresponding external terminals, besides the edge detection pulses ϕ_{EX} and ϕ_{EY} .

Referring now to Figures 2A and 2B, each of P-channel MOSFETs and each of N-channel MOSFETs are shown by symbols which are different from each other. The symbol representative of the P-channel MOSFET such as a MOSFET Q_7 has one straight line added across the drain and source thereof, in order to distinguish it from the N-channel MOSFETs such as a MOSFET Q_6 . The P-channel MOSFETs and N-channel MOSFETs are of the enhancement mode.

The memory array M-ARY consists of a plurality of memory columns and a plurality of word lines W_1 to W_S . The respective memory columns are identical in arrangement to one another. Accordingly, only one memory

column is illustrated in detail in Figure 2A. As shown, each memory column is constructed of one pair of complementary data lines D , $\bar{D}$, and memory cells which are arranged at a predetermined regularity and the input and output nodes of which are respectively coupled to either of the pair of complementary data lines D and $\bar{D}$. The memory cells are identical in arrangement to one another. One memory cell is constructed of, for example, a switching MOSFET Q_{15} and a MOS capacitor C coupled thereto. The gate of the switching MOSFET in one memory cell is used as a terminal for selecting the particular memory cell. The selecting terminals of the respective memory cells are coupled to the corresponding word lines.

The precharge circuit PC_1 is constituted by a switching MOSFET whose source - drain path is coupled between the complementary data lines D and $\bar{D}$, such as a MOSFET Q_{14} illustrated.

As shown the sense amplifier SA is constituted by a CMOS (complementary MOS) FET latch circuit which is composed of P-channel MOSFETs Q_7 , Q_9 and N-channel MOSFETs Q_6 , Q_8 . One pair of input and output nodes of the CMOS FET latch circuit are coupled to the complementary data lines D and $\bar{D}$. The latch circuit is fed with the supply voltage V_{CC} through P-channel MOSFETs Q_{12} , Q_{13} in a parallel connection and with the earth potential voltage V_{SS} of the circuitry through N-channel MOSFETs Q_{10} , Q_{11} in a parallel connection. These power switch MOSFETs Q_{10} , Q_{11} and MOSFETs Q_{12} ,

Q_{13} are used in common for the latch circuits (not shown) arranged in other similar memory columns.

The timing signals ϕ_{pa1} , $\overline{\phi_{pa1}}$ for activating the sense amplifier SA are applied to the gates of the MOSFETs Q_{10} , Q_{12} , while the timing signals ϕ_{pa2} , $\overline{\phi_{pa2}}$ delayed with respect to the timing signals ϕ_{pa1} , $\overline{\phi_{pa1}}$ are applied to the gates of the MOSFETs Q_{11} , Q_{13} . The timing signals ϕ_{pa1} and $\overline{\phi_{pa1}}$ are changed complementarily to each other so as to bring the power switch MOSFETs Q_{10} and Q_{12} into the "on" or "off" states at the same time. Likewise, the timing signals ϕ_{pa2} and $\overline{\phi_{pa2}}$ are changed complementarily to each other so as to bring the power switch MOSFETs Q_{11} and Q_{13} into the "on" or "off" states at the same time. That is, the timing signal $\overline{\phi_{pa1}}$, for example, is a phase-inverted timing signal relative to the timing signal ϕ_{pa1} .

Each of the power switch MCSFETs Q_{10} and Q_{12} is endowed with a comparatively low conductance. In contrast, each of the MCSFETs Q_{11} and Q_{13} is endowed with a comparatively high conductance.

5 Accordingly, the respective latch circuits constituting the sense amplifier SA are activated comparatively weakly by the timing signals ϕ_{pal} and $\overline{\phi_{pal}}$, and they are subsequently activated intensely by the timing signals ϕ_{pa2} and $\overline{\phi_{pa2}}$. Since,
10 the sense amplifier SA is activated in two divided stages, the large drop in the high level potential of the complementary data lines which is otherwise brought about by the starting of the operation of the sense amplifier can be prevented, and fast read-out of data can be executed.

15 More specifically, in the case where a minute read-out voltage from the memory cell is amplified by the sense amplifier SA, the MOSFETs Q_{10} , Q_{12} of comparatively low conductance are first brought into the "on" states by the timing signals ϕ_{pal} , $\overline{\phi_{pal}}$. The sense amplifier
20 SA responsively begins to amplify the potential difference between the complementary data lines. Since the potential difference between the complementary data lines is small in the initial period of the amplifying operation, the MOSFETs Q_6 and Q_8 constituting the sense amplifier SA
25 are both held in the conductive states. For this

reason, charges having previously been held in the data line on the high level side are transiently discharged through one side of the MOSFETs constituting the sense amplifier SA and the power switch MOSFET. Therefore,

5 the potential on the high level side drops. However, since the conductances of the power switch MOSFETs

Q_{10} , Q_{12} which are first brought into the conductive states by the timing signals ϕ_{pa1} and $\overline{\phi_{pa1}}$ are set at a comparatively small value in advance, the quantity

10 of the charges in the high level side data line to be undesirably discharged at this time can be limited to a small value, and the large drop of the high level side potential can be prevented. When the potential difference between the complementary data lines has become sufficiently

15 large, the switching MOSFETs Q_{11} , Q_{13} of comparatively high conductance are brought into the "on" states by the timing signals ϕ_{pa2} , $\overline{\phi_{pa2}}$, whereby the amplifying operation of the sense amplifier SA is rendered fast.

Accordingly, the fast read-out can be effected while

20 the drop of the potential of the high level side of the complementary data lines is prevented, by carrying out the amplifying operation of the sense amplifier SA in the two divided stages in this manner.

The row decoder R-DCR is constructed of a plurality of
25 unit circuits. In Figure 2A, one unit circuit (corresponding

to four word lines) constituting the row decoder R-DCR is shown. The row decoder R-DCR includes a NAND circuit ND of CMOS circuit arrangement which is composed of N-channel MOSFETs Q_{32} to Q_{36} and
 5 P-channel MOSFETs Q_{37} to Q_{41} which receive the internal address signals a_2 to a_6 . Accordingly, four word line select signals for selecting the word lines W_0 to W_3 are formed by the NAND circuit ND.

The output of the NAND circuit ND is inverted by
 10 a CMOS inverter IV_1 , and the inverted signal is transmitted through cut MOSFETs Q_{28} - Q_{31} to the gates of MOSFETs Q_{24} - Q_{27} which constitute a transfer gate circuit TRF.

The sources of the respective MOSFETs Q_{24} to Q_{27} are supplied with word line select timing signals ϕ_{X00}
 15 to ϕ_{X11} . These word line select timing signals ϕ_{X00} to ϕ_{X11} are formed by a circuit (not shown) which constitutes a part of the row decoder R-DCR. The levels of the respective word line select timing signals ϕ_{X00} to ϕ_{X11} are determined by the combinations of the timing pulse
 20 ϕ_X with decode signals formed by decoding the address signals a_0 , a_1 of two bits.

The
 word line select timing signal ϕ_{X00} is brought to its high level in response to the change of the timing pulse
 25 ϕ_X to the high level (logic "1") when both the address

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signals a_0 and a_1 are at the low level (logic "0"). The signal ϕ_{X01} is brought to its high level in synchronism with the timing pulse ϕ_X when the address signal a_0 is at the high level and the signal a_1 is at the low level. Similarly, the signals ϕ_{X10} and ϕ_{X11} are brought to their high level in accordance with the address signals a_0 and a_1 and the timing pulse ϕ_X .

Accordingly, the unit circuit constituting the row decoder R-DCR brings one of the word lines $W_1 - W_4$ to its high level (selected level) in synchronism with the timing pulse ϕ_X when the output of the NAND circuit ND has been rendered to the low level in accordance with the address signals $a_2 - a_6$.

The word line select timing signals $\phi_{X00} - \phi_{X11}$ are also fed to the unit circuits (not shown) constituting the row decoder R-DCR.

In addition, MOSFETs Q_{20} to Q_{23} whose gates are supplied with the output of the NAND circuit are interposed between the respective word lines and earth potential. When the combination of the address signals $a_2 - a_6$ does not indicate one set of word lines ($W_1 - W_4$), that is, when the output of the NAND circuit ND is at the high level, the MOSFETs $Q_{20} - Q_{23}$ are responsively brought into the "on" states. As a result, the word lines $W_1 - W_4$ are held at earth potential by the MOSFETs $Q_{20} - Q_{23}$.

when they are unselected. In this respect, the MOSFETs
5 which are controlled by the output of the NAND circuit are
arranged between the word lines and earth potential

of the circuitry in order that, when the desired
word line in one set of word lines is to be rendered
the selected level, the remaining undesired word lines
10 may be prevented from becoming the selected level.

Resetting MOSFETs Q_1 to Q_5 whose gates are supplied
with a reset pulse ϕ_{pw} are interposed between the
respective word lines and earth. The
word line selected in a preceding operation cycle, e. g.,
15 a read cycle is reset to the earth level for the next
operation cycle in such a way that these MOSFETs Q_1 to Q_5
turn "on" by receiving the reset pulse ϕ_{pw} .

The column switch C-SW is constructed of MOSFETs
which are interposed between the complementary data
20 lines D, $\bar{D}$ and the common complementary data lines CD, $\bar{CD}$,
such as MOSFETs Q_{42} and Q_{43} shown in Figure 2B.

The gates of the MOSFETs Q_{42} and Q_{43} are supplied with
a select signal from the column decoder C-DCR.

A precharge MOSFET Q_{44} which constitutes the precharge
25 circuit PC2 is interposed between the common complementary
data lines CD and $\bar{CD}$.

One pair of input and output nodes of the main
amplifier MA having a circuit arrangement similar to

that of the sense amplifier SA are coupled to the common complementary data lines CD and $\overline{CD}$.

Further, the complementary output nodes of the data input buffer DIB are coupled to the common data
5 lines CD and $\overline{CD}$.

As shown in Figure 2B, the edge trigger circuit EGT_X (EGT_Y) is constituted by the exclusive OR circuits $EX_0 - EX_i$ which receive the internal address signals $a_0 - a_i$ ($a_{i+1} - a_j$) and the delayed signals of these
10 internal address signals formed through delay circuits $D_0 - D_i$, and the OR circuit which receives the output signals of the exclusive OR circuits $EX_0 - EX_i$.

Next, the operations of the above described circuit will be described with reference to the waveform diagram
15 shown in Figure 3.

The timing signals $\overline{\phi_{pa1}}$ and $\overline{\phi_{pa2}}$ are opposite in phase to those ϕ_{pa1} and ϕ_{pa2} as described before. In Figure 3, the timing signals $\overline{\phi_{pa1}}$, $\overline{\phi_{pa2}}$ and $\overline{\phi_{ma1}}$, $\overline{\phi_{ma2}}$ are omitted for the sake of clarity.

20 Now, when any address signal a_n falls from the high level to the low level as shown in waveform A of Figure 3, the delayed signal a_n' thereof falls with a delay. Accordingly, the edge detection pulse ϕ_{EX} (ϕ_{EY}) which is held at the high level ("1") from
25 the beginning of the change of the address signal a_n

until the generation of the delayed signal a_n' is outputted from the edge trigger circuit EGT_X (EGT_Y).

Upon receiving the pulse ϕ_{XE} (ϕ_{EY}), the timing generator TG forms therein a reset pulse ϕ_{RS} as shown in waveform D of Figure 3. This reset pulse ϕ_{RS} resets the operating states of the respective circuits which have been determined in the preceding operation cycle, for example, read operation cycle.

By way of example, the word lines are reset by the word line reset pulse ϕ_{PW} (not shown in Figure 3) formed on the basis of the reset pulse ϕ_{RS} . Likewise, the word line select timing signal ϕ_X , the timing signals ϕ_{pal} , ϕ_{pa2} of the sense amplifier SA, the data line select timing signal ϕ_Y , and the timing signals ϕ_{ma1} , ϕ_{ma2} of the main amplifier MA as shown by waveforms E, H, I and J in Figure 3 are brought into their reset states (reset levels) by the reset pulse ϕ_{RS} . By way of example, the timing signals ϕ_X , ϕ_{pal} , ϕ_{pa2} , ϕ_Y , ϕ_{ma1} and ϕ_{ma2} are brought to the low level.

At the same time that the timing signals ϕ_{pal} , ϕ_{pa2} and ϕ_{ma1} , ϕ_{ma2} are brought to the low level, the timing signals $\overline{\phi_{pal}}$, $\overline{\phi_{pa2}}$ and $\overline{\phi_{ma1}}$, $\overline{\phi_{ma2}}$ lying in the complementary relationship to the former signals are respectively brought to the high level. In consequence, the sense amplifier SA and main amplifier MA are respectively brought

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into their inactive states, and the complementary data lines D , $\bar{D}$ and the common complementary data lines CD , $\overline{CD}$ are brought into their floating states.

Parasitic capacitances (not shown) are coupled
5 to the respective complementary data lines D , $\bar{D}$ and common complementary data lines CD , $\overline{CD}$. In the parasitic capacitances, charges corresponding to the potentials of the respectively associated data lines have been stored in the preceding operation cycle. By way of example, there
10 will be studied the parasitic capacitance (not shown) coupled to the complementary data line D and the parasitic capacitance (not shown) coupled to the complementary data line $\bar{D}$. In the case where the complementary data line D was at the high level (V_{CC}) and the data line $\bar{D}$ at the
15 low level (0 V) in the preceding operation cycle by way of example, the parasitic capacitance of the data line D has stored charges corresponding to the high level (V_{CC}), and that of the data line $\bar{D}$ has stored charges corresponding to the low level (0 V). The respective
20 parasitic capacitances of the common complementary data lines CD , $\overline{CD}$ are similarly rendered to the high or low level.

The complementary data lines D , $\bar{D}$ and common complementary data lines CD , $\overline{CD}$ which have the parasitic capacitances
25 storing the charges determined in the preceding operation

cycle in this manner are brought into the floating states as described above, so that the parasitic capacitances coupled to the complementary data lines D , $\bar{D}$ and common complementary data lines CD , $\overline{CD}$ hold the charges determined in the preceding cycle of operation. Accordingly, the respective potentials of the complementary data lines D , $\bar{D}$ and common complementary data lines CD , $\overline{CD}$ are also held at their values in the preceding cycle of operation. In the case where the predetermined charges have been respectively stored in the parasitic capacitance of the complementary data line D and that of the complementary data line $\bar{D}$ in the preceding cycle of operation as in the above example, the parasitic capacitance in the complementary data line D put into the floating state as described above holds the charges corresponding to the high level (V_{CC}), and that in the complementary data line $\bar{D}$ similarly put into the floating state holds the charges corresponding to the low level (0 V). Therefore, the potential of the complementary data line D put into the floating state holds the high level (V_{CC}), whilst that of the complementary data line $\bar{D}$ holds the low level (0 V). This also applies to the common complementary data lines CD , $\overline{CD}$.

As a result of the de-energization of the sense amplifier SA and main amplifier MA, the complementary

data lines D , $\bar{D}$ and common complementary data lines CD , $\bar{CD}$ hold the high level (V_{CC}) and low level (0 V) in the floating states.

At the time at which the word lines have been
5 reset, the precharge pulses ϕ_{pc1} and ϕ_{pc2} are generated.

Since the precharge MOSFETs Q_{14} and Q_{44} are turned "on" by the generation of the precharge pulses ϕ_{pc1} and ϕ_{pc2} , the complementary data lines D and $\bar{D}$ and the common complementary data lines CD and $\bar{CD}$ are respectively
10 short-circuited therebetween. As a result, the charges disperse between the complementary data lines D and $\bar{D}$ and between the common complementary data lines CD and $\bar{CD}$, so that the complementary data lines D , $\bar{D}$ and the common complementary data lines CD , $\bar{CD}$ are precharged
15 to an intermediate level of about $V_{CC}/2$.

Subsequently, when the reset pulse ϕ_{RS} falls to the low level, the reset status is released. The precharge operation ends upon the release of the reset status.

After the end of the precharge of the complementary
20 data lines D , $\bar{D}$ by the precharge signal ϕ_{pc1} , the word line select timing signal ϕ_x rises to the high level as illustrated in waveform E of Figure 3. Thus, the high level signal outputted from the row decoder R-DCR is applied to one word line which is to be determined by the address
25 signals $A_0 - A_i$. The word line determined by the address

signals $A_0 - A_i$ is selected, and is brought to the select level of the memory cell. The switching MCSFET constituting the memory cell is brought into the "on" state by the high level potential of the selected word line.

- 5 Charge dispersion occurs between the storage capacitor of the selected memory cell and the parasitic capacitance of one data line, e. g., data line $\bar{D}$, to which the memory cell is coupled. The level of the data line $\bar{D}$ is changed to a level which corresponds to charges stored in the memory
- 10 capacitor of the memory cell, in other words, data stored in the memory cell. Since, in this case, the memory cell coupled to the other data line D is not selected, this data line D holds the precharge level $V_{CC}/2$. As a result, a minute potential difference corresponding
- 15 to the held data in the selected memory cell develops between the data lines D and $\bar{D}$. The minute potential difference between the data lines D and $\bar{D}$ arises as follows. In the case where charges corresponding to, e. g., V_{CC} have been stored in the storage capacitor
- 20 of the memory cell coupled to the data line $\bar{D}$, the potential of the data line $\bar{D}$ becomes higher than the potential ($V_{CC}/2$) of the data line D . In contrast, in the case where charges corresponding to, e. g., 0 V have been stored in the storage capacitor of the memory cell, in
- 25 other words, in the case where no charge has been stored

in the storage capacitor, the potential of the data line $\bar{D}$ becomes lower than the potential ($V_{CC}/2$) of the data line D.

When the sense amplifier is activated, the minute
5 potential difference between the data lines $\bar{D}$ and D is thereby amplified. That is, upon the subsequent change of the timing signal ϕ_{pa1} to the high level (the timing signal $\overline{\phi_{pa1}}$ to the low level), the sense amplifier SA is activated, and an amplifying operation which enlarges
10 the potential difference between the complementary data lines D and $\bar{D}$ is started by the sense amplifier SA. Subsequently, the timing signal ϕ_{pa2} is rendered the high level (the timing signal $\overline{\phi_{pa2}}$ the low level). Thus, the gain of the sense amplifier SA is increased, and
15 the potential difference between the complementary data lines D and $\bar{D}$ is further increased.

Next, at the same time that the data line select timing signal ϕ_Y is brought to the high level, the precharge signal ϕ_{pc2} is set at the low level.

20 Owing to the change of the precharge signal ϕ_{pc2} to the low level, the MOSFET Q_{44} is brought into the "off" state, with the result that the precharge of the common complementary data lines CD, $\bar{CD}$ ends.

When the data line select timing signal ϕ_Y is set at
25 the high level, column select signals for coupling to

the common data lines CD , $\overline{CD}$ one pair of complementary data lines D , $\overline{D}$ which are to be determined by the address signals $A_{i+1} - A_j$ are supplied from the column decoder C-DCR to the column switch CSW. Therefore, one pair
5 of complementary data lines D , $\overline{D}$ to be selected by the column select signals are coupled to the common complementary data lines CD , $\overline{CD}$ through the column switch CSW.

With a timing relationship in which, about the time when the complementary data lines D , $\overline{D}$ are coupled
10 to the common complementary data lines CD , $\overline{CD}$, the precharge of the common complementary data lines CD , $\overline{CD}$ is completed by the precharge signal ϕ_{pc2} ; the potentials of the common data lines CD , $\overline{CD}$ can be equalized to each other even when noise has acted on the common data lines
15 before the coupling between the common data lines and the data lines. For this reason, the potential difference between the selected data lines D , $\overline{D}$ is accurately transmitted to the common data lines CD , $\overline{CD}$, so that this semiconductor memory can be rendered immune against noise.

20 Also the common complementary data lines CD , $\overline{CD}$ are precharged to $V_{CC}/2$ by the precharging operation of the precharge MOSFET Q_{44} as described before. The potential of the common data line $\overline{CD}$ is therefore determined by the charge dispersion of the charges stored in the
25 parasitic capacitance of the common data line $\overline{CD}$ (charges

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corresponding to $V_{CC}/2$) and charges stored in the parasitic capacitance of the data line $\bar{D}$ selected and coupled to this common data line $\overline{CD}$. Likewise, the potential of the common data line CD is determined by the charge dispersion of the charges stored in the parasitic capacitance of the common data line CD (charges corresponding to $V_{CC}/2$) and charges stored in the parasitic capacitance of the data line D selected and coupled to the common data line CD.

10 When the complementary data lines D, $\bar{D}$ are coupled to the common complementary data lines CD, $\overline{CD}$, the potential of the common data line CD which is determined by the charge dispersion of the charges of the parasitic capacitance of the data line D and those of the parasitic capacitance of the common data line CD becomes higher (lower) than the potential of the common data line $\overline{CD}$ which is determined by the charge dispersion of the charges of the parasitic capacitance of the data line $\bar{D}$ and those of the parasitic capacitance of the common data line $\overline{CD}$.

20 Waveform G shown in Figure 3 illustrates by solid lines the respective potential changes of the data lines, D, $\bar{D}$ and common data lines CD, $\overline{CD}$ in the case where the memory cell coupled to the data line D is selected and where the charges corresponding to V_{CC} are stored in the storage capacitor of the selected memory cell (or the case where

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the memory cell coupled to the data line $\bar{D}$ is selected and where the charges corresponding to 0 V are stored in the storage capacitor of the memory cell).

The potential difference between the common data lines CD and $\bar{CD}$ is amplified by the main amplifier. More specifically, when the timing signals ϕ_{ma1} , ϕ_{ma2} are subsequently set at the high level and the timing signals $\overline{\phi_{ma1}}$, $\overline{\phi_{ma2}}$ the low level, the main amplifier MA is operated in response to these changes, and the potential difference between the common data lines CD and $\bar{CD}$ is amplified.

In the reading operation, the potential difference amplified by the main amplifier MA is supplied to the data output buffer DOB. The data output buffer DOB transmits an output signal corresponding to the input signal, to the terminal I/O.

In the writing operation, write data is transmitted to the common data lines CD, $\bar{CD}$ through the data input buffer DIB. The levels of the data lines D, $\bar{D}$ are determined in accordance with the write data supplied to the common data lines CD, $\bar{CD}$. As a result, the write data is transmitted to the selected memory cell.

In order to apply a voltage of at least the supply voltage $V_{CC} + V_{th}$ (the threshold voltage of the switching MOSFET)

to the gate of the switching MOSFET of the memory cell in writing data into the memory cell, the word line select timing signal ϕ_x is brought to a high level of at least the supply voltage $V_{CC} + V_{th}$ by a bootstrap circuit (not shown). Thus, the high level (V_{CC}) of the data line as it is can be transmitted to the MOS capacitor of the memory cell without any level loss, and charges to be stored in the MOS capacitor can be increased.

Also in refreshing the memory cell, the word line select timing signal ϕ_x is brought to the high level of at least the supply voltage $V_{CC} + V_{th}$ by the bootstrap circuit (not shown). Thus, the high level (V_{CC}) of the data line kept intact is rewritten without any level loss into the MOS capacitor of the memory cell having held the high level.

In the reading operation, the potentials of the selected complementary data lines are amplified to the high level (V_{CC}) and low level (0 V) by the sense amplifier SA, and the potentials of the common complementary data lines are similarly amplified to the high level (V_{CC}) and low level (0 V) by the main amplifier MA. Also the potentials of the unselected complementary data lines are amplified to the high level (V_{CC}) and low level (0 V) by the sense amplifiers SA of the corresponding columns.

By way of example, as indicated by the solid lines in waveform G of Figure 3, the selected data line D and common data line CD are respectively amplified to the high level (V_{CC}) by the sense amplifier SA and main amplifier MA, while the selected data line $\bar{D}$ and common data line $\bar{CD}$ are respectively amplified to the low level (0 V) by the sense amplifier and main amplifier. In addition, as indicated by dotted lines in waveform G of Figure 3, the unselected one of the complementary data lines is amplified to the high level (V_{CC}), and the remaining complementary data line to the low level (0 V) by the sense amplifier.

The potentials of the data lines set at the high level or low level in this manner are transmitted to the MOS capacitor of the memory cell in the refresh operation described above.

Also in the writing operation, in accordance with data to be written, the potentials of the common data lines and the data lines are respectively set at the high level (V_{CC}) or low level (0 V) by the data input buffer DIB and sense amplifier SA. By way of example, in accordance with the data to be written, the potentials of the common data line CD and data line D are brought to the high level (V_{CC}), and those of the common data line $\bar{CD}$ and data line $\bar{D}$ to the low level (0 V).

In this manner, in any operation, the potentials

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of the data lines D , $\bar{D}$ are respectively set at the high level (V_{CC}) or low level (0 V), and also the potentials of the common data lines CD , $\bar{CD}$ are respectively set at the high level (V_{CC}) or low level (0 V). In consequence, changes corresponding to the high level and those corresponding to the low level are stored in the respective capacitances of the data lines D and $\bar{D}$. Likewise, charges corresponding to the high level and those corresponding to the low level are stored in the respective capacitances of the common data lines CD and $\bar{CD}$. That is, when the charges corresponding to the high level (V_{CC} level) are stored in the capacitance of one data line (common data line), the charges corresponding to the low level (0 V level) are stored in the capacitance of the other data line (common data line).

The charges stored in the respective capacitances of the data lines D , $\bar{D}$ and common data lines CD , $\bar{CD}$ in this manner are used for the precharge of the data lines D , $\bar{D}$ and the precharge of the common data lines CD , $\bar{CD}$ as described above. That is, the charges are used for precharging the data lines and common data lines in the next operation.

In the case of writing logic "1" into the memory cell coupled to one data line D of the complementary data lines, charges corresponding to, e.g.,

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the supply voltage V_{CC} are stored in the storage capacitor of the memory cell. In contrast, in the case of similarly writing logic "1" into the memory cell coupled to the other data line $\bar{D}$, charges corresponding to earth potential (0 V) of the circuitry are stored in the memory cell. In addition, in the case of writing logic "0" into the memory cell coupled to one data line D, charges corresponding to earth potential (0 V) are stored in the storage capacitor of the memory cell, and in the case of writing logic "0" into the memory cell coupled to the other data line $\bar{D}$, charges corresponding to the supply voltage V_{CC} are stored in the storage capacitor of the memory cell. As illustrated,

when the potential of the I/O terminal is at the high level (logic "1"), the data input buffer DIB brings the common data line CD to the high level (V_{CC}) and the common data line $\bar{CD}$ to the low level (0 V)

Conversely, when the potential of the I/O terminal is at the low level (logic "0"), the data input buffer DIB brings the common data line CD to the low level (0 V) and the common data line $\bar{CD}$ to the high level (V_{CC}). The

main amplifier MA amplifies the level of one common data line CD and then transmits it to the node CDI of the output buffer DCB, and it amplifies the level of

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the other common data line $\overline{CD}$ and then transmits it to the other node $\overline{CDI}$ of the output buffer DOB.

The output buffer DOB is arranged so that when the level of the node CDI is higher

5 than the level of the node $\overline{CDI}$, it supplies an output signal of high level (logic "1") to the terminal I/O, whereas when the level of the node CDI is lower than the level of the node $\overline{CDI}$, it supplies an output signal of low level (logic "0") to the terminal I/O.

10 According to this arrangement, the complementary signals delivered from the main amplifier MA are supplied to the data output buffer DOB. However, the arrangement shown in Figure 2B, may well be replaced with an arrangement wherein only one of the complementary signals
15 delivered from the main amplifier MA is supplied to the data output buffer DOB. In this case, the data output buffer DOB can have, for example, an arrangement which compares a certain reference voltage (for example, the logic threshold voltage of the DOB) and the level
20 of the signal from the main amplifier MA and which supplies the I/O terminal with an output signal conformed to the result of the comparison.

The timing generator circuit TG is so arranged as to provide the precharge signal ϕ_{pc2} , timing signal
25 ϕ_y , main amplifier control signals ϕ_{ma1} , ϕ_{ma2}

on the basis of, not only the detection signal ϕ_{EX} from the edge trigger circuit EGT_X , but also the detection signal ϕ_{EY} from the edge trigger circuit EGT_Y directed toward the column-group address signals. Thus, it becomes possible to successively read out data amplified by the sense amplifiers in advance.

That is, when the column-group address signals $A_{i+1} - A_j$ are successively changed after supplying one set of row-group address signals $A_0 - A_i$ to the memory, the data can be read out from the corresponding addresses.

The detection signals ϕ_{EX} and ϕ_{EY} may well be caused to correspond respectively to a row address strobe signal and a column address strobe signal which are supplied to a memory of the known address multiplexing system. Accordingly, the logic construction of the timing generator circuit for forming the various timing signals mentioned above may well be similar to that of a timing generator circuit in the known memory.

The above described embodiment is provided with a substrate bias voltage generator circuit V_{BB} -G in order to obtain a fast operation of the memory.

Furthermore, the above described embodiment is so arranged that, with a view to reducing the power consumption, the main amplifier MA is prevented

from operating during the writing operation.

In the semiconductor memory of this embodiment, the precharge is executed by utilizing the edge of the address signal. The semiconductor memory can therefore
5 be handled similarly to the conventional MOS static type RAM, except that any timing signal to be externally supplied to the memory is dispensed with and that the refresh operation is required. Accordingly, the external timing control can be simplified.

10 As the constituent memory cell, it is possible to use a memory cell of the type which is used in the dynamic type RAM, for example, a memory cell of comparatively small occupying area which is constructed of a single switching MOSFET and a single storage capacitor as stated
15 before. In consequence, the operation control can be assimilated to that of the static type RAM, and the memory capacity can be rendered large.

The precharge operation is such that one pair of complementary data lines and common complementary data
20 lines are merely short-circuited, in order to bring them to the intermediate level (about $V_{CC}/2$) below the V_{CC} level. This precharge operation can be executed at high speed because the magnitude of the level change can be rendered smaller than in the precharge of the
25 conventional dynamic type RAM in which data lines are

charged up from 0 V to the V_{CC} level. Since the precharge level is the intermediate level below the V_{CC} level as stated above, the precharge MOSFETs satisfactorily fall into "on" states even when the gate voltage thereof is set at the ordinary logic level (V_{CC}). Thus, a satisfactory precharge level can be formed. In contrast, in the case of precharging the data lines to the V_{CC} level as in the prior art, a high bootstrap voltage above the V_{CC} level needs to be applied to the gate of a precharge MOSFET in order to sufficiently raise the precharge level. As a result, the circuit becomes complicated, and the operation thereof becomes slow due to the complicated circuit. In the above described embodiment, the precharge level is formed by the charge dispersion of the complementary data lines, and hence, no current is dissipated at the precharge. Therefore, the power consumption can be reduced.

Since the precharge level is the intermediate level of about $V_{CC}/2$, the switching MOSFET in the memory cell falls into the "on" state favorably in reading out data from the memory cell even when its gate voltage (word line potential) is the ordinary logic high level (V_{CC}). The switching MOSFET in the memory cell turns "on" in an unsaturation region when its gate voltage becomes at least $\frac{1}{2} V_{CC} + V_{th}$. As a result, all

charges in the MCS capacitor can be read out even when the bootstrap voltage is not used as in the conventional dyanmic type RAM. Accordingly, fast read-out and high reliability can be realized.

5 Since dummy memory cells as in the conventional dynamic type RAM are not provided, the above described embodiment can reduce the chip size by the part of the dummy memory cells and a part corresponding to a dummy word line selector circuit. Further, since the read-out reference
10 voltage to be referred to by the sense amplifier SA is formed of the equal precharge levels of the complementary data lines D , $\bar{D}$ immediately before the read-out, it follows up the fluctuation of the supply voltage V_{CC} .

Moreover, the read-out reference voltage is, in
15 effect, free from influence by the dispersion of elements in the memory cells and such dummy memory cells. As a result, the operating margin of the circuit can be greatly enhanced.

Furthermore, in the case where peripheral circuits including
20 the sense amplifier SA are constructed of CMOS circuits, a reduced power consumption can be attained.

The sense amplifier SA and the main
amplifier MA are preferably constructed of CMOS
circuits. More specifically, when the sense amplifier
25 SA and main amplifier MA are respectively constructed

of the CMOS circuits which are composed of P-channel MOSFETs and N-channel MOSFETs, it is possible, without providing a special circuit such as active restore circuit, to amplify the potentials of the complementary data lines D, $\bar{D}$ to the supply voltage (V_{CC}) and earth potential (0 V) of the circuitry respectively and also to amplify the potentials of the common complementary data lines CD, $\bar{CD}$ to the supply voltage (V_{CC}) and earth potential (0 V) of the circuitry respectively.

5 Therefore, the potential difference between the data lines D, $\bar{D}$ and that between the common data lines CD, $\bar{CD}$ at the reading operation, writing operation or refresh operation can be rendered great with a simple circuit, so that malfunctions can be reduced. Cwing to the provision

10 of such sense amplifier, charges corresponding to the supply voltage (V_{CC}) and those corresponding to earth potential (0 V) can be stored in the respective parasitic capacitances of the data lines D, $\bar{D}$ before the precharge operation is started, so that the precharge

15 levels of the data lines D, $\bar{D}$ can be brought to about $V_{CC}/2$ by the execution of the precharge operation. This also applies to the common complementary data lines CD, $\bar{CD}$.

The address buffers X-ADB, Y-ADB, the edge trigger

25 circuits EGT_X , EGT_Y and the timing generator circuit TG

described above are preferably constructed of static type circuits so that the output signals may be formed whenever the respective input signals change.

- The peripheral circuits of the sense amplifier
- 5 SA, may alternatively be constructed of MOSFETs of either one channel type; P-channel MOSFETs or N-channel MOSFETs in order to reduce the chip area. However, in the case of constructing, e. g., the sense amplifier SA out of only the single-channel MOSFETs, it is necessary
- 10 to add a special circuit for normally keeping the potentials of the respective data lines D , $\bar{D}$ at the high level (V_{CC}) and the low level (0 V). As the special circuit, it is desirable to use the so-called active restore circuit which is a kind of bootstrap circuit.
- 15 One-side data lines in the M-ARY may well be constructed as dummy data lines.

The respective complementary data lines D , $\bar{D}$ may have dummy cells coupled thereto as well. In this case, the circuit is so arranged that when the memory cell

20 coupled to one complementary data line is selected, the dummy cell coupled to the other complementary data line is selected. Thus, the potential change of the word line is transmitted to the one data line through the

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undesired capacitance of the switching MOSFET of the selected memory cell (the overlap capacitance between the gate electrode of the FET and the one data line), while at the same time the potential change of a word line for the dummy cell is transmitted to the other data line through the undesired capacitance of the switching MOSFET of the selected dummy cell. In this respect, a potential change afforded to a data line in response to the potential change of a word line is regarded as noise. However, potential changes simultaneously afforded to a pair of data lines are regarded as inphase noise. The sense amplifier is, in effect, insensitive to the inphase noise. Accordingly, the malfunctions of the circuit can be further reduced in spite of the undesired potential changes afforded to the pair of complementary data lines.

As the edge trigger circuit, it is also possible to employ an OR or AND gate which receives the complementary address signals a_0 , $\overline{a_0}$ and whose logic threshold voltage is biased to the high level or low level side.

The edge trigger circuit may well be one with which a plurality of bit data are read/written in parallel.

Further, the peripheral circuits can adopt various aspects of performance.

In addition, redundant memory arrays for saving

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defective bits and a switching circuit may be provided.

Furthermore, the auto-refresh function may well be included.



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CLAIMS.

1. A semiconductor memory including:

(a) a plurality of dynamic memory cells;

(b) a first selector circuit which receives first address signals, and which selects one of said plurality of dynamic memory cells specified by the first address signals, and the time of operation of which is controlled by a first timing signal;

(c) a plurality of pairs of data lines connected to said dynamic memory cells so that each pair of data lines is respectively provided with a potential difference in accordance with the data read out from a selected dynamic memory cell;

(d) a plurality of sense amplifiers each of which has a pair of input and output terminals that are coupled to a corresponding pair of data lines, the respective sense amplifiers having their operations controlled by second timing signals;

(e) a first precharge circuit which is coupled to said plurality of pairs of data lines and operates so as to precharge said data lines at a potential intermediate between binary signal levels to be stored in dynamic memory cells in accordance with a third timing signal;

(f) a first detector circuit including means connected to receive said first address signals for detecting level changes in the first address signals; and



(g) a timing generator circuit connected to receive the detection outputs of said first detector circuit, and including means for generating said third timing signal for operating said first precharge circuit, said first timing signal for operating said first selector circuit after stopping the operation of said first precharge circuit, and said second timing signals for operating said sense amplifiers.

2. A semiconductor memory according to claim 1, wherein said each dynamic memory cell comprises a MOSFET whose gate is used as a selecting terminal, and a charge holding capacitor which is coupled to said MOSFET.

3. A semiconductor memory according to claim 2, wherein said precharge circuit comprises MOSFETs each of which short-circuits the corresponding pair of data lines in response to the timing signal supplied from said timing generator circuit.

4. A semiconductor memory according to claim 3, wherein said each sense amplifier comprises a complementary MOSFET circuit.

5. A semiconductor memory according to claim 4, further including:

(h) a pair of common data lines;

(i) a second selector circuit which receives second address signals, in order to couple to said common data lines the pair of data lines specified by the second address signals among said plurality of pairs



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of data lines, and the time of operation of which is controlled by a fourth timing signal;

(j) a second precharge circuit which is coupled to said common data lines;

5 (k) a main amplifier which is coupled to said common data lines, and the time of operation of which is controlled by a fifth timing signal; and

(l) a second detector circuit which detects changes of the second address signals;

10 said timing generator circuit receiving outputs of said first and second detector circuits, in order to generate said timing signals for controlling operation timings of said second selector circuit, said precharge circuits and said main amplifier.

15 6. A semiconductor memory according to claim 5, wherein said main amplifier comprises a complementary MOSFET circuit.

7. A semiconductor memory according to claim 3, wherein said first detector circuit and said timing
20 generator circuit comprise static type complementary MOSFET circuits.

8. A semiconductor memory according to claim 3, wherein said each sense amplifier comprises a static type complementary MOSFET latch circuit, a first switching
25 MOSFET which is interposed between one power feed terminal of said latch circuit and a power source terminal, and a second switching MOSFET which is



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interposed between a remaining power feed terminal of said latch circuit and another power source terminal.

9. A semiconductor memory constructed and arranged to operate substantially as herein described with reference to and as illustrated in the accompanying drawings.
