Description

The present invention relates to apparatus for detecting arc-over conditions in the cathode-ray tube (CRT) of a television display and for reestablishing any digital data which may have been corrupted by the arc-over conditions.

Accelerating potential or ultor voltage for the electron beams within a CRT is generated by rectification of an alternating current voltage and coupling the rectified voltage to the ultor electrode of the CRT. The ultor electrode is coupled to an ultor inner conductive coating the the CRT envelope. The inner coating forms one plate of an ultor capacitor. An ultor outer conductive coating forms the other plate which serves as the ultor ground return terminal for ultor current.

The anode electrode of the electron gun is connected to the inner conductive coating, typically by means of spring contacts. The ultor accelerating potential serves as an energizing voltage for the anode electrode. Energizing voltages for the other electrodes, such as the screen, grid, and cathode electrodes, are developed by associated energizing circuitry external to the CRT. Connecting pins at the base of the CRT couple the energizing voltages to the associated electron gun electrodes.

One of the pins at the base of the CRT, for example, one of the filament pins, may serve as the ground return base pin for ultor current. This pin is connected both to ground and to the ultor outer conductive coating. Typical termination structure to the outer coating from the ground return base pin may comprise a U-shaped braid of copper wire closely pressed over the outer conductive coating on the CRT envelope. One or several copper wires connect various points along the copper braid to the ground return base pin. The ground return base pin is also connected by a copper wire to the common ground current return terminal of the energizing circuitry or to a chassis grounding terminal if the energizing circuitry and chassis have mutual ground current returns.

CRT arc-over is a spontaneous condition in which the ultor voltage across the ultor capacitor may be coupled to several of the connecting base pins, thereby subjecting the energizing circuitry and other circuitry sharing common current return paths to overvoltages from the relatively low impedance ultor capacitor source. Sensitive semiconductor devices may be damaged due to the overvoltages developed, and the relatively large arc-over currents flowing in the chassis and energizing circuitry.

Conventional techniques for arc-over protection involve shunting the arc-over current away from the energizing circuitry directly to the ultor ground return terminal through a spark gap coupled to the cathode ray tube connecting base pins. Relatively high impedance resistors may also be coupled between various ones of the base pins and the energizing circuitry to provide a voltage drop across the resistor for limiting arc-over voltages.

Nevertheless, arc-over current oscillation within the energizing circuitry may still develop. Stray capacity between the ultor ground return terminal and the chassis or energizing circuitry may provide a sufficiently low impedance AC current path from the ground return base pin to sustain relatively large and undesirable arc-over current oscillations.

In conventional digital television receivers, the settings of viewer controls such as audio volume, brightness, tint, and saturation are held in digital data storage elements. CRT arc-over oscillations may temporarily raise the ground potential well over its nominal value throughout the television display circuitry. These perturbations in ground potential may randomly change the states of digital data storage elements such as registers of flip-flops or random-access memories (RAM'S) and corrupt the data which they hold. A random corruption of these values is similar to randomly turning the corresponding user control potentiometers on an analog television receiver.

European Patent Application EP-A-0 021 288 discloses a power monitoring and distribution system as comprised in the pre-charaterizing part of claim 1.

The present invention as set out in claim 1 relates to a television display system including a cathode ray tube and first digital data storage means which may be subject to random changes in state resulting in corruption of the data stored therein caused by arc-over in the cathode ray tube. The system includes means coupled to the cathode ray tube for generating a control signal on the occurrence of an arc-over in the cathode ray tube; and fault recovery means including means coupled to the first digital data storage means and responsive to the control signal for changing the data held by the first digital data storage means to a predetermined value.

FIGURE 1 is a partial view of a cathode ray tube and a schematic diagram of associated circuitry which is useful in explaining the environment of the invention;

FIGURE 2 is a schematic diagram illustrating an equivalent circuit of the structure shown in FIGURE 1;

FIGURE 3 is a graph of current versus time which illustrates a waveform useful in describing the structure shown in FIGURE 1; and

FIGURE 4 is a block diagram, partially in schematic form, of a digital television receiver including data protection apparatus embodying the present invention.

As illustrated in FIG. 1, a CRT 21, of a television receiver, for example, includes a glass envelope 22, an inner conductive coating 23 and an outer conductive coating 24. Coatings 23 and 24 form the plates or electrodes of an ultor capacitor 40. During operation of the television receiver, a high voltage accelerating potential is developed across ultor capacitor 40. An alternating current voltage, such as developed by a flyback transformer, not illustrated, is rectified and coupled to inner coating 23 through a conventional ultor high voltage termination structure 25.

A conventional electron gun structure 26 is located interior of the neck portion 27 of the CRT envelope 22. A spring contact 29 connects inner coating 23 to an anode electrode 28 of electron gun 26. The ultor high voltage provides the energizing voltage for the anode electrode 28.

Energizing voltages for the other electrodes of electron gun 26, such as the focus and screen electrodes, are coupled through other base pins from energizing circuitry associated with the cathode ray tube and other television receiver components. As illustrated in FIG. 1, energizing voltage for the cathode electrode 30, for example, is coupled through a cathode base pin 31 from a video output energizing circuit 32, only partially illustrated.

Video output circuit 32 includes a driver transistor 33 coupled to a DC voltage source $+V_B$ through a resistor 34. Video input signals are coupled to the base of transistor 33 from conventional video processing circuitry not illustrated. Cathode drive signals at the collector of transistor 33 are coupled to cathode base pin 31 through a resistor 35. The termination from energizing circuit 32 to base pin 31 may be conventional and is indicated generally by a solder terminal C.

The emitter of transistor 33 is coupled to a common ground current return terminal S of energizing circuit 32 through a resistor 41. Such common return terminal S may be located on a frame or chassis 36 or on a separate printed circuit board, with the printed circuit board and chassis sharing mutual ground return paths.

Other electrode base pins, not illustrated, may be electrically interconnected with their respective energizing circuits in a manner similar to that described for the cathode base pin 31.

The outer conductive coating 24 serves as the ultor current return terminal. Electrical connection is provided from ground return base pin 37, which, for example, is coupled by a spark gap to the cathode base pin 31, to the ultor outer conductive coating 24 and to either the chassis 36 ground as illustrated in FIG. 1 or to the common current return terminals of the energizing circuitry for electron gun 26, not illustrated. Typically, conductor lengths 38, 38' and 39 are connected between base pin 37 and two different points on the outer coating 24, and between base pin 37 and chassis ground, respectively. The termination structures for the conductor lengths 38, 38' and 39 to base pin 37, outer conductive coating 24, and chassis 36 ground may be conventional and are indicated generally in FIG. 1 by respective solder terminals P, A, A' and common return terminal S.

Conductor lengths 38 and 38' form a first direct current path from ground base pin 37 to the ultor current return terminals of outer coating 24. Conductor length 39 forms a second direct current path from ground base pin 37 to the chassis or energizing circuitry common current return terminal S.

An AC current path for CRT arc-over currents between chassis 36 and the ultor current return terminal of outer coating 24 is formed by means of the stray capacitance between chassis 36 and outer coating 24, as illustrated in FIG. 1 by capacitors C_{S1} and C_{S2}. Although only C_{S1} and C_{S2} are illustrated, the stray capacitance of the chassis is distributed over the entire structure of chassis 36 and may be represented by a capacitor C_S of an equivalent circuit 50, schematically illustrated in FIG. 2.

In FIGURE 2, circuit 50 represents an electrical schematic of the arc-over current paths between terminal C and the external plate 24 of the ultor capacitor (terminal A), between terminal P and terminal A, between terminal P and common return terminal S and between terminal A and terminal S. Elements L_{38} and R_{38} represent the inherent inductance and resistance of conductor 38; L_{38}', and R_{38}', the inherent inductance and resistance of conductor 38'; and L_{39} and R_{39} the inherent inductance and resistance of conductor 39. Inductor L_{40}, resistor R_{40} and capacitor C_{40} represent, respectively, the ultor inductance, resistance and capacitance. Resistor R26 represents the resistance of the termination structure between the electron gun 26 and the inner coating 23. R_A represents the resistance of the outer conductive coating and the copper braid termination structure. Terminals A and A' are connected at separate points on this terminal structure. While there is some resistance and inductance inherent in this terminal structure, it is negligible, under arc-over conditions, when compared to the illustrated elements of the equivalent circuit 50. Accordingly, the path between points A and A' is modeled as a conductor. As noted above, the capacitor C_S, shown in phantom, represents the distributed capacitance between the outer conductive coating 24 and the chassis 36.

As illustrated by the arrows X-X in FIG. 1, arc-over may occur between cathode base pin 31 and ground return base pin 37. Much of the ultor voltage will be coupled to terminals P and C. First and second arc-over currents I_1 and I_2 will flow in

conductors 38 and 38' to provide the discharge path for ultor return current. As illustrated in FIG. 2, a voltage V_1 is developed between terminal P and terminal A; the termination of outer coating 24. This voltage will be developed across the parallel impedances of the inductor L_{38} and resistor R_{38} and the inductor L_{38}' and resistor R_{38}'.

The voltage V_1 acts as a driving potential during arc-over and generates a second oscillatory arc-over current I_3 flowing in conductor 39, chassis 36, and the ground current return paths of the electron gun electrode energizing circuitry. In FIG. 2, the normally underdamped oscillatory current I_3 is shown coupled to ultor ground return terminal A by means of the stray capacitance C_S. A coltage V_2 from terminal P to terminal S is produced by current I_3 across the series impedance of the inductor L_{39} and resistor R_{39}.

The underdamped oscillatory current I_3 is illustrated in FIG. 3 during typical arc-over situations. Arc-over begins near time t_1 creating current I_3 which oscillates for several cycles, reaching a first maximum near time t_2 and a first minimum near time t_3.

With oscillatory current I_3 as illustrated in FIG. 3, the voltage V_2 will assume relatively large values of both positive and negative magnitudes. The positive peak magnitude will be produced by the resistive voltage drop developed across R_{39} and also by the positive inductive voltage drop developed across L_{39} caused by the relatively large current change, $+dI_3/dt$, during the interval t_1-t_2, for example. A relatively large negative peak magnitude for voltage V_2 will be produced by the negative inductive voltage drop developed across L_{39} caused by the relatively large current change, $-dI_3/dt$, during the interval t_2-t_3.

Oscillatory currents similar to I_3, caused by arc-over conditions may flow in other circuitry having a common ground return path with chassis 36. These currents may cause this circuitry to develop voltages with relatively large positive and negative magnitudes. Voltages of this sort, applied to the ground connection of digital data storage elements such as metal-oxide-semiconductor (MOS) flip-flops, may randomly change the values of data stored in these elements.

FIGURE 4 illustrates a digital television receiver in which the values of the viewer controls for audio volume, image brightness, color tint and color saturation are held in digital data storage elements. The illustrated receiver also includes circuitry to detect the occurrence of a CRT arc-over condition - without inhibiting its discharge - and to restore the viewer control values held in the data storage elements which may have been affected by the arc-over condition.

Referring to FIGURE 4, radio frequency color television signals are received by antenna 408 and applied to the tuner, intermediate frequency amplifier and detector circuitry 410. Circuitry 410 includes conventional circuit elements and provides, at separate output terminals, baseband audio and baseband composite video signals. The baseband audio signals are applied to an audio processing unit (APU) 412. APU 412 may, for example, adjust the amplitude of the baseband audio signal according to viewer preferences for audio volume. In the present embodiment, a digital value corresponding to the audio volume level set by the viewer is applied to the APU 412 by a control microprocessor 440, described below. APU 412 applies a volume-adjusted signal to audio amplifier 414 which drives a loudspeaker 416 to reproduce the audio portion of a television program.

The baseband composite video signal from the circuitry 410 is applied to the analog-to-digital converter (ADC) 420. ADC 420 provides digital samples representing the composite video signal to video processing unit (VPU) 422, which, for example, separates the composite video signal into its luminance and chrominance components, adjusts the brightness of the luminance component, adjusts the tint and saturation of the chrominance components and otherwise processes the luminance and chrominance components to produce luminance and (R-Y) and (B-Y) color difference signals. The adjustments to the luminance and chrominance components are controlled by digital values representing the viewer preferred valued of brightness, tint and saturation applied to the VPU 422 by control microprocessor 440.

In the present embodiment, the viewer changes these values and the audio volume value via the viewer controls 450. Using these controls, the viewer may, for example, increase or decrease the values stored in the color saturation latch 442, the image brightness (pix) latch 444, the color tint latch 446, and the audio volume latch 448. The latches 442 through 448 are, for example, registers of MOS flip-flops. Each of the latches 442 through 448 is periodically read by the microprocessor 440. Based on these values, microprocessor 440 adjusts the level of the audio signal being processed by APU 412, the level of the luminance signal and the level and phase of the chrominance signals being processed by VPU 422 to conform to the viewer preferences.

When power is applied to the television receiver shown in FIGURE 4, the values held by the latches 442 through 448 may be zero or undefined. Shortly after power is applied, power-on reset circuitry 454 generates a pulse which is applied to one input pin of an OR gate 456 and, via gate 456 to a reset input pin of the control microprocessor 440. This pulse causes the microprocessor 440 to

retrieve preset values for the saturation, brightness, tint and volume latches from an electronically erasable programmable read-only memory (EEPROM) 452 and to copy these values into the corresponding latches 442 through 448. The values held in EEPROM 452 may be set at the factory or they may be changed by the viewer to the adjusted values in the latches 442 through 448. To change the preset values in EEPROM 452, the viewer is provided with a preset switch in the viewer controls 450. This switch applies a pulse to the microprocessor 440 causing it to copy the values in the latches 442 through 448 into the corresponding storage cells of EEPROM 452.

VPU 422 applies the adjusted digital signals representing the luminance signal and the (R-Y) and (B-Y) color difference signals to a digital-to-analog converter (DAC) 423. In the present embodiment, DAC 423 and ADC 420 may be incorporated within the same integrated circuit. DAC 423 also includes a matrix which converts the digital values representing the luminance signal and the (R-Y) and (B-Y) color difference signals into analog red, green and blue primary color signals and applies these analog signals to an RGB amplifier 424. RGB amplifier 424 develops the cathode drive signals R, G and B which are applied to the base pins of the CRT. Accordingly, RGB amplifier 424 includes the transistor 33 and resistors 34, 35 and 41, as shown in FIGURE 1.

ADC 420 also applies the digitized composite video signal to a deflection processing unit (DPU) 430. This circuitry, for example, separates the horizontal synchronization pulses from the composite video signal and generates a horizontal drive signal which is applied to the horizontal output circuit 432. DPU 430, microprocessor 440, APU 412, ADC 420 and VPU 422 may be commercially available integrated circuits such as the MAA 2500, MAA 2000, MAA 2400, MAA 2100 and MAA 2200 respectively manufactured by ITT Intermetal GmbH, Freiburg, West Germany.

The circuitry 432 includes the horizontal output amplifier, horizontal output, or flyback, transformer and damper diode of a conventional television receiver. One of the signals provided by the horizontal output circuit 432 is a high voltage alternating current which is applied to the high voltage supply circuit 434. Circuit 434 rectifies the high voltage alternating current and develops the anode voltage for the CRT 21. As set forth above, this anode voltage is applied to the inner conductive coating 23 of the CRT 21 which forms one plate of the ultor capacitor. The outer conductive coating 24 of the CRT 21 is the second plate of the ultor capacitor. The outer coating 24 is coupled to the ground return base pin 37 of the CRT 21 by the conductors 38 and 38'. The base pin 37 is coupled to spark gaps SG_1, SG_2 and SG_3. In the present emboidment, these spark gaps protect the circuitry coupled to the cathode base pins of the CRT 21 from the high voltages and currents which may flow during a CRT arc-over. The spark gaps conduct the arc-over current to the outer conductive coating 24 via the conductors 38 and 38' and to chassis ground via conductor 39.

The circuitry used to detect the CRT arc-over condition includes ferrite torroid 460, diode 462, resistor 464, capacitor 466 and zener diode 468. The conductor 38 passes through the torroid 460 and acts as the primary winding of a pulse transformer 461. The secondary winding 465 of the pulse transformer consists, for example, of two turns of wire wrapped around the torroid. One end of the secondary winding is connected to ground and the other end is connected to the anode terminal of a diode 462.

When a CRT arc-over condition occurs, a current flows through the conductor 38 from, for example, the spark gap SG_1 to the outer conductive coating 24 of CRT 21. This current induces a similar current in the secondary winding of the pulse transformer 461. The current in the secondary winding is rectified by the diode 462. A resistor 464, connected between the anode terminal of the diode 462 and the first terminal of a capacitor 466, attenuates the current flow that charges the capacitor 466, the second terminal of which is connected to ground. Zener diode 468 is connected in parallel with capacitor 466 with its cathode terminal connected to ground. The interconnected first terminal of the capacitor 466 and anode terminal of zener diode 468 are also connected to the second input terminal of OR gate 456. Zener diode 468 acts to limit the voltage developed across the capacitor 466 to prevent damage to OR gate 456. By appropriate choice of component values, the CRT arc-over detection circuit described above, may be designed to produce a pulse at the input of OR gate 456 which has sufficient amplitude and duration to propagate through gate 456 to the reset input terminal of control microprocessor 440. This pulse causes the microprocessor to restore the values in the latches 442 through 448 from the EEPROM 452 as set forth above in reference to the power on reset function.

The CRT arc-over sensing circuit is coupled to only one of the conductors 38 and 38' which connect the ground return base pin 37 to the outer conductive coating 24 of CRT 21. This configuration leaves a low impedance path via conductor 38' for the rapid discharge of arc-over currents. Without this discharge path, the additional impedance in the direct current path between the ground base pin 37 and the ultor current return terminals of the outer coating 24 caused by the torroid 460, may

allow a large potential to develop at the base pins of the CRT. This potential may be of sufficient magnitude to harm the energizing circuitry connected to these base pins.

It is contemplated that other circuitry may be used to detect CRT arc-over conditions. For example, circuitry (not shown) may be coupled to the high voltage supply 434 which would sense a sudden drop in its output potential caused by CRT arc-over and provide an output pulse to OR gate 456.

To summarize the operation of the described embodiment, a CRT arc-over condition produces a large current pulse which, when it discharges via the chassis ground, disrupts the reference ground potentials of other circuitry coupled to the chassis ground. The affected circuitry includes digital data storage elements which may experience random state changes caused by the fluctuating ground potential. The CRT arc-over condition is detected by circuitry which applies a pulse to the reset terminal of the microprocessor, causing it to restore the potentially corrupted data in the data storage elements using preset data stored in a less volatile programmable read only memory.

Claims

1. Apparatus comprising:

first digital data storage means (442-450) for storing data representative of selected parameters of said apparatus, said first digital storage means being subject to a disruption of power supplied to said first digital storage means tending to corrupt said data stored in said first digital storage means;

second digital data storage means (452) for storing data to be written into said first digital storage means following said power disruption;

fault recovery means (440,452,456) responsive to a first control signal for causing said digital data stored in said second digital data storage means to be written into said first digital data storage means;

control means (454,461) generating said first control signal in response to said disruption of power;

characterized in that

said apparatus comprises a television display system including a cathode ray tube (21) subject to arc-over;

said control means (454,461) being coupled to said cathode ray tube (21) for generating a second control signal in response to the occurrence of said arc-over in said cathode ray tube;

said data stored in said first digital storage means tending to be corrupted by said arc-over;

said second digital data storage means comprising nonvolatile memory means for retaining uncorrupted said digital data stored in said second digital data storage means despite the occurrence of said power disruption or said arc-over, said uncorrupted retention of said data in said nonvolatile memory means occurring continuously rather than in response to detection of the occurrence of said power disruption or said arc-over;

said fault recovery means (440, 452, 456) being responsive to said second control signal for writing said data stored in said second digital data storage means into said first digital data storage means.

2. Apparatus as claimed in claim 1 including power-on pulse generating means (454) for generating a pulse signal when power is applied to the television display system wherein said fault recovery means includes means (456) responsive to said control signal and to said power-on pulse signal for changing the data held by said first digital data storage means to said predetermined value.

3. Apparatus as claimed in claim 1 or 2 wherein

said first digital data storage means (442-450) includes means (450) for changing the data held in said first digital data storage means, and means (440) coupled to said first digital data storage means (442-450) and to said second data storage means (452) for selectively copying digital values from said first digital storage means to said second data storage means.

4. Apparatus as claimed in claim 1, 2 or 3 wherein

said first digital data storage means (442-450) comprises a plurality of metal-oxide semiconductor flip-flops;

said second data storage means (452) comprises an electronically erasable programmable read-only memory (EEPROM); and

said means (440) for copying digital data values from said second data storage means to said first digital data storage means includes a microprocessor.

5. Apparatus as claimed in any preceding claim wherein said cathode ray tube (21) includes an ultor capacitor (40) having first (23) and second (24) plates, an electrode (25) for coupling a source of high voltage to said first plate, an energizing electrode (30), a base pin (31)

allow a large potential to develop at the base pins of the CRT. This potential may be of sufficient magnitude to harm the energizing circuitry connected to these base pins.

It is contemplated that other circuitry may be used to detect CRT arc-over conditions. For example, circuitry (not shown) may be coupled to the high voltage supply 434 which would sense a sudden drop in its output potential caused by CRT arc-over and provide an output pulse to OR gate 456.

To summarize the operation of the described embodiment, a CRT arc-over condition produces a large current pulse which, when it discharges via the chassis ground, disrupts the reference ground potentials of other circuitry coupled to the chassis ground. The affected circuitry includes digital data storage elements which may experience random state changes caused by the fluctuating ground potential. The CRT arc-over condition is detected by circuitry which applies a pulse to the reset terminal of the microprocessor, causing it to restore the potentially corrupted data in the data storage elements using preset data stored in a less volatile programmable read only memory.

Claims

1. Apparatus comprising:

first digital data storage means (442-450) for storing data representative of selected parameters of said apparatus, said first digital storage means being subject to a disruption of power supplied to said first digital storage means tending to corrupt said data stored in said first digital storage means;

second digital data storage means (452) for storing data to be written into said first digital storage means following said power disruption;

fault recovery means (440,452,456) responsive to a first control signal for causing said digital data stored in said second digital data storage means to be written into said first digital data storage means;

control means (454,461) generating said first control signal in response to said disruption of power;

characterized in that

said apparatus comprises a television display system including a cathode ray tube (21) subject to arc-over;

said control means (454,461) being coupled to said cathode ray tube (21) for generating a second control signal in response to the occurrence of said arc-over in said cathode ray tube;

said data stored in said first digital storage means tending to be corrupted by said arc-over;

said second digital data storage means comprising nonvolatile memory means for retaining uncorrupted said digital data stored in said second digital data storage means despite the occurrence of said power disruption or said arc-over, said uncorrupted retention of said data in said nonvolatile memory means occurring continuously rather than in response to detection of the occurrence of said power disruption or said arc-over;

said fault recovery means (440, 452, 456) being responsive to said second control signal for writing said data stored in said second digital data storage means into said first digital data storage means.

2. Apparatus as claimed in claim 1 including power-on pulse generating means (454) for generating a pulse signal when power is applied to the television display system wherein said fault recovery means includes means (456) responsive to said control signal and to said power-on pulse signal for changing the data held by said first digital data storage means to said predetermined value.

3. Apparatus as claimed in claim 1 or 2 wherein

said first digital data storage means (442-450) includes means (450) for changing the data held in said first digital data storage means, and means (440) coupled to said first digital data storage means (442-450) and to said second data storage means (452) for selectively copying digital values from said first digital storage means to said second data storage means.

4. Apparatus as claimed in claim 1, 2 or 3 wherein

said first digital data storage means (442-450) comprises a plurality of metal-oxide semiconductor flip-flops;

said second data storage means (452) comprises an electronically erasable programmable read-only memory (EEPROM); and

said means (440) for copying digital data values from said second data storage means to said first digital data storage means includes a microprocessor.

5. Apparatus as claimed in any preceding claim wherein said cathode ray tube (21) includes an ultor capacitor (40) having first (23) and second (24) plates, an electrode (25) for coupling a source of high voltage to said first plate, an energizing electrode (30), a base pin (31)

* C L M S *

coupled to said energizing electrode, a ground return base pin (37), means (SG_1, SG_2, SG_3) coupling said energizing electrode base pin to said ground return base pin for discharging excess current applied to said energizing electrode during arc-over between the first plate of said ultor capacitor and said energizing electrode, and ultor current return means (38, 38') coupled between said ground return base pin (37) and the second electrode of said ultor capacitor for returning said excess current to said ultor capacitor and wherein said control means (461) is coupled to said ultor current return means for generating a signal indicative of a rapid increase in the current flow therethrough.

6. Apparatus as claimed in claim 5

wherein said control means includes a transformer (461), said ultor current return means (38) forming a primary winding of said transformer said transformer (461) including a secondary winding (465) having a first terminal coupled to a source of reference potential (ground) for providing, at a second terminal, an alternating current signal with respect to said reference potential indicative of the magnitude of the current flow through said primary winding;

a rectifier (462), coupled to the second terminal of said secondary winding of said transformer for converting said alternating current signal into a direct current signal; and

a capacitor (466) coupled between said rectifier and said source of reference potential to provide a control potential indicative of the occurrence of an arc-over in the cathode ray tube.

Patentansprüche

1. Vorrichtung mit:

ersten Speichermitteln (442-450) zur Speicherung von digitalen Daten, die ausgewählte Parameter der Vorrichtung darstellen, wobei die ersten digitalen Speichermittel einer Unterbrechung des den ersten digitalen Speichermitteln zugeführten Stroms unterworfen sind, die die in den ersten digitalen Speichermitteln gespeicherten Daten verfälschen kann;

zweiten Speichermitteln (452) zur Speicherung von digitalen Daten, die in die ersten digitalen Speichermittel nach der Stromunterbrechung eingeschrieben werden sollen;

Fehlerbeseitigungsmitteln (440, 452, 456), die auf ein ertes Steuersignal ansprechen, um zu bewirken, daß die in den zweiten digitalen Speichermitteln gespeicherten Daten in die ersten digitalen Speichermittel eingeschrieben werden;

Steuermitteln (454, 461) zur Erzeugung des ersten Steuersignals in Abhängigkeit von der Stromunterbrechung; dadurch gekennzeichnet,

daß die Vorrichtung ein Fernsehanzeigesystem mit einer einem Überschlag ausgesetzten Kathodenstrahlröhre enthält;

daß die Steuermittel (454, 461) mit der Kathodenstrahlröhre (21) gekoppelt sind, um ein zweites Steuersignal in Abhängigkeit von dem Auftreten des Überschlags in der Kathodenstrahlröhre zu erzeugen;

daß die in den ersten digitalen Speichermitteln gespeicherten Daten dazu neigen, durch den Überschlag verfälscht zu werden;

daß die zweiten digitalen Speichermittel Permanentspeichernittel umfassen, um die in den zweiten digitalen Speichermitteln gespeicherten Daten trotz des Auftretens der Stromunterbrechung oder des Überschlags unverfälscht zu halten, wobei das Unverfälschthalten der Daten in den Permanentspeichermitteln kontinuierlich erfolgt anstatt in Abhängigkeit von der Feststellung des Auftretens der Stromunterbrechung oder des Überschlags;

daß die Fehlerbeseitigungsmittel (440, 452, 456) auf das zweite Steuersignal ansprechen, um die in den zweiten digitalen Speichermitteln gespeicherten Daten in die ersten digitalen Speichermittel einzuschreiben.

2. Vorrichtung nach Anspruch 1, mit Mitteln (454) zur Erzeugung eines Strom-EIN-Impulses, um ein Impulssignal zu erzeugen, wenn dem Fernsehanzeigesystem Strom zugeführt wird, wobei die Fehler-beseitigungsmittel Mittel (456) enthalten, die auf das Steuersignal und auf das Strom-EIN-Impulssignal ansprechen, um die in den ersten digitalen Speichermitteln gespeicherten Daten auf den vorgegebenen Wert zu ändern.

3. Vorrichtung nach Anspruch 1 oder 2, bei der die ersten Speichermittel (442-450) für digitale Daten Mittel (450) enthalten, um die in den ersten Speichermitteln gehaltenen Daten zu ändern, wobei Mittel (440) mit den ersten Speichermitteln (442-450) und den zweiten Speichermitteln (452) gekoppelt sind, um wahlweise digitale Werte aus den ersten digitalen Speichermitteln in die zweiten Datenspeichermittel zu kopieren.

4. Vorrichtung nach Anspruch 1, 2 oder 3, bei der die ersten Speichermittel (442-450) für digitale Daten eine Vielzahl von Metalloxid-Halbleiter-

* C L M S *

Flip-Flops umfassen; bei der die zweiten Speichermittel (452) für digitale Daten einen elektronisch löschbaren Nurlesespeicher (EEPROM) umfassen; und bei der die Mittel (440) zum Kopieren der digitalen Werte aus den zweiten Datenspeichermitteln in die ersten Datenspeichermittel einen Mikroprozessor enthalten.

5. Vorrichtung nach einem der vorhergehenden Ansprüche, bei der die Kathodenstrahlröhre (21) einen Endanodenkondensator (40) mit einer ersten (23) und einer zweiten Platte (24), eine Elektrode (25) zum Verbinden einer Hochspannungsquelle mit der ersten Platte (23), eine Speiseelektrode (30), einen mit der Speiseelektrode verbundenen Basisstift (31), einen Erdrückleitungs-Basisstift (37), Mittel (SG_1, SG_2, SG_3) zum Verbinden des Speiseelektroden-Basisstifts mit dem Erdrückleitungs-Basisstift, um überschüssigen Strom, der der Speiseelektrode während eines Überschlags zwischen der ersten Platte des Endanodenkondensators und der Speiseelektrode zugeführt wird, zu entladen, und Endanoden-Stromrückleitungsmittel (38, 38') zwischen dem Erdrückleitungs-Basisstift (37) und der zweiten Elektrode des Endanodenkondensators, um den überschüsigen Strom zu dem Endanodenkondensator zurückzuleiten, enthält, wobei die Steuermittel (461) mit den Endanoden-Stromrückleitungsmitteln gekoppelt sind, um ein Signal zu erzeugen, das ein schnelles Ansteigen eines hindurchfließenden Stromes anzeigt.

6. Vorrichtung nach Anspruch 5, bei der die Steuermittel einen Transformator (461) enthalten, wobei die EndanodenStromrück-leitungsmittel (38) eine Primärwicklung des Transformators bilden und der Transformator (461) eine Sekundärwicklung (465) enthält, die eine erste, mit einer Bezugsspannungsquelle (Erde) verbundene Klemme hat, um an einer zweiten Klemme ein Wechselstromsignal in Bezug auf das Bezugspotential zu erzeugen, das die Größe des Stromflusses durch die Primärwicklung angibt; bei der mit der zweiten Klemme der Sekundärwicklung des Transformators ein Gleichrichter (462) verbunden ist, um das Wechselstromsignal in ein Gleichstromsignal umzuwandeln; und bei der ein Kondensator (466) zwischen dem Gleichrichter und der Bezugspotentialquelle angeordnet ist, um ein Steuerpotential zu erzeugen, das das Auftreten eines Überschlags in der Kathodenstrahlröhre anzeigt.

Revendications

1. Dispositif comprenant :
   - des premiers moyens de stockage de données numériques (442-450) pour emmagasiner des données représentant des paramètres sélectionnés dudit dispositif, lesdits premiers moyens de stockage numériques étant sujet à une disruption de l'énergie délivrée auxdits premiers moyens de stockage numériques tendant à altérer lesdites données stockées dans lesdits premiers moyens de stockage numériques ;
   - des seconds moyens de stockage de données numériques (452) pour stocker des données devant être inscrites dans lesdits premiers moyens de stockage numériques à la suite de ladite disruption d'énergie ;
   - des moyens de redressement de défaut (440, 452, 456) agissant en réponse à un premier signal de commande pour amener lesdites données numériques stockées dans lesdits seconds moyens de stockage numériques à être inscrites dans lesdits premiers moyens de stockage de données numériques ;
   - des moyens de commande (454, 461) pour générer ledit premier signal de commande en réponse à ladite disruption de puissance ;

   caractérisé en ce que
   - ledit dispositif comprend un système d'affichage de télévision comportant un tube à rayons cathodiques (21) sujet à fuites ;
   - lesdits moyens de commande (454, 461) étant couplés audit tube à rayons cathodiques (21) pour générer un second signal de commande en réponse à l'apparition de ladite fuite dans ledit tube à rayons cathodiques ;
   - lesdites données stockées dans les premiers moyens de stockage numériques tendant à être altérées par ladite fuite.
   - lesdits seconds moyens de stockage de données numériques comprenant une mémoire non volatile pour maintenir inaltérée lesdites données numériques stockées dans lesdits seconds moyens de stockage de données numériques malgré l'apparition de ladite disruption d'énergie ou de ladite fuite, ledit maintien à l'état non altéré desdites données dans la mémoire non volatile survenant de manière continue plutôt qu'en réponse à une détection de la survenue de ladite disrup-

* C L M S *

tion d'énergie ou de ladite fuite ;

- lesdits moyens de redressement de défaut (440, 452, 456) agissant en réponse audit second signal de commande pour inscrire les données emmagasinées dans lesdits seconds moyens de stockage de données numériques, dans lesdits premier moyens de stockage de données numériques.

2. Dispositif selon la revendication 1 comportant des moyens pour générer une impulsion lors de la mise sous puissance (454), générant un signal d'impulsion quand de l'énergie est appliquée au système d'affichage de télévision dans lequel lesdits moyens de redressement de défaut comportent des moyens (456) agissant en réponse audit signal de commande et audit signal d'impulsion généré lors de la mise en puissance pour modifier les données maintenues dans les premiers moyens de stockage numériques, en ladite valeur prédéterminée.

3. Dispositif selon la revendication 1 ou 2 dans lequel lesdits premiers moyens de stockage de données numériques (442-450) comportent des moyens (450) pour modifier les données conservées dans lesdits premiers moyens de stockage de données numériques et des moyens (440) couplés auxdits premiers moyens de stockage de données numériques (442-450) et auxdits seconds moyens de stockage de données (452) pour copier sélectivement des valeurs numériques des premiers moyens de stockage numériques vers les seconds moyens de stockage de données.

4. Dispositif selon la revendication 1, 2 ou 3 dans lequel

- lesdits premiers moyens de stockage de données numériques (442, 450) comprennent une pluralité de flip-flop semiconducteurs métal-oxyde ;
- lesdits seconds moyens de stockage de données (452) comprennent une mémoire morte programmable effaçable électriquement (EEPROM) et,
- lesdits moyens (440) pour copier des valeurs de données numériques des seconds moyens de stockage de données vers lesdits premiers moyens de stockage de données numériques comprennent un microprocesseur.

5. Dispositif selon l'une des revendications précédentes dans lequel ledit tube à rayons cathodiques (21) comporte un condensateur d'accélération final (40) ayant des première (23) et seconde (24) plaques, une électrode (25) pour coupler une source de haute tension à ladite première plaque, une électrode d'excitation (30), une broche de base (31) couplée à ladite électrode d'excitation, une broche de base de retour à la terre (37), des moyens (SG_1, SG_2, SG_3) couplant ladite broche de base d'électrode d'excitation à ladite broche de base de retour à la terre pour décharger du courant en excès appliqué à ladite électrode d'excitation lors d'une fuite entre la première plaque dudit condensateur d'accélération finale et ladite électrode d'excitation et des moyens de retour du courant d'accélération finale (38, 38') couplés entre ladite broche de base de retour à la terre (37) et la seconde électrode dudit condensateur d'accélération finale pour ramener ledit courant en excès audit condensateur d'accélération finale et, dans lequel lesdits moyens de commande (461) sont couplés auxdits moyens de retour du courant d'accélération finale pour générer un signal indiquant une augmentation rapide du flux de courant y circulant.

6. Dispositif selon la revendication 5 dans lequel lesdits moyens de commande comprennent un transformateur (461), lesdits moyens de retour du courant d'accélération finale (38) formant un enroulement primaire dudit transformateur, ledit transformateur (461) incluant un enroulement secondaire (465) ayant une première borne couplée à une source de potentiel de référence (masse) pour fournir, sur une seconde broche, un signal en courant alternatif, par rapport audit potentiel de référence, indiquant l'amplitude du flux de courant au travers dudit enroulement primaire ;

- un redresseur (462) couplé à la seconde borne dudit second enroulement secondaire du transformateur pour transformer ledit signal en courant alternatif en un signal en courant direct et,
- un condensateur (466) couplé entre ledit redresseur et ladite source de potentiel de référence, pour fournir un potentiel de commande indiquant l'apparition d'une fuite dans le tube à rayons cathodiques.

* C L M S *