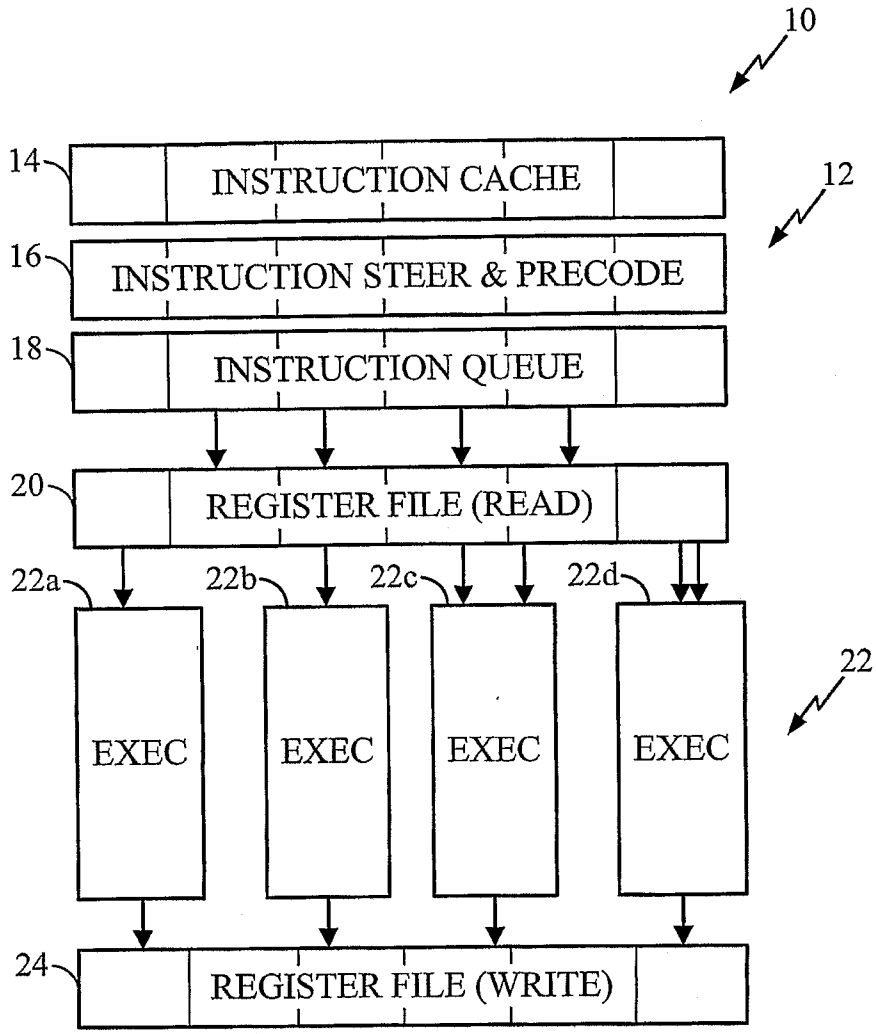

10
14
INSTRUCTION CACHE
12
16
INSTRUCTION STEER & PRECODE
18
INSTRUCTION QUEUE
20
REGISTER FILE (READ)
22a
22b
22c
22d
EXEC
EXEC
EXEC
EXEC
22
24
REGISTER FILE (WRITE)

FIG. 1

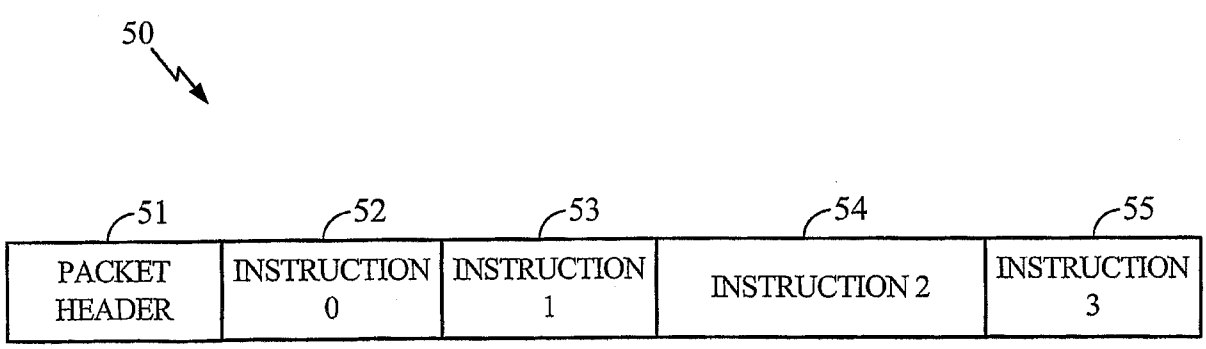

50
51
52
53
54
55
PACKET HEADER
INSTRUCTION 0
INSTRUCTION 1
INSTRUCTION 2
INSTRUCTION 3

FIG. 4

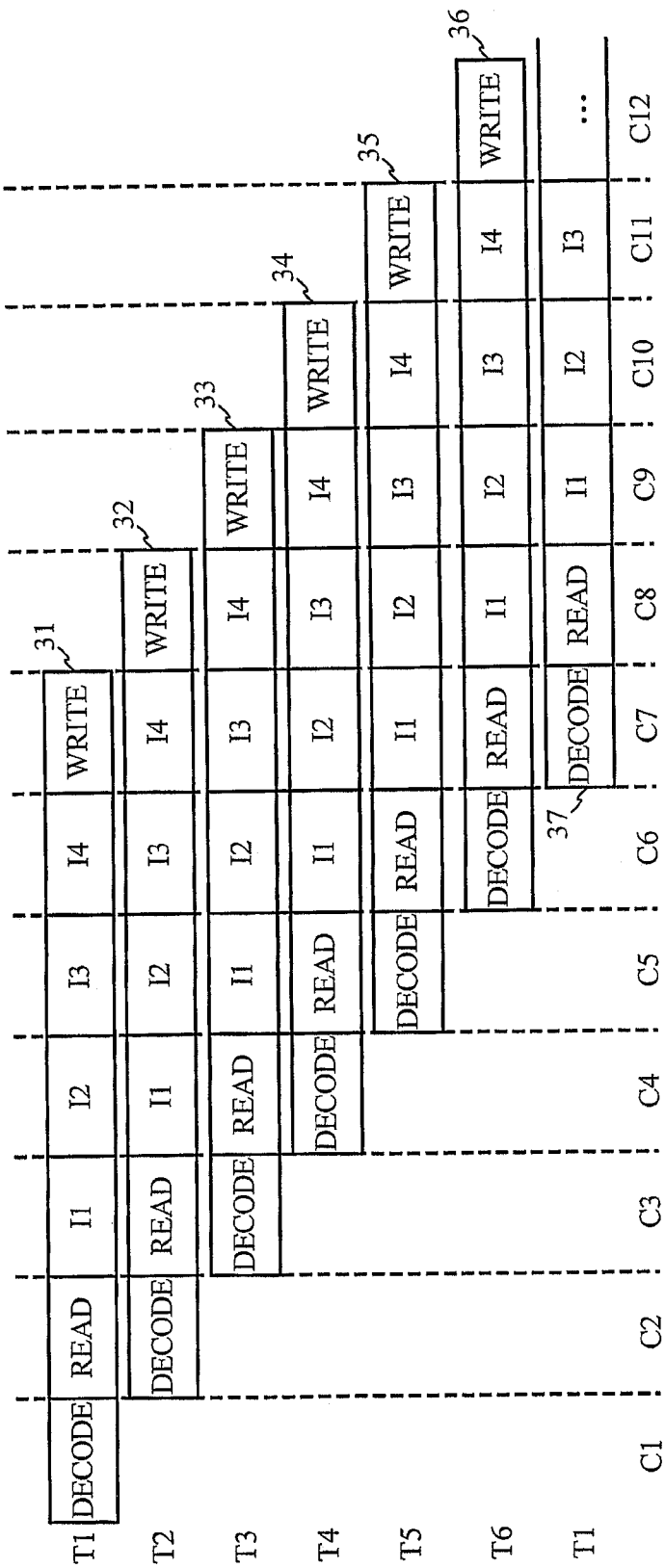

T1
T2
T3
T4
T5
T6
T1
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
DECODE
READ
I1
I2
I3
I4
WRITE
31
32
33
34
35
36
37

FIG. 2

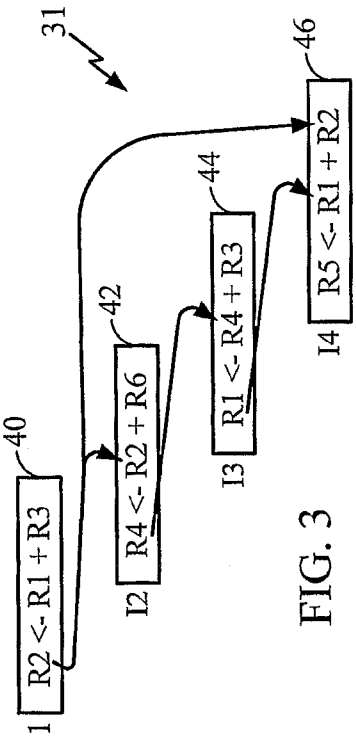

31
I1
R2 <- R1 + R3
40
I2
R4 <- R2 + R6
42
I3
R1 <- R4 + R3
44
I4
R5 <- R1 + R2
46

FIG. 3