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ABSTRACT

A digital processing device P, generally configured
 as a regular tree with $n+1$ levels $S_0, S_1, S_2 \dots S_n$
 and degree k , is provided in the form of a circuit P_n
 5 on the level S_n and forms the root node of the tree,
 an underlying level $S_{n-q}, q=1,2,\dots,n-1$, in the
 circuit P comprising generally k^q circuits P_{n-q}
 provided nested in the k^{q-1} circuits P_{n-q+1} on the
 overlying level S_{n-q+1} , each circuit P_{n-q+1} on this
 10 level comprising k circuits P_{n-q} . A for $q=n$ defined
 zeroth level in the circuit P_n comprises from $k^{n-1}+1$
 to k^n circuits P_0 which form kernel processors in the
 processing device P and on the level S_0 constitute
 the leaf nodes of the tree, the kernel processor P_0
 15 being provided nested in a number from 1 to k in
 each of the circuits P_1 on the level S_1 . Each of the
 circuits $P_1, P_2, \dots P_n$, comprises a logic unit E
 which generally is connected with circuits $P_0, P_1, \dots$
 P_{n-1} provided nested in the former circuits on the
 20 nearest underlying level and is additionally adapted
 to connect nodes on the same or underlying levels
 in neighbour trees. Each of the circuits $P_0, P_1, \dots P_n$
 has additionally identical interfaces I, such that
 $I_{P_0} = I_{P_1} = \dots I_{P_n}$.

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(Figs. 1 and 2)



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